ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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ASNT6793-DIE
DC-33*GHz* 1-to-3 Analog Signal Splitter

- DC to 33*GHz* broadband linear signal splitter
- Exhibits an extra-flat frequency response ideal for PAM3 and PAM4 applications
- One differential CML-type input port and three phase-matched differential CML-type output ports
- Single ended input linearity range up to $0.6V_{pk\text{-}pk}$ and differential input linearity up to $1.2V_{pk\text{-}pk}$
- Two gain settings: default and high
- Two peaking settings: default and high
- Adjustable internal currents for power consumption and bandwidth control
- Low jitter and limited temperature variation over industrial temperature range
- Single +3.6*V* or -3.6*V* power supply
- Power consumption: 1*W* typical
- Fabricated in flip-chip configuration with 44 Cu pillar mounting structures
- Die size 1.34x1.34mm^2

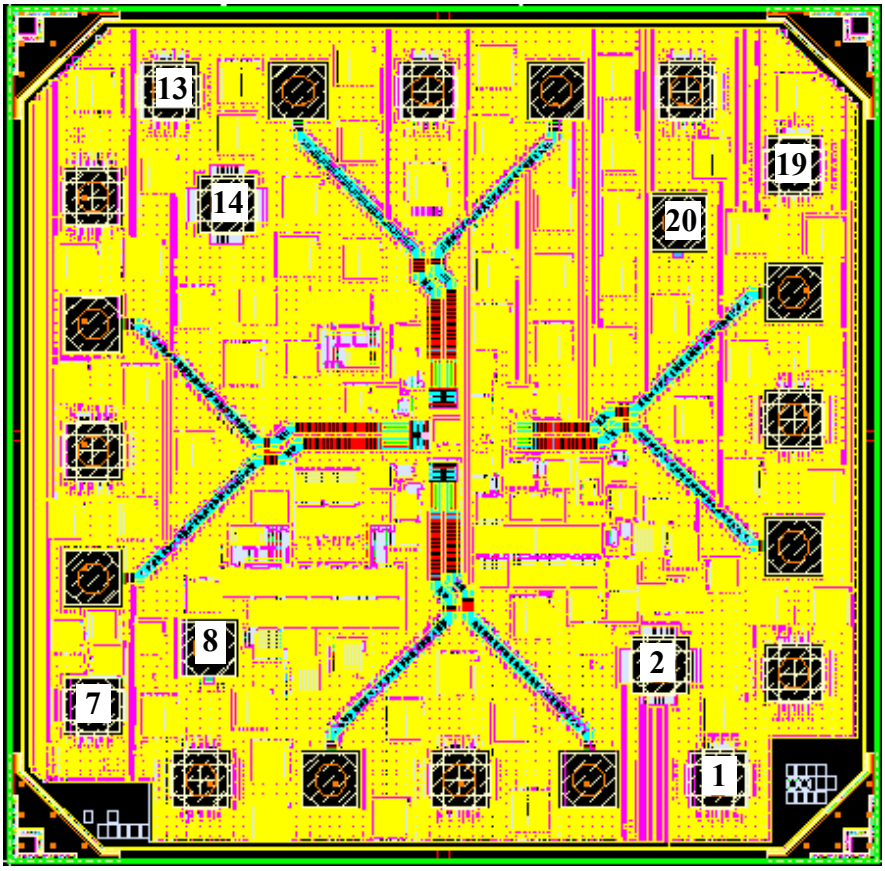

Fig. 1. Die Top View

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DESCRIPTION

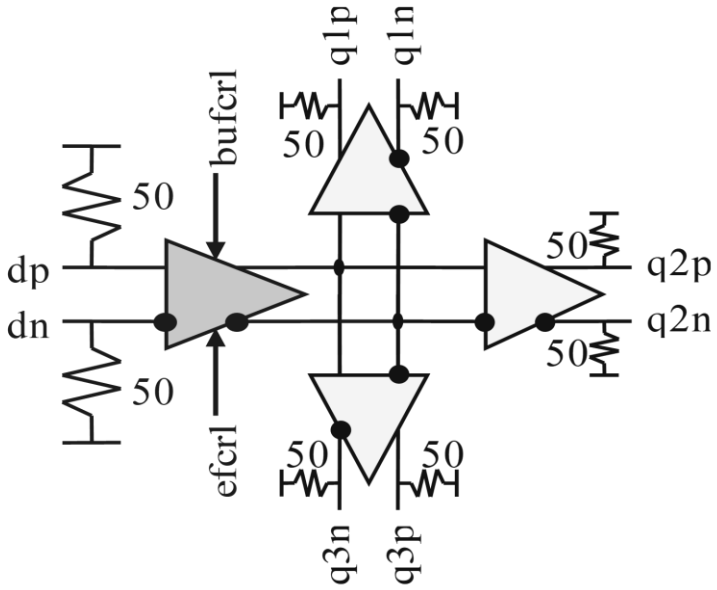

Fig. 2. Functional Block Diagram

The temperature stable ASNT6793-DIE 1-to-3 analog signal splitter is intended for use in high-speed interleaved ADCs or similar systems. Its extra-flat frequency response is ideal for PAM3 and PAM4 signals. The IC shown in Fig. 2 can receive a broad-band analog signal at its differential input dp/dn and effectively distribute it to three separate phase matched differential outputs q1p/q1n, q2p/q2n, and q3p/q3n with a nominal gain of 0*dB*. Low-speed analog current controls efcrl and bufcrl are available for power consumption and bandwidth adjustments. Each control range is separated into two zones: Zone 1 and Zone 2. While each zone has a full adjustment range for the corresponding current control, switching between zones allows for the binary selection between default and maximum values for peaking and gain. A relatively flat frequency response with variation of no more than ±0.5*dB* within DC-to-30*GHz* can be achieved with these two control voltages.

The part's I/O's support a CML logic interface with an on-chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.6*V*) or positive supply (vcc = +3.6*V* and vee = 0.0*V* = ground). In the case of a positive supply, all I/Os need AC termination when connected to any devices with a 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.6*V*.

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TYPICAL PERFORMANCE CHARACTERISTICS

The frequency responses of ASNT6793-DIE at various efcrl and bufcrl settings are shown in Fig. 3, Fig. 4, Fig. 5, Fig. 6, Fig. 7, Fig. 8, Fig. 9, Fig. 10.

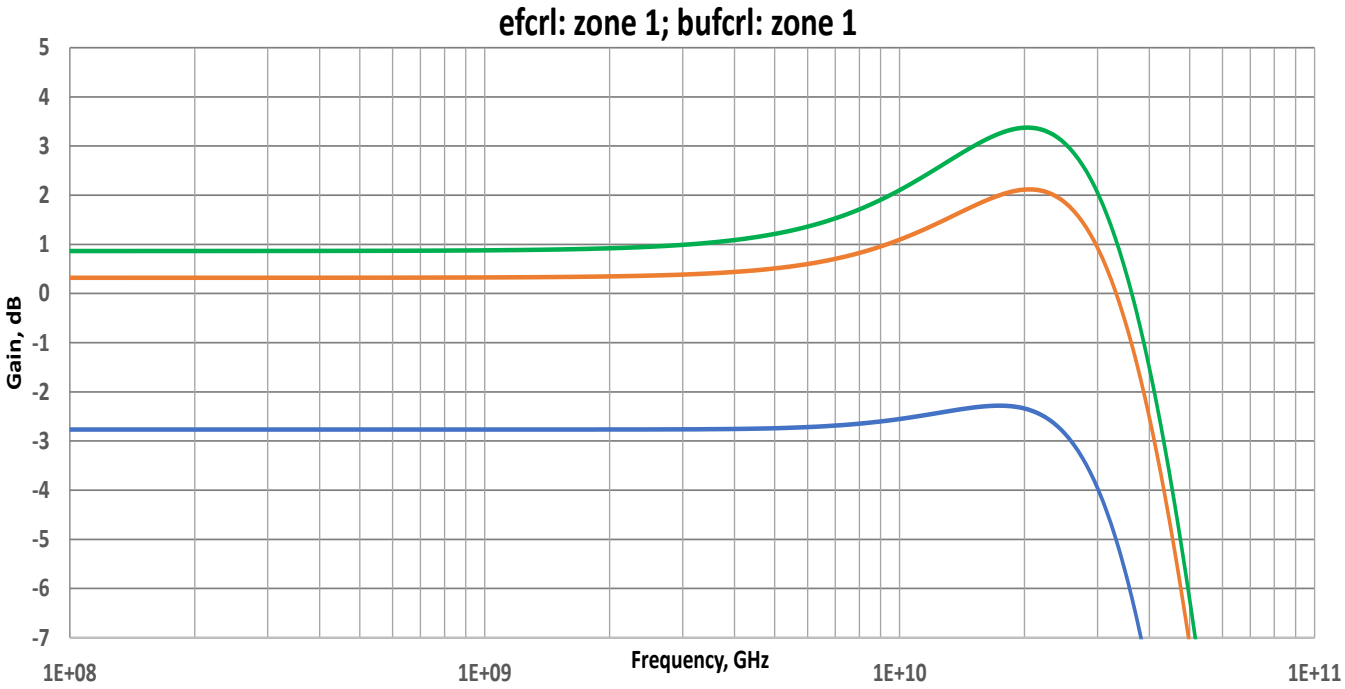

Fig. 3. Frequency Response. efcrl=+2.3V, bufcrl=+2.1V/+2.3V/+2.5V

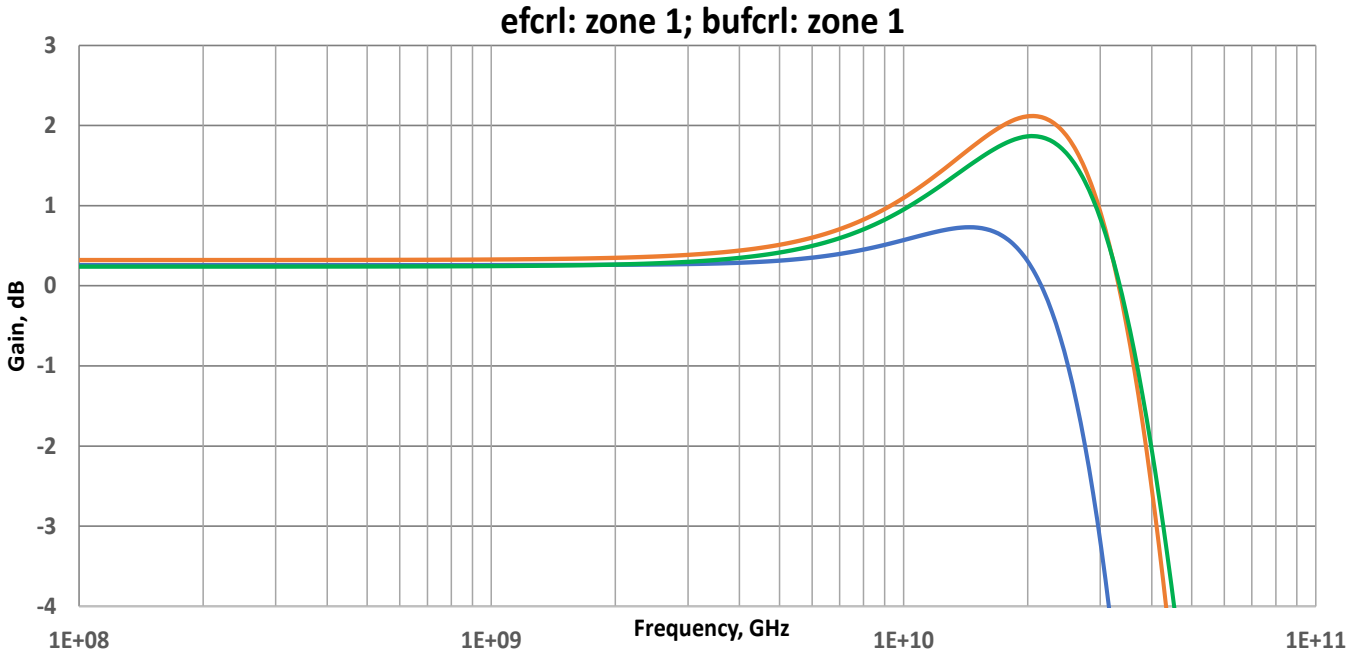

Fig. 4. Frequency Response. efcrl=+2.1V/+2.3V/+2.5V, bufcrl=+2.3V

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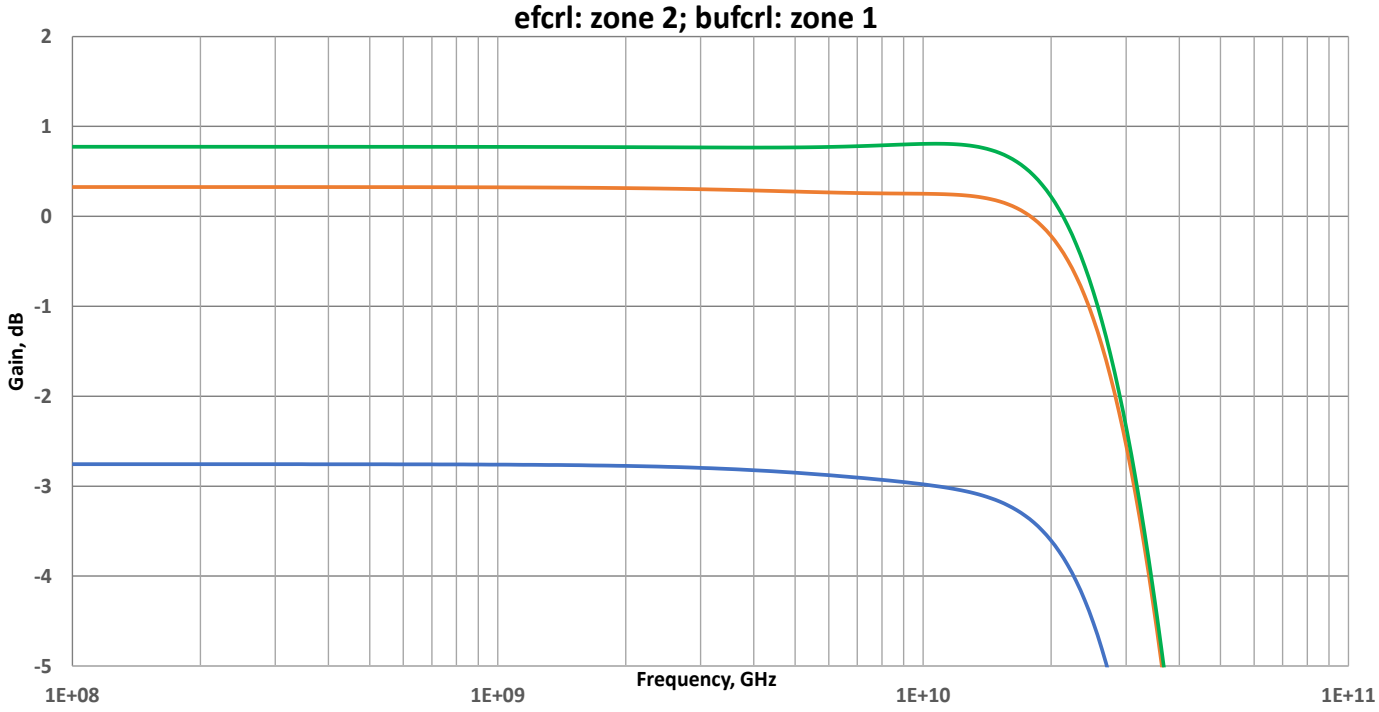

Fig. 5. Frequency Response. efcrl=+3.2V, bufcrl=+2.1V/+2.3V/+2.5V

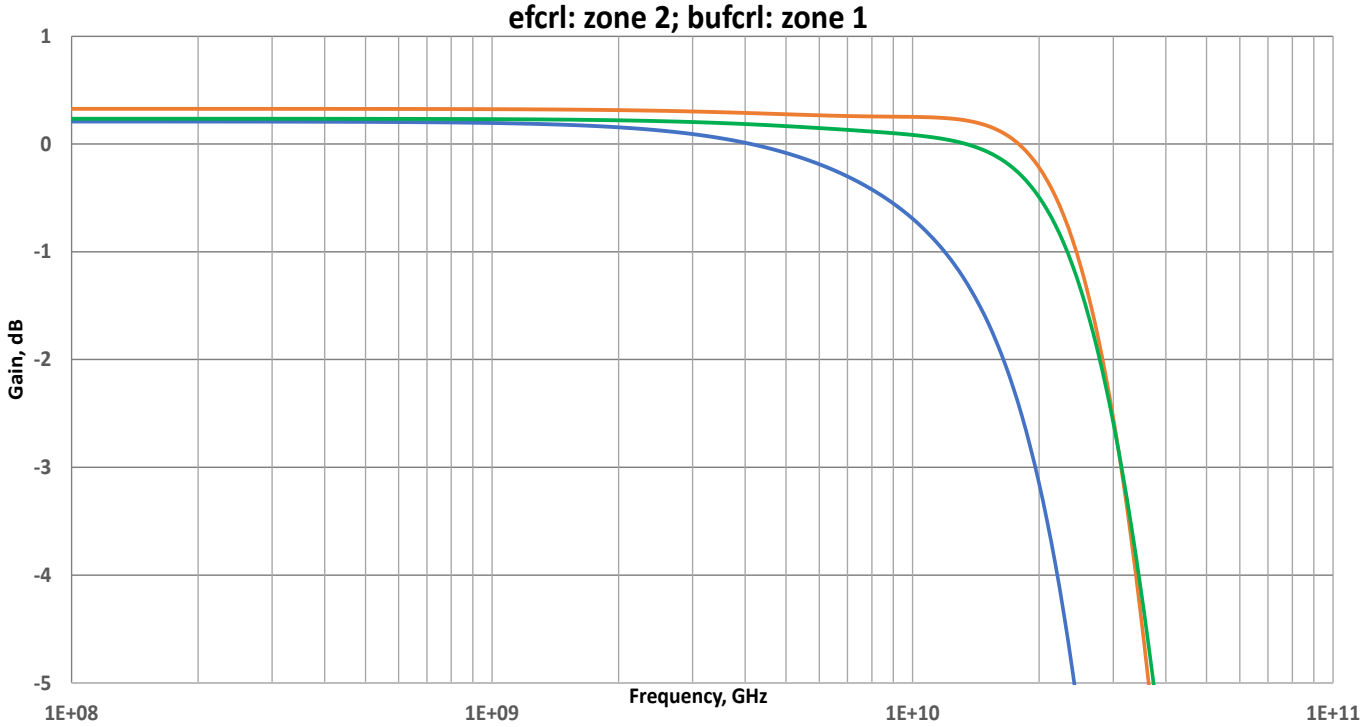

Fig. 6. Frequency Response. efcrl=+3V/+3.2V/+3.5V, bufcrl=+2.3V

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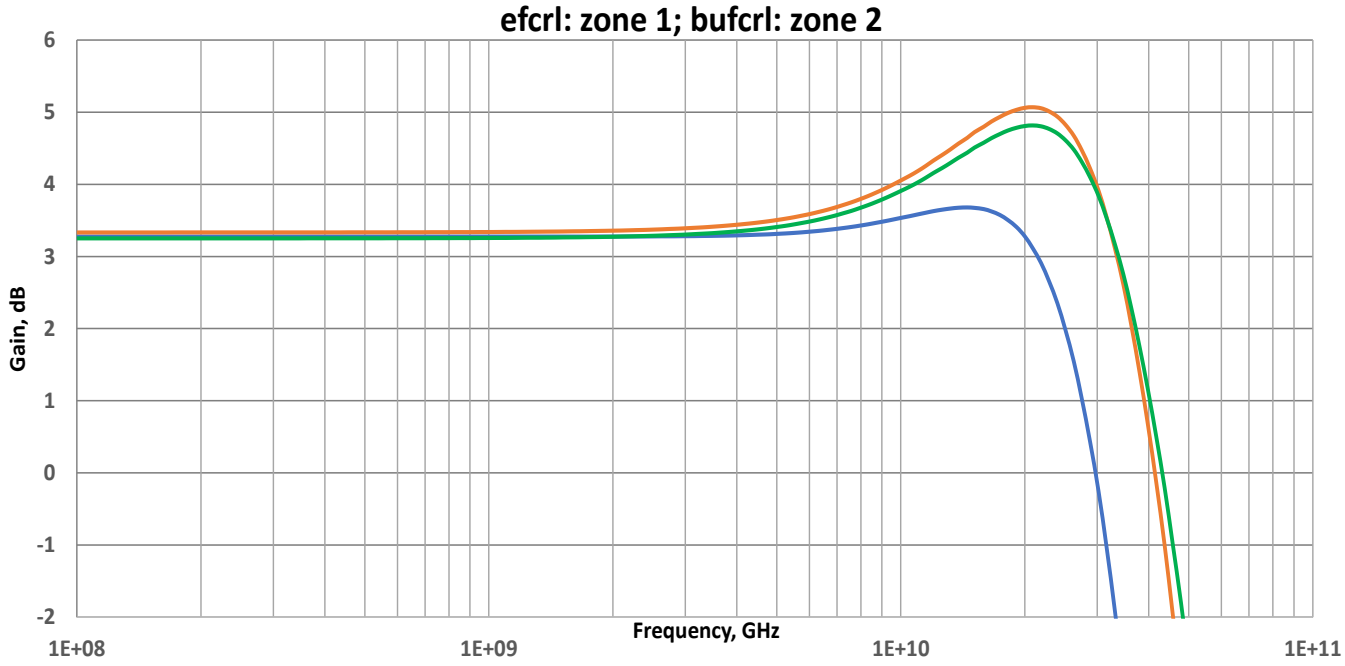

Fig. 7. Frequency Response. efcrl=+2.1V/+2.3V/+2.5V, bufcrl=+3.2V

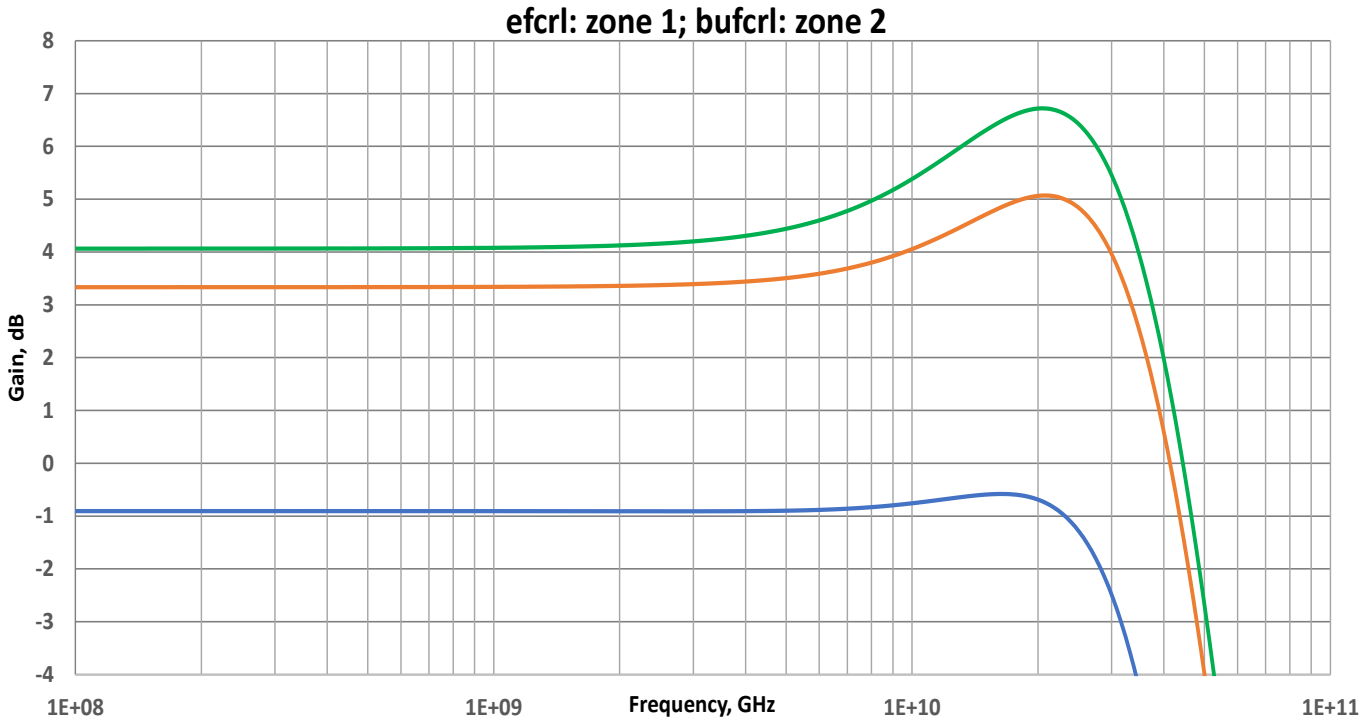

Fig. 8. Frequency Response. efcrl=+2.3V, bufcrl=+3V/+3.2V/+3.5V

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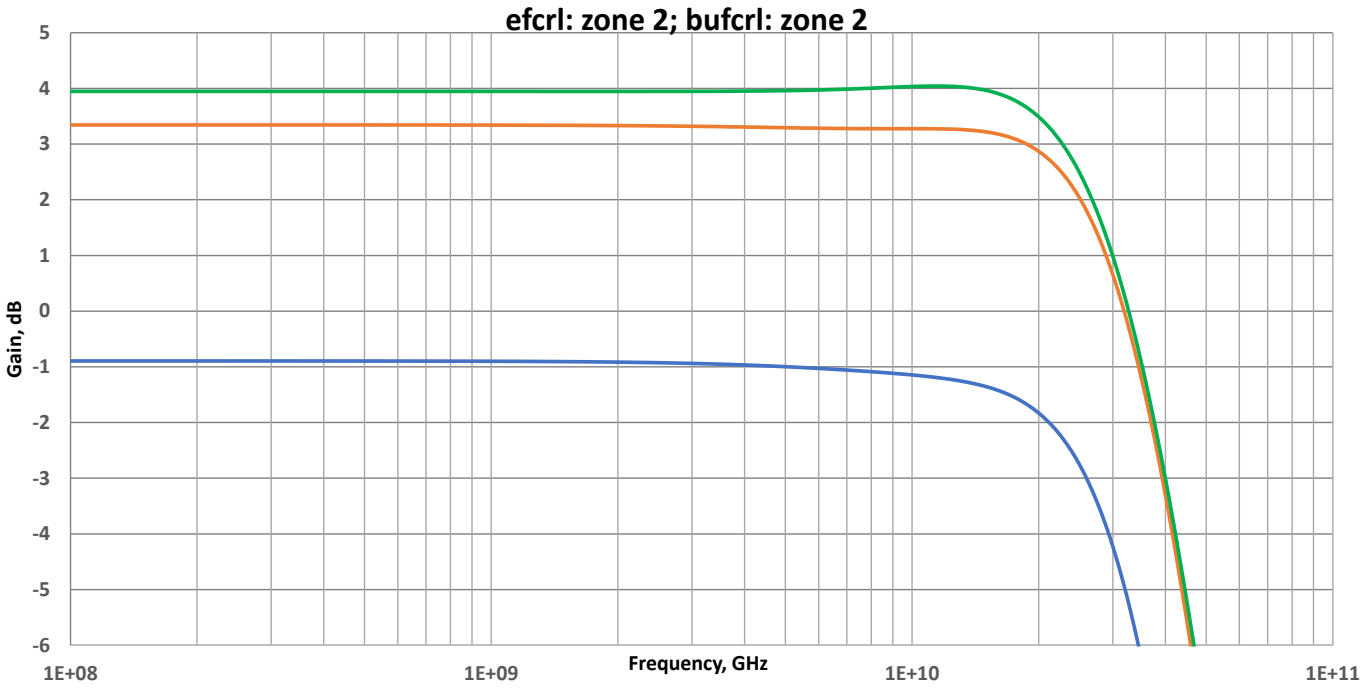

Fig. 9. Frequency Response. efcrl=+3.2V, bufcrl=+3V/+3.2V/+3.5V

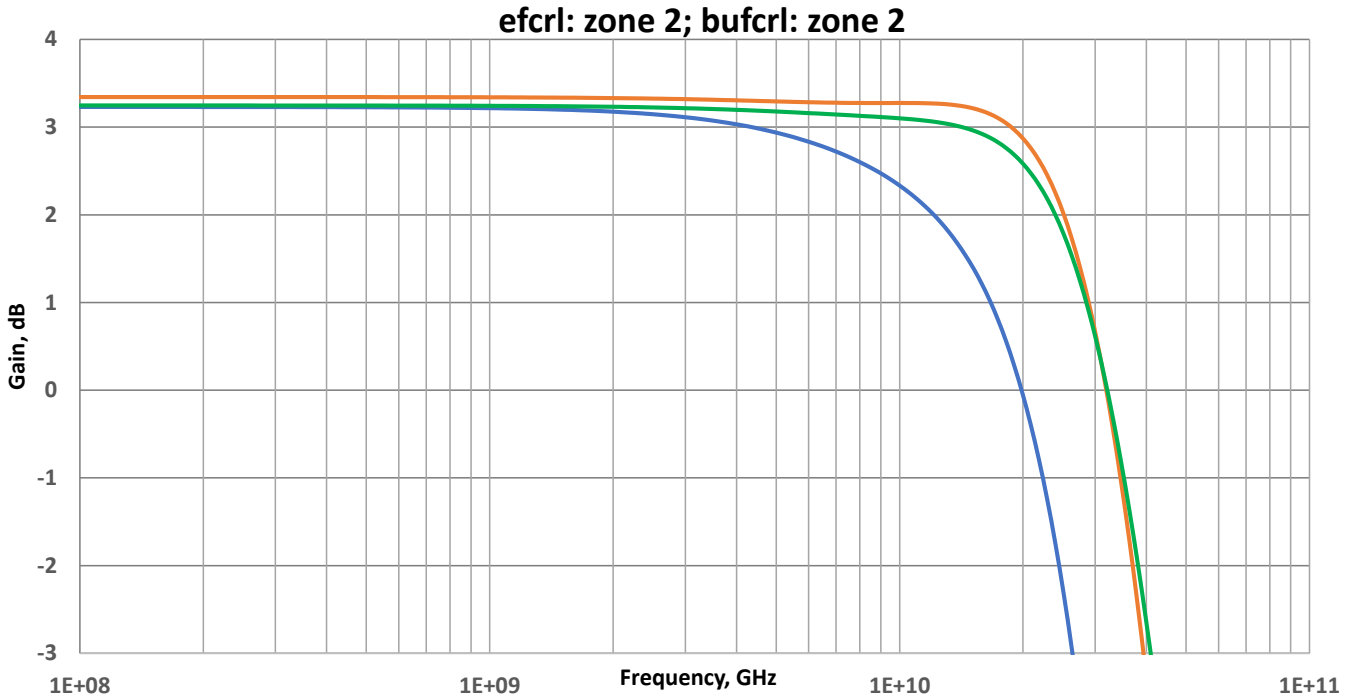

Fig. 10. Frequency Response. efcrl=+3V/+3.2V/+3.5V, bufcrl=+3.2V

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PAM4 SIGNAL EYE PROPAGATION

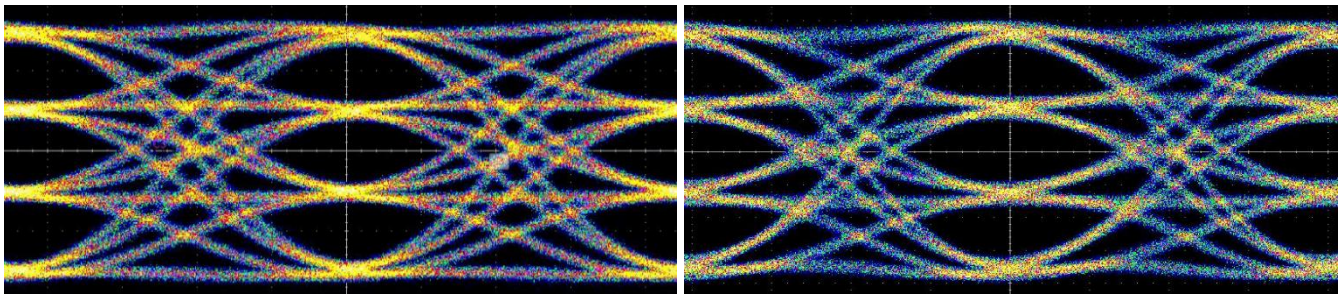

Fig.5. PAM4 at 25Gbaud, 800mV Differential Peak-Peak, Left: Input, Right: Output

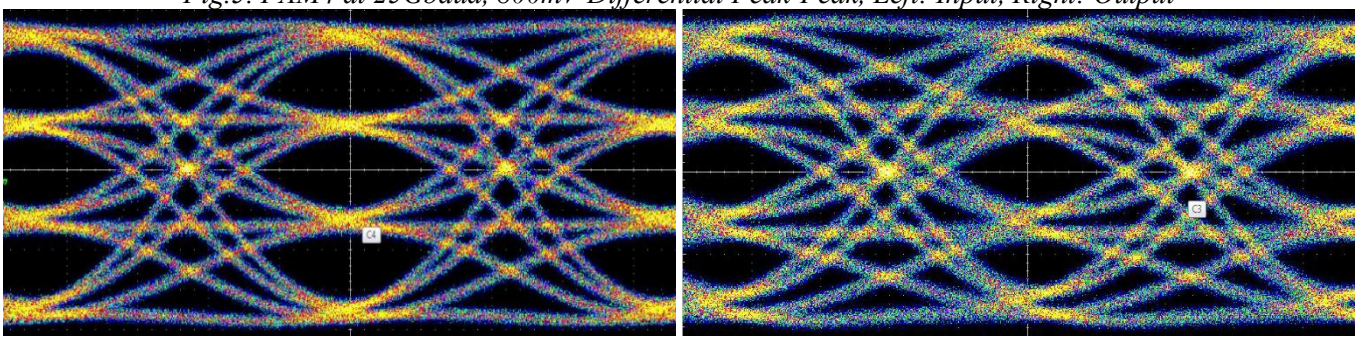

Fig.6. PAM4 at 32Gbaud, 800mV Differential Peak-Peak, Left: Input, Right: Output

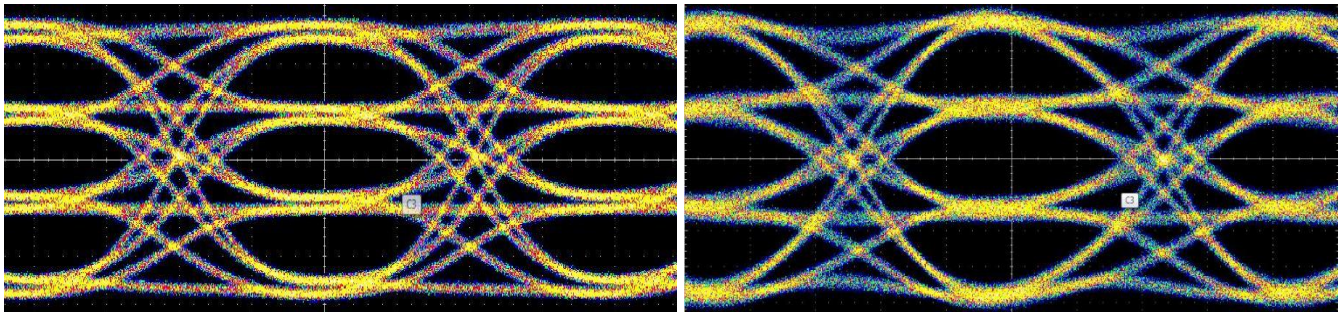

Fig.7. PAM4 at 25Gbaud, 1200mV Differential Peak-Peak, Left: Input, Right: Output

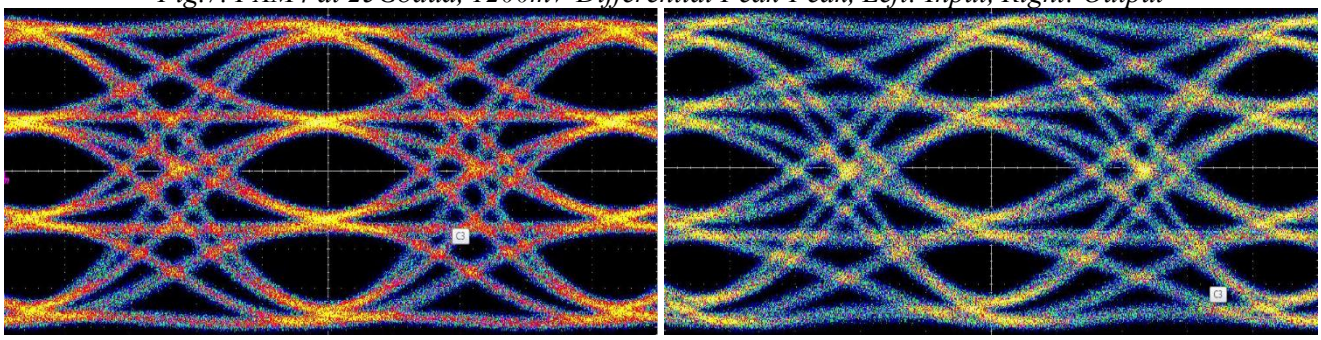

Fig.8. PAM4 at 32Gbaud, 1200mV Differential Peak-Peak, Left: Input, Right: Output

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.9	*V*
Power supply current		350	*mA*
Input Voltage	vcc-1.0	vcc+0.4	*V*
RF Input Voltage Swing (SE)		0.8	*V*
Analog control voltages	vee	vcc	*V*
Storage Temperature	-40	+100	*°C*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTION

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
dp	21	CML input	Differential high-speed data inputs with an internal SE 50*Ohm* termination to vcc
dn	23		
q1p	17	CML output	Differential high-speed data outputs with an internal SE 50*Ohm* termination to vcc. Requires an external SE 50*Ohm* termination to vcc
q1n	15		
q2p	11	CML output	
q2n	9		
q3p	5	CML output	
q3n	3		
efcrl	7	Analog Control	Dual zone analog current/binary peaking control with an internal 8.5*KOhm* termination to vcc and 91.8*KOhm* termination to vee.
bufcrl	19		Dual zone analog current/binary gain control with an internal 8.5*KOhm* termination to vcc and 91.8*KOhm* termination to vee.

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.6*V* or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.6*V*)	1, 13

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.2	-3.6	-3.8	*V*	-12%, +6%
vcc		0.0		*V*	External ground
*I*vee	100	280	330	*mA*	At max. control range
Power consumption	320	1000	1250	*mW*	At max. control range
Junction temperature	-25	50	125	*°C*	
Input Analog (dp/dn)					
Bandwidth	DC		33	*GHz*	-3*dB*
Common mode voltage level		vcc		*V*	Internally generated
Single-ended voltage swing, pk-pk; unused input not connected or AC terminated		600		*mV*	THD < 0.8% at 2*GHz*
		600		*mV*	THD < 0.4% at 5*GHz*
		600		*mV*	THD < 1.1% at 10*GHz*
Single-ended voltage swing, pk-pk; unused input not connected or AC terminated		1.2		*V*	THD < 4% at 2*GHz*
		1.2		*V*	THD < 2.3% at 5*GHz*
		1.2		*V*	THD < 3.6% at 10*GHz*
Input Noise Density		TBD		*nV*/sqrt*(Hz)*	
S11		TBD		*dB*	at 3*GHz*
		TBD		*dB*	at 10*GHz*
		TBD		*dB*	at 20*GHz*
		TBD		*dB*	at 25*GHz*
Output Analog (q1p/q1n, q2p/q2n, q3p/q3n)					
Common mode level		vcc-0.6		*V*	With an external 50*Ohm* DC termination
Small signal differential gain	0		+3	*dB*	up to 30*GHz*
Gain variation with optimal peaking control settings		±0.5		*dB*	up to 30*GHz*
Output referred 1*dB* Compression Point		>6		*dBm*	Single-Ended, 10*GHz*

PARAMETER	MIN	TYP	MAX	UNIT	ZONE CONTROL	COMMENTS
EF Current Control Signal (efcrl)						
Control range, **zone 1**	+2.1	+2.3	+2.5	*V*	Maximum peaking, +4dB	from vee, ±3.6*V* supply
Control range, **zone 2**	+3	+3.2	+3.5		Default peaking	
Current adjustment	170	220	270	*mA*		
BUF Current Control Signal (bufcrl)						
Control range, **zone 1**	+2.1	+2.3	+2.5	*V*	Default gain, 0dB	from vee, ±3.6*V* supply
Control range, **zone 2**	+3	+3.2	+3.5		Maximum gain, +3dB	
Current adjustment	150	220	270	*mA*		

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Die INFORMATION

The square die has dimensions of 1.93*mm*X1.93*mm*. It includes 24 Cu Pillar bumps as shown in Fig. 1. Fig. 1a shows the pad frame view from the top side of the chip. Fig. 1b (e.g. a horizontally flipped version of the Fig. 1a view) shows the chip mounting footprint that is required for its attachment to any type of PCB.

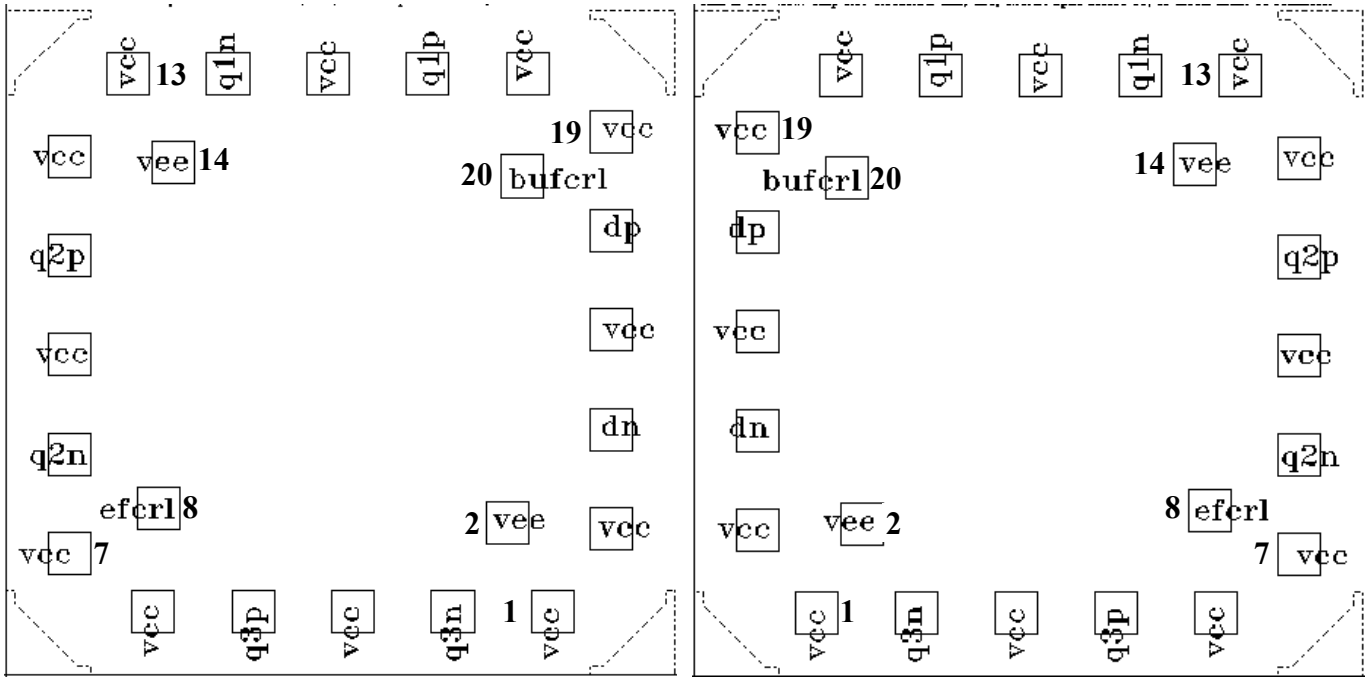

Fig. 1. Pad Frame View From Top (a) and Chip Mounting Footprint (b)

The mounting footprint pad coordinates in relation to the chip's bottom-left corner are shown in Table 2. Here. the Pink pads (DC) represent DC signals, the Red pads (HS) represent high-speed connections that require a 50*Ohm* environment, and the Green pads (vcc) represent the positive power supply in the chip.

Table 2. Pad Coordinates for the Chip Mounting Footprint

Pad #	X, um	Y, um	Pad #	X, um	Y, um	Pad #	X, um	Y, um	Pad #	X, um	Y, um
1	245	128	7	1212	245	13	1095	1212	19	128	1095
2	335	307	8	1033	335	14	1005	1033	20	307	1005
3	445	128	9	1212	445	15	895	1212	21	128	895
4	645	128	10	1212	645	16	695	1212	22	128	695
5	845	128	11	1212	845	17	495	1212	23	128	495
6	1045	128	12	1212	1045	18	295	1212	24	128	295

The chip aluminum pads are octagonal with dimensions of 90*um*X90*um* and octagonal pad opening of 47*um*X47*um*. The Cu pillars formed on the pads are round with a UBM diameter of 80*um* and the final pillar height of 65*um*. The bump stack and solder alloy are: Cu 37*um*, Ni 3*um*, Sn1:8Ag-cap 25*um*.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances

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in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.1.2	05-2026	Changed name from BD to DIE and minor edits to wording
1.0.2	05-2026	First release
0.0.1	02-2025	Preliminary release