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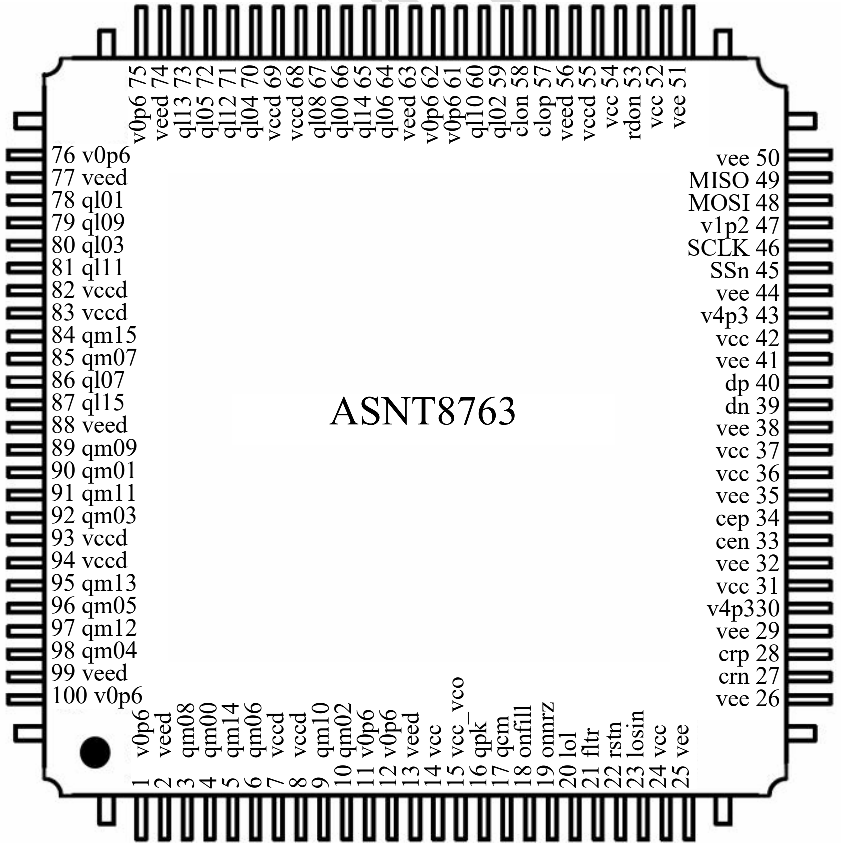
ASNT8763-KMT

PAM3 or NRZ CDR with Adaptive DFE

- High-speed CDR for NRZ or PAM3 signals
- Optional high-speed external clock mode with disabled clock recovery
- On-chip adaptive 3-tap DFE
- Selectable automatic or manual DFE control
- Fully differential CML-type analog input data interface
- Fully differential CML high-speed input clock interface
- Pseudo-differential SSTL interfaces for low-speed clock and data outputs
- LVDS interface for reference clock input
- High-speed CMOS 3-wire interface for manual chip control
- Four power supplies (two for analog and two for digital chip sections) and a termination voltage
- Average power consumption: 4.0*W*
- Die size 2.4x2.4*mm*^{2}
- Custom CQFP 100-pin package



DESCRIPTION

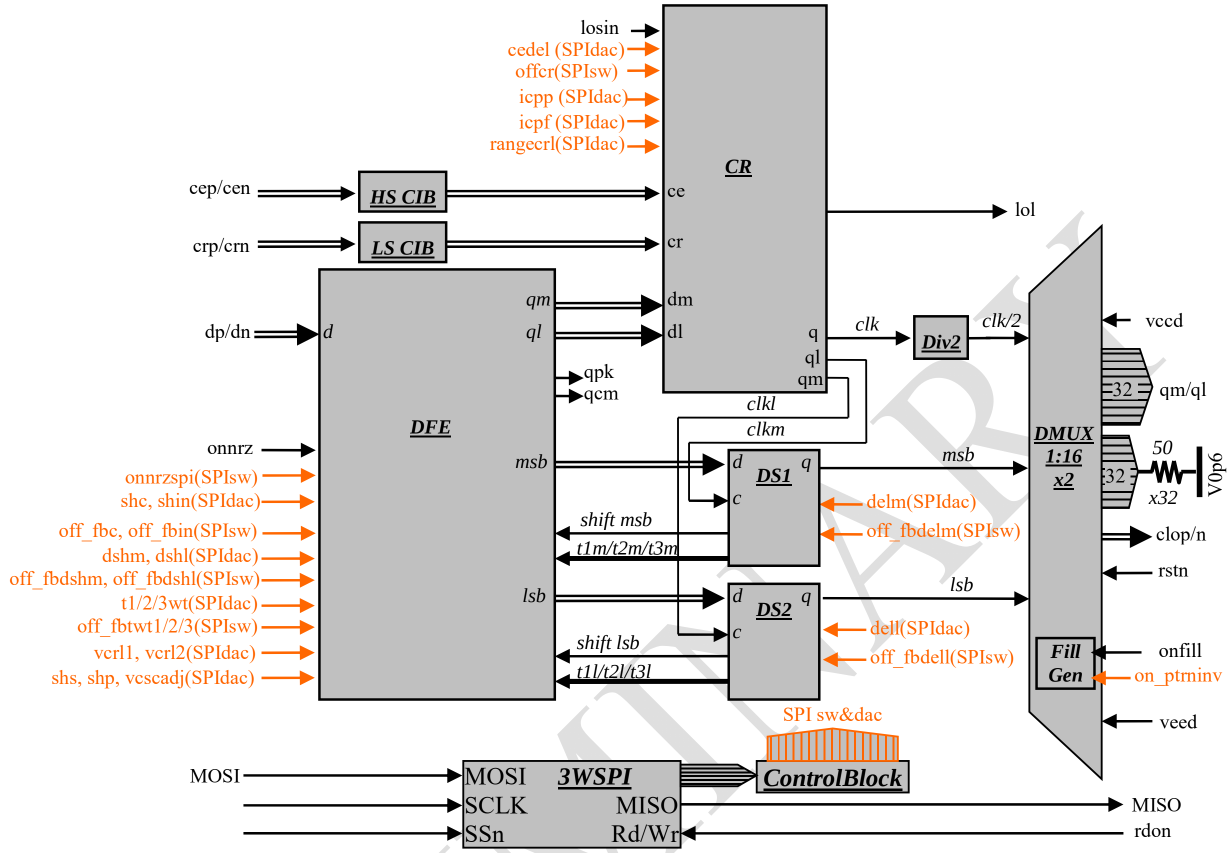


Fig. 1. Functional Block Diagram

The IC shown in Fig. 1 is an adjustable clock and data recovery (CDR) system for either NRZ or PAM3 signals. Its operational modes are controlled through the on-chip 3-wire SPI and/or through external ports. The onnrz control (external analog port or SPI byte combined through 2-input logic OR function) must be set in accordance with the input signal type. An internal DFE is designed for optimal data reconstruction of the differential input signal dp/dn as well as for automatic conversion of the input signal into two pairs of binary signals that represent transitions either in the top (MSB) or the bottom (LSB) portions of the PAM3 signal.

The first two of the binary output signals of DFE go to the Clock Recovery (CR) block. CR can either let an external clock signal from the input cep/cen through or use the two NRZ data signals from DFE along with the reference clock input signal crp/crn to generate a recovered clock signal which is phase-locked to input data.

The other two output data signals from DFE are delivered to two identical Data Sample blocks (DS1 and DS2). DS1 reconstructs the MSB portion of the PAM3 signal by latching it with the clock signal provided by CR. Similarly, DS2 reconstructs the LSB portion of the PAM3 signal by latching it with the clock signal provided by CR. DS1 and DS2 also provide data shift feedback controls, tap weight feedback controls, and tap signals for DFE. Six tap signals are fed back to DFE to optimally shape its output signals. The tap weights and polarities are automatically set by three independent feedback loops.

The reconstructed data streams from DS1 and DS2 are demultiplexed by a dual demultiplexer 1-to-16 (DMX1:16x2) block and delivered to the output SSTL interface as single-ended signals qm00-qm15 and ql00-ql15 together with the corresponding low-speed differential SSTL clock clop/clon. The real data can be replaced by a pre-defined bit pattern generated inside the block.

Most operational modes of the chip are controlled by the Control Block that communicates with an external computer through a high-speed 3-wire serial interface (3wSPI). The SPI is activated by active-low chip enable signal (SSn).The SPI can be forced by the active-low external signal rdon to read its internal registers without re-writing them. The SPI supply voltage can be controlled or adjusted through the v1p2 pin.

The part operates with a positive supply vcc = +3.3*V* for the main data paths and a positive supply vcc_vco = +3.3*V* for VCO, and additional positive supplies v4p3 = +4.3*V* for DFE. A separate positive supply vccd=+1.2*V* is provided for the internal output CMOS circuitry. The additional termination supply v0p6=+0.6*V* with a bi-directional current is required for the output interface operation. The negative supply rails vee and veed should be both connected to external ground.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process either differential or single-ended external CML clock signal cep/cen. In the single-ended mode, the clock is applied to one of the pins together with a threshold voltage applied to the unused pin. The buffer utilizes on-chip single-ended termination of 50*Ohm* to vcc for each input line. When CR is in external clock mode (SPI bit offcr = “High”), the external clock phase can be adjusted through the control cedel. Fig. 2 presents the dependence of CIB latency on the control cedel.

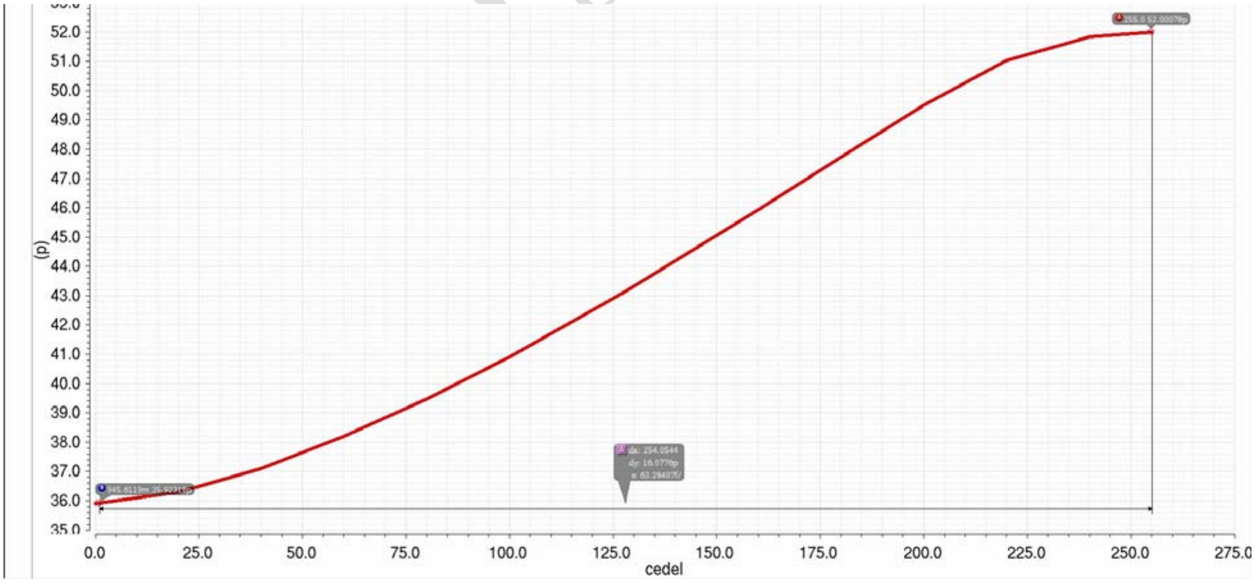


Fig. 2. CIB Latency Vs cedel

LS CIB

The Low-Speed Clock Input Buffer (LS CIB) is a proprietary universal input buffer (UIB) that operates in LVDS mode. Its differential input crp/crn has differential input impedance of 100 *Ohms*. The purpose of the buffer is to deliver low-speed reference clock of 1/32 rate of high-speed clock to the frequency loop of CR.

DFE

The main purpose of DFE is to optimally shape the input data signal eye and to form two NRZ data streams out of the top part of the input PAM3 signal (MSB) and two NRZ data streams out of the bottom part of the input PAM3 signal (LSB). Fig. 3 presents the block diagram of DFE.

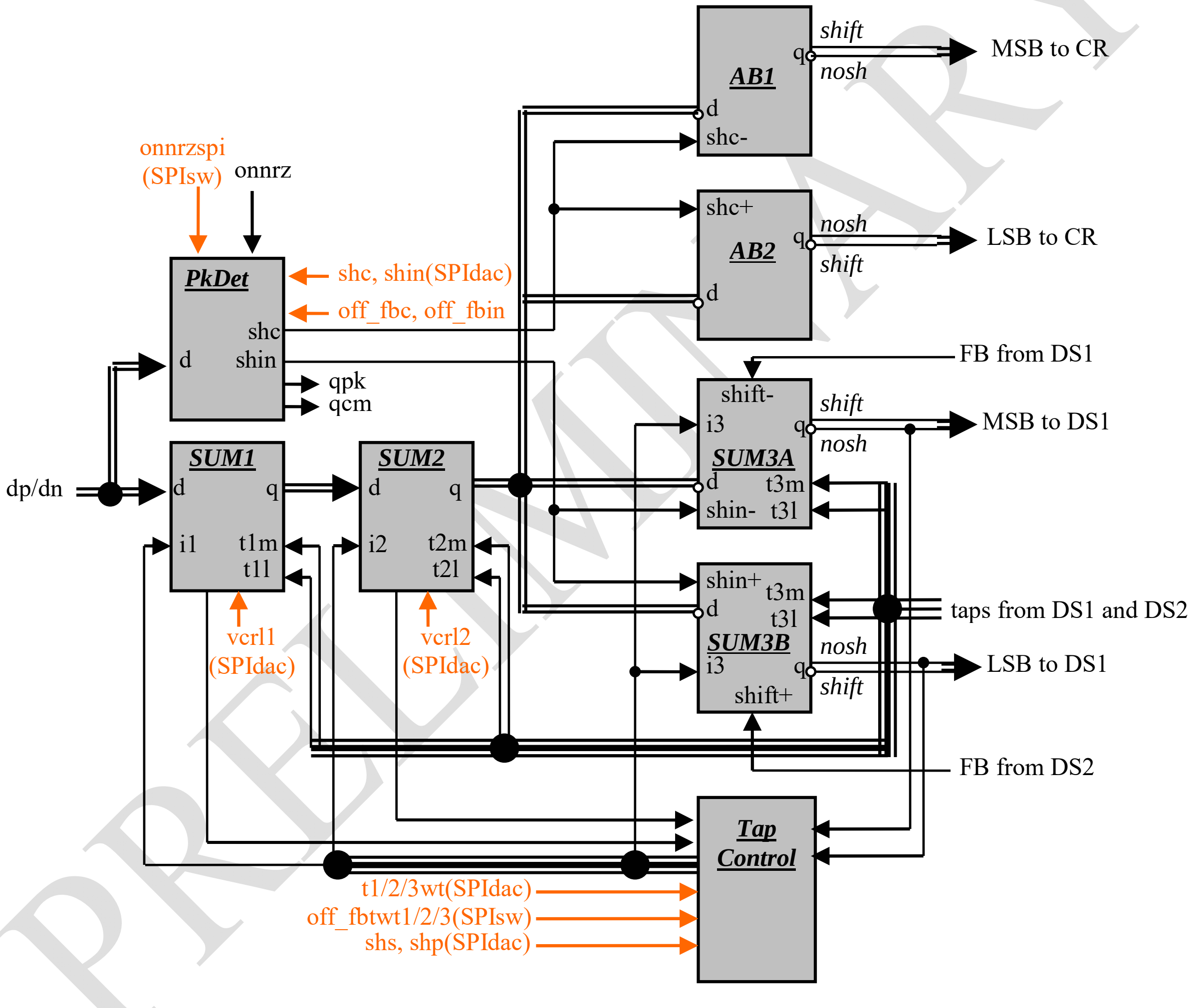


Fig. 3. DFE Functional Block Diagram

The differential analog input signal dp/dn goes to the first DFE summation block (SUM1). In SUM1 the differential digital signals t1m and t1l from latching DFFs of DS1 and DS2 are injected into the analog signal with a certain weight and polarity determined by one of the feedback loops in order to achieve optimal eye reconstruction. The resulting signal goes to the second DFE summation block (SUM2) where the differential feedback signals t2m and t2l with their own weight and polarity are injected into it.

The resulting signal is then split into four paths and is delivered to two summation blocks (SUM3A and SUM3B) and two analog buffers (AB1 and AB2) in parallel. In SUM3A and SUM3B the signal is subjected to the similar reconstruction process as in the previous blocks with the help of differential signals t3m and t3l.

Weights and polarities of injected signals are determined by three separate feedback loops. The speed of the first loop is the highest out of the three, and the speed of the third loop is the lowest. The tap weights are determined by comparing the signal to the perfect square wave.

In the manual mode (when the SPI bits off_fbtwt<1>/<2>/<3> are "High"), the weight of the injected signals into SUM1, SUM2, and SUM3A/B can be individually adjusted with the SPI bytes t1wt, t2wt, and t3wt respectively. Fig. 4 presents the simulated dependence of weights of direct and inverted tap signals on control codes t1wt/t2wt/t3wt. The red curve is the weight of the direct taps, and the blue curve is the weight of the inverted taps.

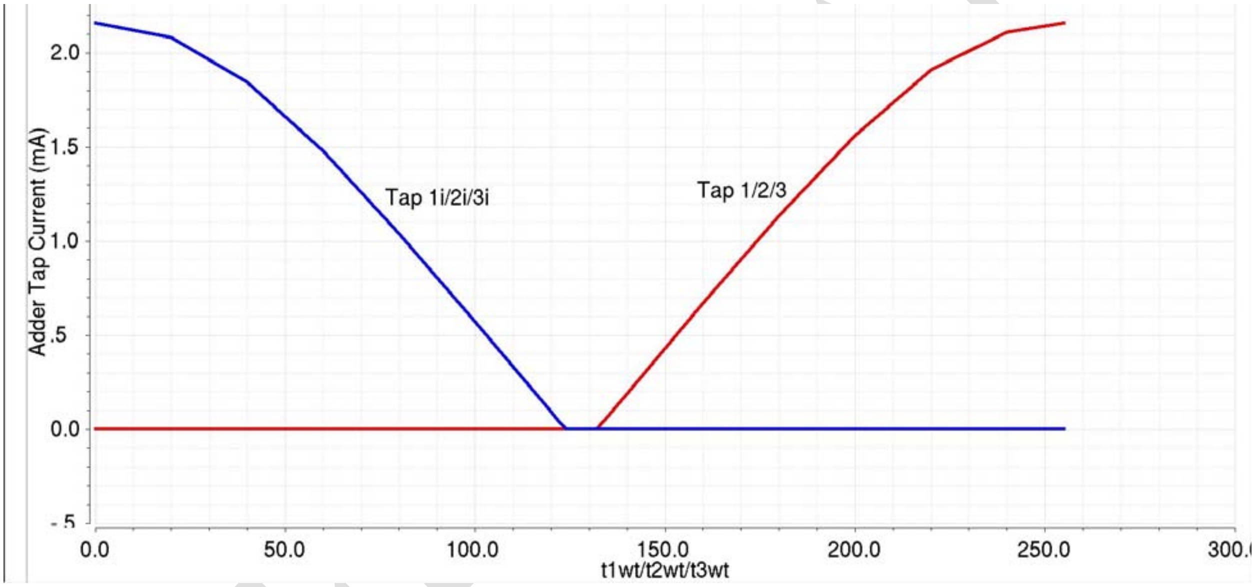


Fig. 4. Tap Weight Vs. Control t1wt/t2wt/t3wt

Each summation block has additional current sources that automatically keep total currents through their loads constant in order to stabilize their output common modes.

SUM3A, SUM3B, AB1, and AB2 have an additional ability to shift one of its differential outputs down. SUM3A and AB1 shift their direct output signals down in order to ensure correct sampling of the top (MSB) portion of the eye of the PAM3 input signal. SUM3B and AB2 shift their inverted output signals down in order to ensure correct sampling of the bottom portion (LSB) of the eye. A voltage shift in a buffer is produced by connecting an adjustable DC current source to one of the outputs of a differential buffer. The voltage drop on the output load due to the resulting current results in the output common mode voltage shift in that buffer.

AB1 and AB2 outputs are converted to NRZ data streams by limiting buffers in order to obtain signals that represent transitions in the top and the bottom portions of the PAM3 signal. The resulting signals are delivered to CR. The SPI bit off_fbshc can be used to switch shift control of AB1 and AB2 between automatic and manual modes of operation.

In the automatic mode (off_fbshc = “Low”), shifting currents of AB1 and AB2 are derived automatically by the input peak detector (PkDet). Shifts of output common mode voltages of AB1 and AB2 are the same in magnitude, but opposite in polarity. The common mode voltage of AB1 is shifted halfway between the middle and the top levels of PAM3 signal in order to retrieve MSB transitions of the signal. The common mode voltage of AB2 is shifted halfway between the middle and the bottom levels of PAM3 signal in order to retrieve LSB transitions. In the manual mode (off_fbshc = “High”), shifting voltages of AB1 and AB2 are set by the SPI byte shc. Fig. 5 presents the simulated dependence of differential common mode voltages of AB1 and AB2 on the control shc.

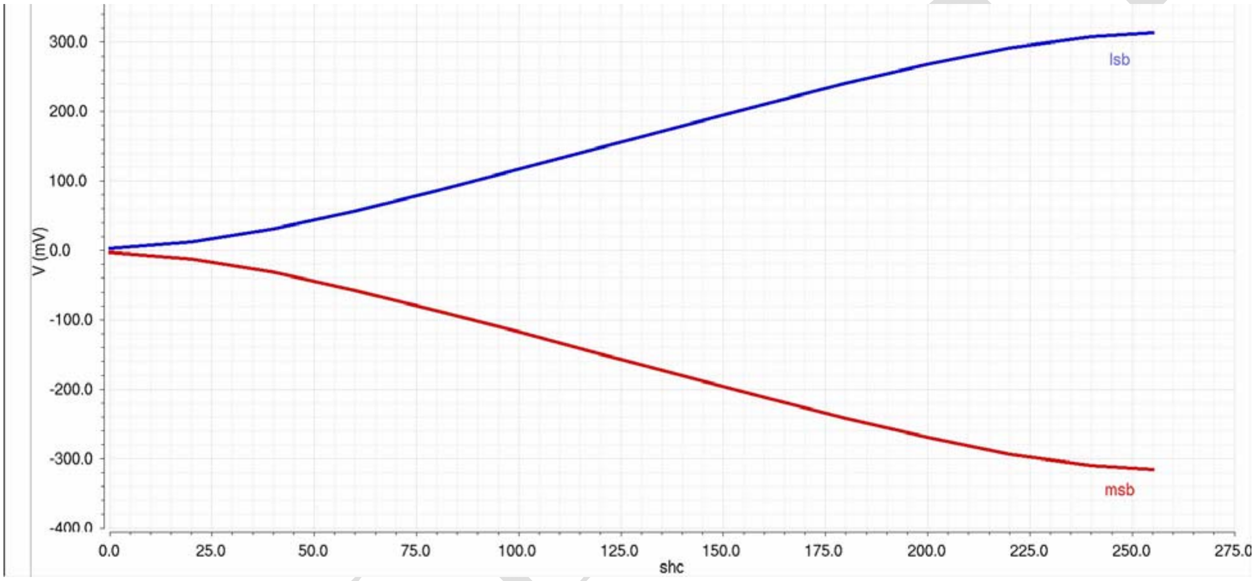


Fig. 5. Differential Output Common Mode of AB1 and AB2 Vs. shc

Shifting processes of output common mode voltages of SUM3A and SUM3B are similar to shift processes in AB1 and AB2, but are more complex. A shifting current source of SUM3A/B consists out of two parts. Current of the first part is the same for SUM3A and SUM3B in magnitude and can be set either manually or automatically by PkDet output. The SPI bit off_fbshin can be used to switch shift control of this current between automatic and manual modes of operation. This current is needed to provide a small initial voltage shift of SUM3A and SUM3B that is used as a starting point by feedback loops to derive a more precise common mode voltage shift of SUM3A and SUM3B. The output of the peak detector can be monitored through output pins qpk and qcm. In automatic mode (off_fbshin = “Low”), PkDet measures amplitude of input data and sets the value of the initial shift automatically. In manual mode (off_fbshin = “High”), the SPI byte shin can be used set this current manually. Fig. 6 presents the dependence of the common mode voltage of SUM3A and SUM3B associated with initial shift on the control shin.

The second part of the shifting current source of SUM3A/B is needed to set the common mode voltage to the middle of the eye opening with high precision in order to maximize latching accuracy. Switching of shift control between automatic and manual modes of operation can be performed by the SPI bit off_fbshm for SUM3A and the SPI bit off_fbdshl for SUM3B. In the automatic mode (off_fbdshm/l = “Low”), two separate feedback loops control common mode shifts of SUM3A and SUM3B independently. DS1 provides controls for the SUM3A feedback loop, and DS2 provides controls for the SUM3B feedback loop. As a result, the differential output common mode voltage of SUM3A settles to the middle of the MSB eye opening of the PAM3 signal, and the differential output common mode voltage of SUM3B settles to the middle of the LSB eye opening. In the manual mode (off_fbdshm/l = “High”), SPI bytes dshm and dshl can be used to manually adjust output common mode voltages of SUM3A and SUM3B.

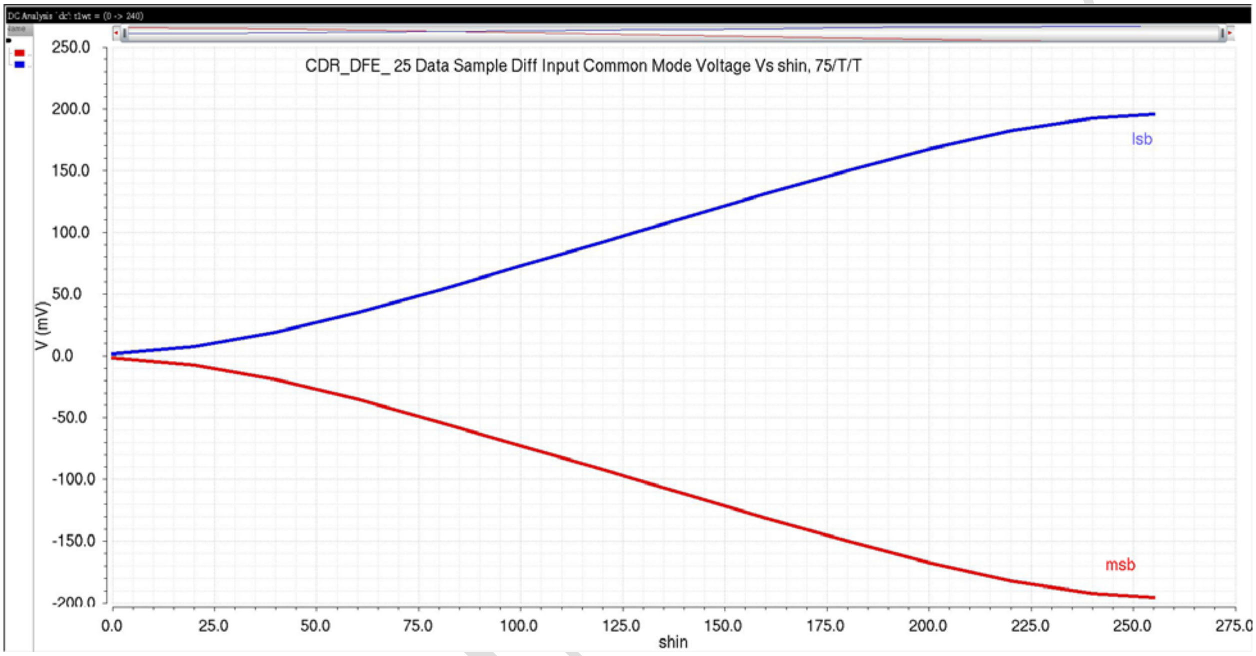


Fig. 6. Differential Common Mode Voltage of SUM3A and SUM3B Vs. Control shin

Fig. 7 presents the simulated dependence of differential common mode voltage of SUM3A on the control dshm for three values of shin in manual mode.

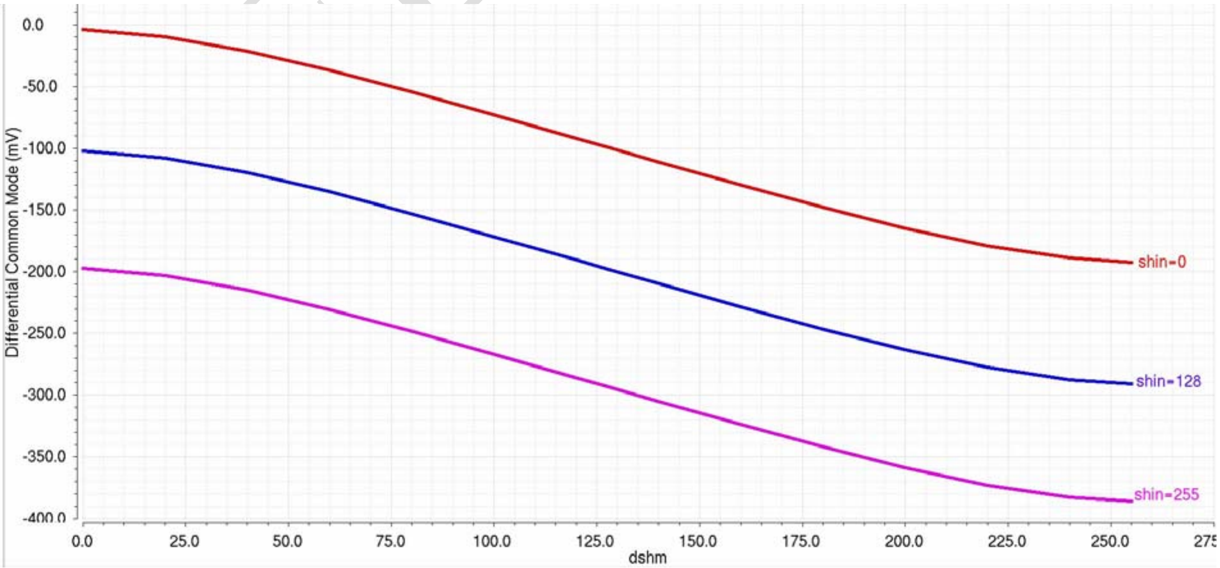


Fig. 7. Differential Common Mode Voltage of SUM3A Vs. Control dshm

Fig. 8 presents the simulated dependence of differential common mode voltage of SUM3B on the control dshl for three values of shin in manual mode.

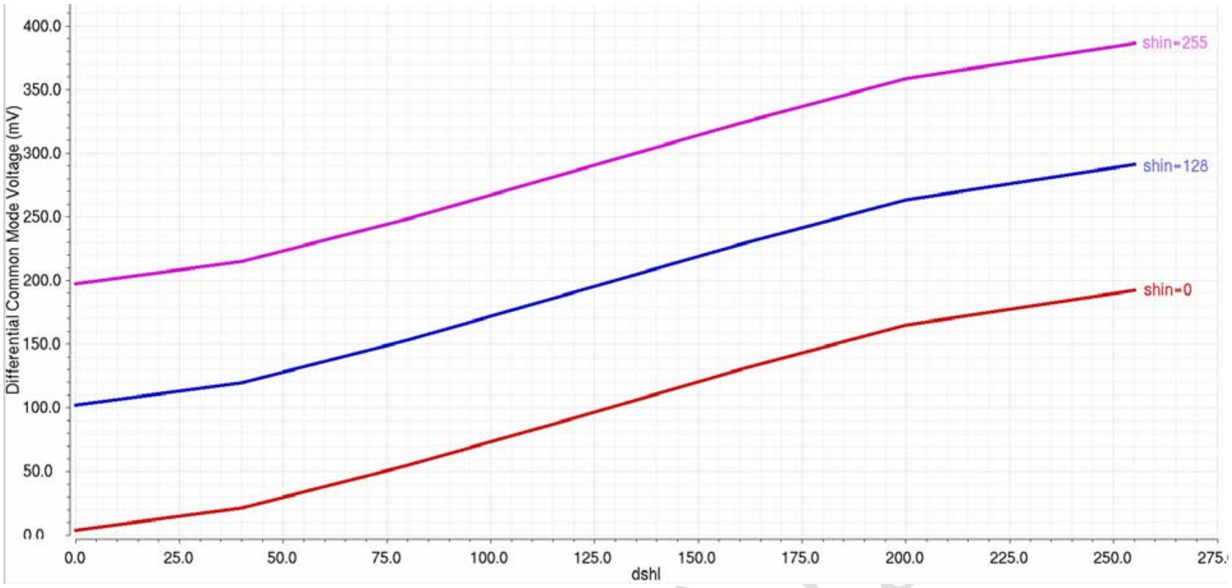


Fig. 8. Differential Common Mode Voltage of SUM3B Vs. Control dshl

In NRZ mode (when at least one of the onnrz or onnrzspi controls is "High"), all the vertical data shifts turn off and are not affected by feedback loops or manual adjustments. Outputs of SUM3A, SUM3B, AB1, and AB2 become identical signals without any common mode shifts.

The SPI byte vcscadj can be used to adjust internal cascode DC voltage of all summation blocks and analog buffers of DFE simultaneously in order to achieve optimal DC biasing conditions. It should be set to its default value during normal operation. Fig. 9 presents the simulated dependence of cascode voltage on the control vcscadj.

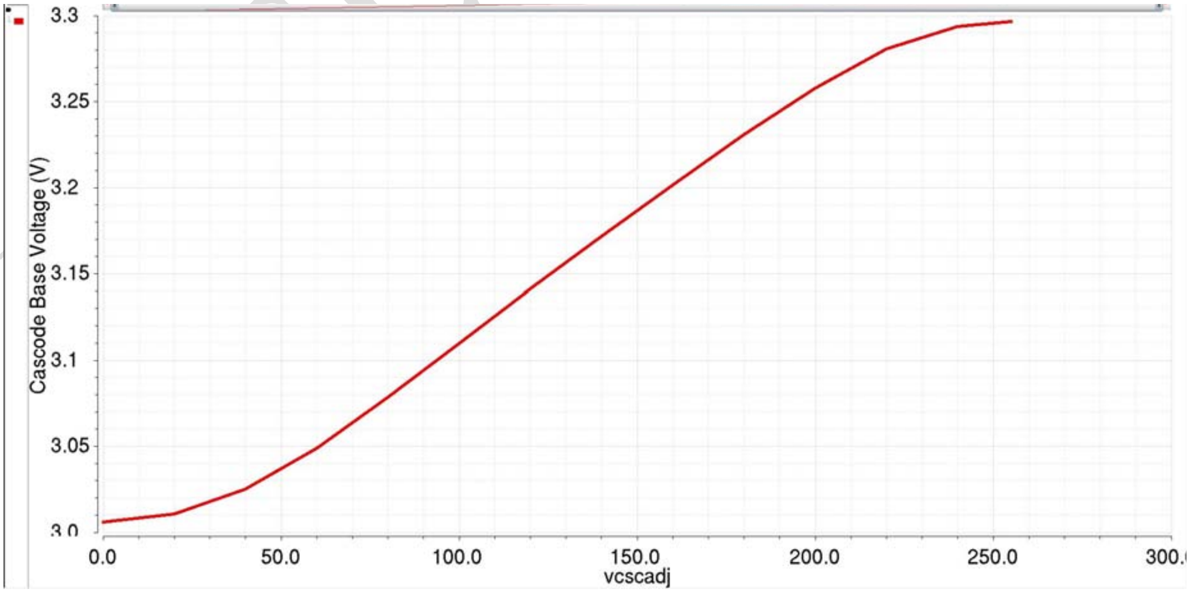


Fig. 9. Cascode Voltage Vs. Control vcscadj

The SPI bytes shs and shp determine the strength of temperature and process corner compensation circuitry that is needed to tune tap weight loops. The adaptation circuitry automatically adapts to different conditions. These controls should be kept at their default values for normal operation.

The DFE uses peaking equalization in order to eliminate losses caused by the package and input transmission lines. Peaking of SUM1 can be adjusted through the SPI byte vcrl1. Peaking of SUM2 can be adjusted through the SPI byte vcrl2. Fig. 10 presents the simulated dependence of the reverse bias voltage of varactors in SUM1/2 on the control vcrl1/2.

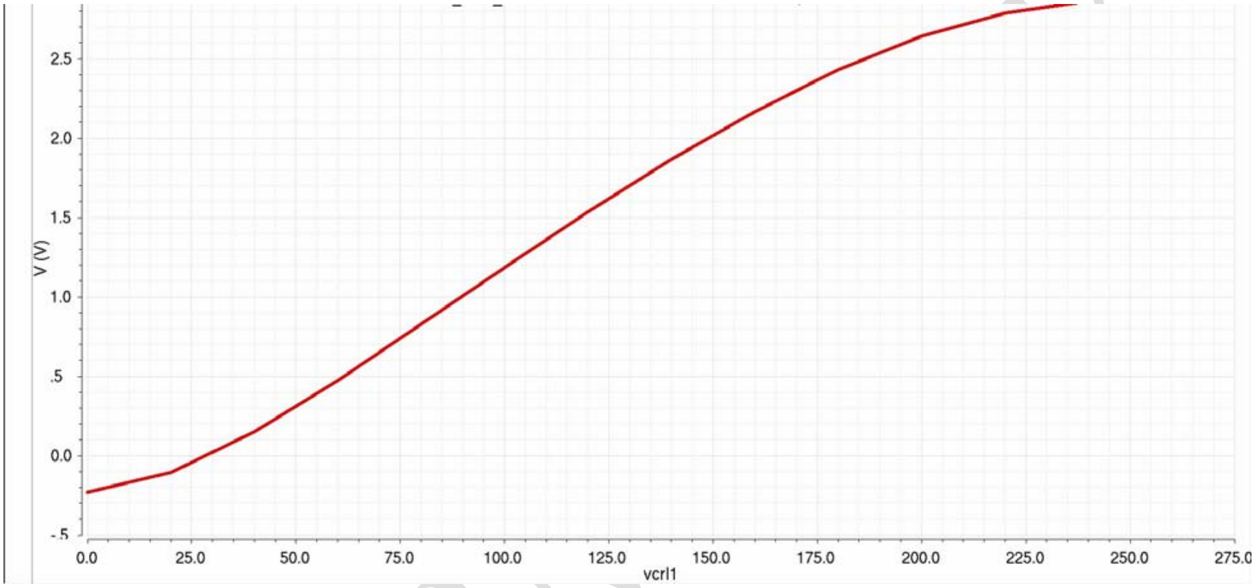


Fig. 10. Varactor Reverse Bias Voltage in SUM1/2 Vs vcrl1/2

CR

The Clock Recovery block (CR) includes a high-speed VCO (voltage-controlled oscillator), a charge pump, a dual phase detector, and a frequency detector. The dual phase detector consists out of two identical phase detectors which are connected in parallel. The frequency loop works in concert with low-speed clock crp/crn. The dual phase detector of the phase loop utilizes transition data from both MSB and LSB portions of the input PAM3 signal for more reliable locking. Data transitions in the MSB portion of the PAM3 input signal are acquired by putting the outputs of AB1 through a limiting buffer. Data transitions in the LSB portion of the PAM3 input signal are acquired by putting the output of AB2 through a limiting buffer. The logic OR function combines the two signals into a single set of “up/down” charge pump signals. The CR requires a single off-chip filter shown in Fig. 11 to be connected to pin fltr.

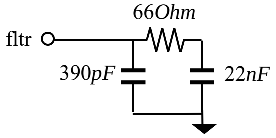


Fig. 11. External Loop Filter

The main function of the CR is to frequency-lock the on-chip VCO to the input data signal. By default, the CR aligns the recovered clock's working edge in the middle of the incoming data bits. Clock phase in each DS is independently fine-tuned by their feedback loops for optimum latching. The clock signal provided by CR is divided down in frequency by two (C2) and is utilized by DMX block for demultiplexation of the recovered data.

To help with VCO locking, its DC control signal after the filter can be shifted down by a certain voltage controlled by the SPI byte rangecrl.

The high-speed clock signal can be generated by internal VCO or routed from outside through the input cep/cen. By utilizing the SPI bit offcr, the desired mode of operation of the CR can be selected in accordance with Table 1 below.

Table 1. CR Mode Selection

offcr	**Mode of Operation**
"Low"	Internal VCO (CR)
"High"	External (cep/cen)

The dependence of VCO's frequency on the DC filter voltage (pin fltr) for typical and extreme conditions is shown in Fig. 12.

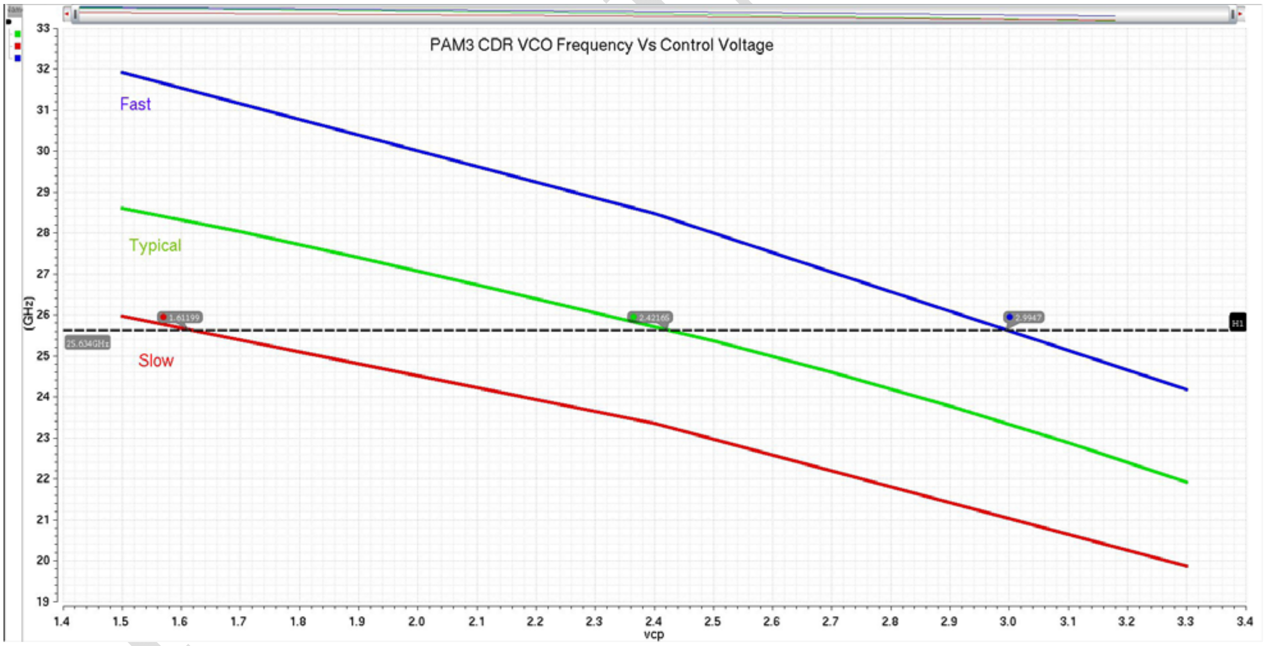


Fig. 12. VCO Frequency Vs. Filter Voltage

The phase and frequency loop gains can be adjusted by two SPI bytes icpp and icpf that adjust the charge pump currents. Fig. 13 presents the dependence of charge pump current on controls icpp and icpf when the other control is being held at its minimum (code "0").

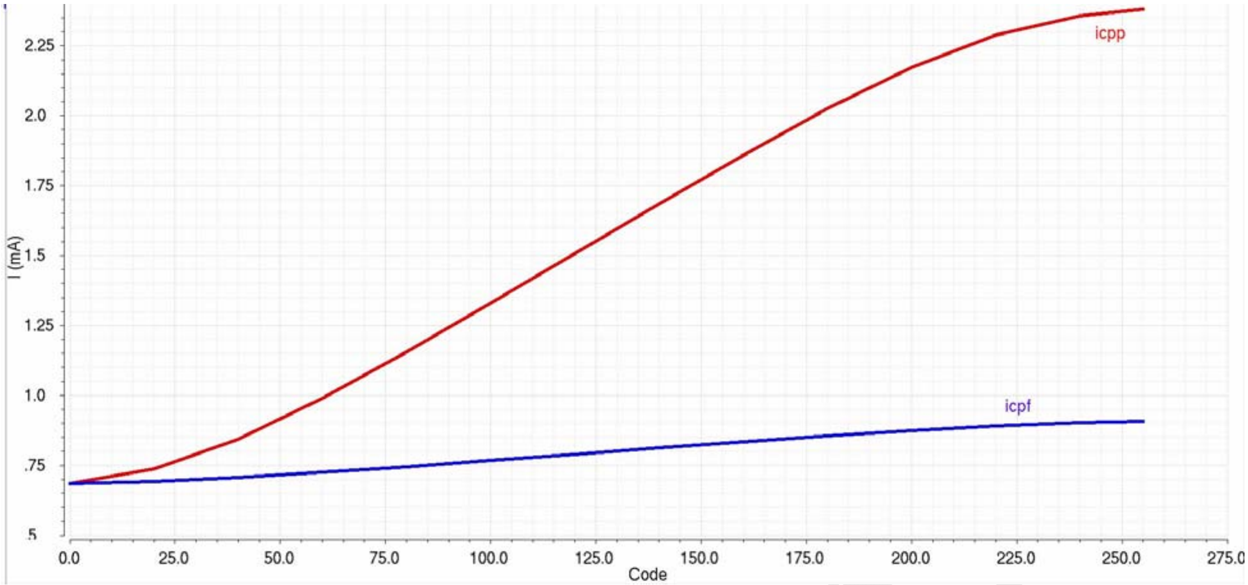


Fig. 13. Charge Pump Current Vs. icpp/icpf

The CMOS output lol can be used to detect the lock state of CR in Clock Recovery mode. “High” state signalizes the loss-of-lock, and the “Low” state signalizes normal operation. In case of absence of input data, the CMOS input pin losin can be used to turn the phase loop of clock recovery circuitry off in order to prevent clock recovery from locking onto input noise. If losin is “High”, the phase loop is turned off, the strength of the frequency loop increases, and the CR locks only to reference clock without phase alignment to data.

DS1 and DS2

The two NRZ data streams that are obtained by letting outputs of SUM3A and SUM3B through limiting buffers are delivered to the two separate Data Sample blocks (DS1 and DS2). DS1 processes the MSB data stream, and DS2 processes the LSB stream. The purpose of each DS is to correctly latch data for further demultiplexation, to produce tap signals, and to create error signals for voltage and clock phase shifting feedback loops.

The NRZ data input from DFE in each DS is split into three paths and delivered to three limiting buffers. Common modes of two of these buffers are shifted in opposite directions by feedback controls. The resulting signals are latched in parallel and are compared to the not shifted latched version of the input data. The comparison results are used in two internal local feedback loops to scan the top and the bottom limits of the eye opening. The third much slower feedback loop sets the shift of SUM3A or SUM3B so that the common mode of the not shifted version of the input moves to the middle of the eye opening. The fourth feedback sets the phase of the latching clock of DS to the optimum latching position by comparing two versions of the not shifted input data latched by two clocks with slight phase difference. The phase shift control in each DS can be switched between the automatic and manual modes of operation by the SPI bits off_fbdelm for MSB and off_fbdell for LSB. In manual mode (off_fbdelm/l = “High”), the SPI bytes delm and dell can be used to fine tune the sampling point in each DS manually. Fig. 14 shows the dependence of latency (in *ps*) of the clock buffer of DS1/2 on the control delm/l.

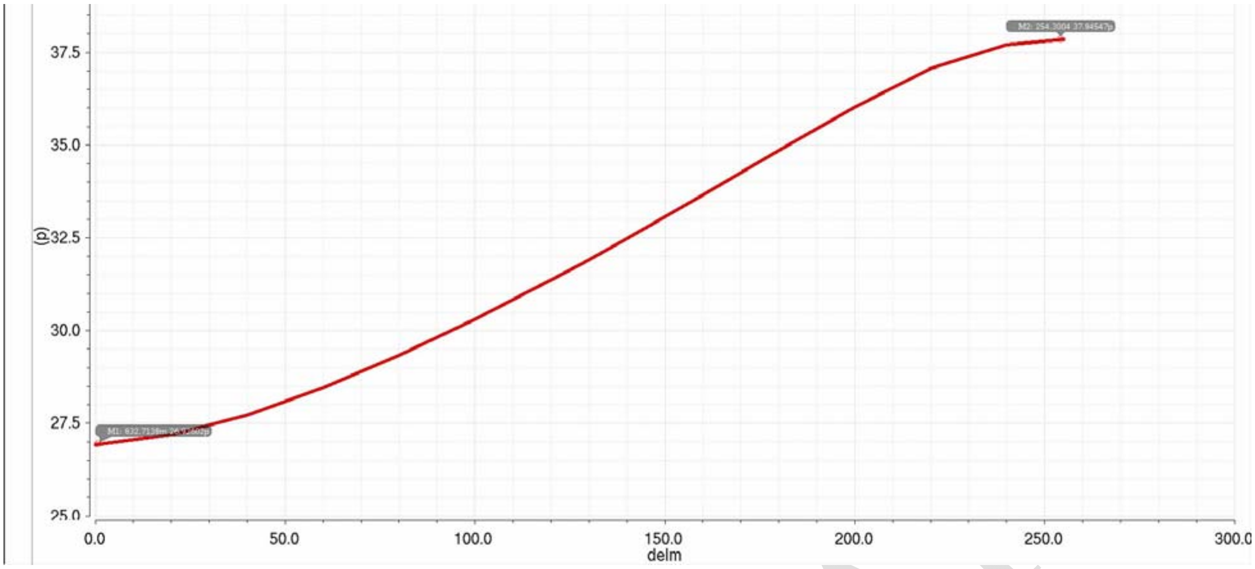


Fig. 14. Clock Tree Block Latency Vs. delm/l

As a result, both MSB and LSB eyes are independently scanned vertically and horizontally by feedback loops in each DS to derive the optimum latching point in order to minimize latching errors. The version of the input data that is not shifted is optimally latched by the full-rate clock. In each DS there are three copies of this signal that are delayed relative to each other. The second copy (t2m/t2l) is delayed by one clock period in relation to the first (t1m/t1l), and the third copy (t3m/t3l) is delayed by one clock period in relation to the second (t2m/t2l). Output copies of MSB data from DS1 and LSB data from DS2 with the same delay form a set of tap signals which are fed back to summation blocks of DFE for eye shaping optimization.

DMX

The reconstructed data streams from DS1 and DS2 are demultiplexed by a dual demultiplexer 1-to-16 (DMX1:16x2) block and delivered to the output SSTL interface as single-ended signals qm00-qm15 and ql00-ql15 together with the corresponding low-speed differential SSTL clock clop/clon. Additional 32 inverted single-ended data output signals are internally terminated to a special external supply v0p6=+0.6*V* to cancel out the switching noise. All LSB bits are inverted to avoid the 11 state in the corresponding LSB and MSB bits.

DMX1:16x2 can also provide a standard fill pattern instead of real data. The fill pattern mode is activated by the external digital signal onfill. To cancel out the switching noise, half of the fill pattern including bits ql00-ql07 and qm00-qm07 may be inverted using the SPI bit on_ptrninv.

The two parallel 1-to-16 Demultiplexers (DMX1:16) latch in the retimed data stream MSB and LSB from DS1 and DS2 on both edges of the half rate clock signal C2. Each of the two high speed data signals is subsequently demultiplexed into 16 NRZ data signals. The 32 single-ended data output signals as well as the differential low-speed output clock signal (full-rate clock divided by 32) are delivered to the output pins qm00-qm15, ql00-ql15, and clop/clon through CMOS output buffers. The additional 32 inverted single-ended data output signals are internally terminated to a special external 0.6*V* supply to cancel out the switching noise. The first bits of a serial stream are qm15 and ql15. All LSB bits are inverted to avoid the 11 state in the corresponding LSB and MSB bits. This results in the output encoding shown in Table 2.

Table 2. DEMUX Output Encoding

Slicer code	00	01	11
PAM3 bit value	0	1	2
NRZ bit value	0	Does not exist	1
Output MSB	0	0	1
Output LSB	1	0	0

The input CMOS pin onfill can be used to switch between Data output mode and Fill-Pattern output mode (onfill = "Low" (default): Data mode; onfill = "High": Fill-Pattern mode). When Fill-Pattern mode is selected, internally generated fill pattern is delivered to the output pins instead of input data. The 64-bit pattern consists of alternating 16 logic "0"s and 16 logic "1"s followed by alternating 16 logic "1"s and 16 logic "0"s. As a result, an alternating double logic "1" or double logic "0" appears at each of 32 outputs after every 30 bits. To cancel out the switching noise, half of the fill pattern including bits ql00-ql07 and qm00-qm07 may be inverted using the SPI bit on_ptrninv.

The clock divider that provides divided clock signals (c4, c8, 16, and c32) for demultiplexation is automatically reset during power-up in order to provide correct phase relations between divided clocks signals. The divider can be manually reset by applying an active "Low" voltage pulse to the CMOS input pin rstn. The pin rstn has to be connected to "High" voltage or left unconnected for the divider to become operational.

3-Wire Interface

All functions of the chip are controlled through the 3-wire SPI. The interface includes a 20-byte internal register and operates with CMOS signals with any levels from 1.2*V* to 3.3*V*. The 3.3*V* mode is preferred. The SPI operates in Mode 0: data changes at falling edges of SCLK and is sampled at its rising edges.

In the write operational mode, the read enable signal RdOn must be set to logic "0" before SSn becomes active and must stay unchanged until SSn release. The internal data is updated at a rising edge of SSn. In the read operational mode, the read enable signal RdOn must be set to logic "1" before SSn becomes active and must stay unchanged until SSn release. The output data transmission starts at a rising edge of SSn. The bit map of the interface is shown in Timing Diagram
Table 3, and its timing diagram in Fig. 15.

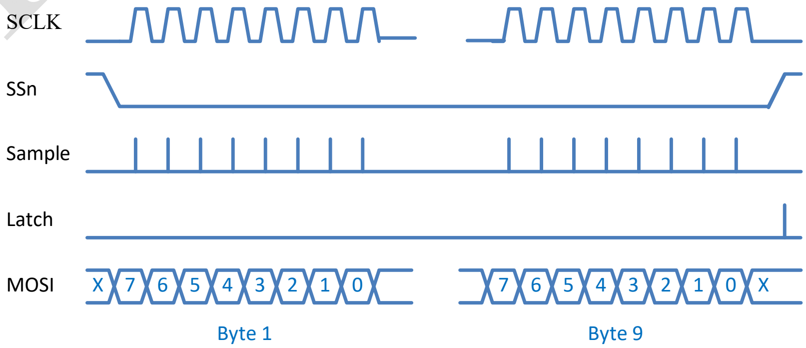


Fig. 15. SPI Timing Diagram

Table 3. 3-Wire Interface Bit Map

Byte #	Bit #	Bit order	Signal name	Signal function	Default State
1	From 7	MSB	shs	Initial adaptive FB balance at nominal temperature	“10000000”
	to 0	LSB			
2	From 7	MSB	shp	Temperature variation control of adaptive FB balance	“10000000”
	to 0	LSB			
3	From 7	MSB	vcscadj	Adjustment of cascode reference voltage in high speed analog buffers	“10000000”
	to 0	LSB			
4	From 7	MSB	t1tw	Tap 1 weight manual control (FB off)	“10000000”
	to 0	LSB			
5	From 7	MSB	t2tw	Tap 2 weight manual control (FB off)	“10000000”
	to 0	LSB			
6	From 7	MSB	t3tw	Tap 3 weight manual control (FB off)	“10000000”
	to 0	LSB			
7	From 7	MSB	icpp	CR phase loop gain adjust	“00000000”
	to 0	LSB			
8	From 7	MSB	icpf	CR frequency loop gain adjust	“00000000”
	to 0	LSB			
9	From 7	MSB	rangecrl	VCO locking range control	“00000000”
	to 0	LSB			
10	From 7	MSB	vcrl1	Varactor control of SUM1	“10000000”
	to 0	LSB			
11	From 7	MSB	vcrl2	Varactor control of SUM2	“10000000”
	to 0	LSB			
12	From 7	MSB	shc	Manual CM shift for AB1 and AB2 (FB off)	“10000000”
	to 0	LSB			
13	From 7	MSB	shin	Manual CM initial shift for SUM3A and SUM3B (FB off)	“10000000”
	to 0	LSB			
14	From 7	MSB	dshm	Manual CM shift for SUM3A (FB off)	“10000000”
	to 0	LSB			
15	From 7	MSB	dshl	Manual CM shift for SUM3B (FB off)	“10000000”
	to 0	LSB			
16	From 7	MSB	delm	Manual clock phase shift for DS1(FB off)	“10000000”
	to 0	LSB			
17	From 7	MSB	dell	Manual clock phase shift for DS2(FB off)	“10000000”
	to 0	LSB			
18	From 7	MSB	cedel	Manual clock phase shift for CIB(CR off)	“10000000”
	to 0	LSB			
19	7		--	Not used	“1”
	6		offcr	CR disable	“0”
	5		onnrz	Input NRZ mode enable	“0”
	4		off_fbt1tw	Tap 1 FB disable	“0”
	3		off_fbt2tw	Tap 2 FB disable	“0”

Byte #	Bit #	Bit order	Signal name	Signal function	Default State
	2		off_fbt3tw	Tap 3 FB disable	"0"
	1		on_ptrninv	Inverts fill patterns for half of outputs	"0"
	0		off_fbc	Automatic CM shift for AB1 and AB2 disable	"0"
20	7		off_fbin	Automatic initial CM shift for SUM3A and SUM3B disable	"0"
	6		off_fbdshm	SUM3A CM shift FB disable	"0"
	5		off_fbdshl	SUM3B CM shift FB disable	"0"
	4		off_fbdelm	DS1 clock phase shift FB disable	"0"
	3		off_fbdell	DS2 clock phase shift FB disable	"0"
	2		--	Not Used	"0"
	1		--		"0"
	0		--		"0"

The SPI internal registers are preset to the default states at the power supply activation time.

TERMINAL FUNCTIONS

TERMINAL			Description
Name	No.	Type	
CMOS I/Os			
SSn	45	1.2*V* CMOS I/Os	3-wire interface enable input with internal 536*KOhm* pull-up to vcc
SCLK	46		3-wire interface clock input with internal 536*KOhm* pull-down to vee
MOSI	48		3-wire interface data input with internal 536*KOhm* pull-down to vee
MISO	49		3-wire interface 3-state data output activated by 3wrdon control signal
rdon	53		3-wire interface read/write select input with internal 536*KOhm* pull-up to v1p2 (active: low – write and read; default: high – read only)
onfill	18		Active-high fill pattern activation flag (fill pattern replaces output data), default: low (536*KOhm* to vee)
onnrz	19		Active-high input data type selector (two-level NRZ-type input data), default: low (536*KOhm* to vee)
lol	20		Active-high loss of lock indicator output
rstn	22		Active-low DeMUX reset signal with internal 536*KOhm* pull-up to vcc
losin	23		No input signal indicator input with internal 536*KOhm* pull-down to vee
PLL Loop Filter			
fltr	21	Analog	Pin for external loop filter connection

TERMINAL			**Description**
Name	**No.**	**Type**	
High-Speed I/Os			
dp	40	CML-type Analog Inputs	Differential high-speed data inputs with internal SE 50Ohm termination to vcc
dn	39		
cep	34		Differential high-speed clock inputs with internal SE 50Ohm termination to vcc
cen	33		
Low-Speed I/Os			
ql00	66	SSTL Outputs	Single-ended low-speed data outputs
ql01	78		
ql02	59		
ql03	80		
ql04	70		
ql05	72		
ql06	64		
ql07	86		
ql08	67		
ql09	79		
ql10	60		
ql11	81		
ql12	71		
ql13	73		
ql14	65		
ql15	87		
qm00	4		
qm01	90		
qm02	10		
qm03	92		
qm04	98		
qm05	96		
qm06	6		
qm07	85		
qm08	3		
qm09	89		
qm10	9		
qm11	91		
qm12	97		
qm13	95		
qm14	5		
qm15	84		
clop	57	SSTL Output	Single-ended low-speed direct clock output
clon	58		Single-ended low-speed inverted clock output
crp	28	LVDS Input	Differential low-speed reference clock inputs
crn	27		
qpk	16	DC Analog Output	Direct output of input peak detector
qcm	17		Common mode output of input peak detector

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vee	Analog ground	25, 26, 29, 32, 35, 38, 41, 44, 50, 51
veed	Digital ground	2, 13, 56, 63, 74, 77, 88, 99
v4p3	+4.3*V* analog power supply in relation to vee	30, 43
vcc	+3.3*V* analog power supply in relation to vee	14, 24, 31, 36, 37, 42, 52, 54
vcc_vco	+3.3*V* VCO power supply in relation to vee	15
vccd	+1.2*V* digital power supply in relation to veed	7, 8, 55, 68, 69, 82, 83, 93, 94
v1p2	+1.2*V* internal positive supply control pin	47
v0p6	+0.6*V* termination supply in relation to veed	1, 11, 12, 61, 62, 75, 76, 100

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee, veed		0.0		*V*	External ground
vcc, vcc_vco		3.3		*V*	positive in relation to vee
v4p3		4.3		*V*	positive in relation to vee
vccd		1.2		*V*	positive in relation to veed
v0p6		0.6		*V*	positive in relation to veed
I_{vcc}		907		*mA*	Depending on the state of SPI control bytes
I_{vcc_vco}		18		*mA*	
I_{v4p3}		126		*mA*	
Power Consumption		4.0		*W*	
I_{veed} , I_{vccd}		400		*mA*	
I_{v0p6}		±380		*mA*	Bi-directional termination current
Junction temperature	0	50	125	°*C*	
Data input (d1p/d1n, d2p/d2n)					
Data rate	DC		25.6	*Gb/s*	
SE Swing	400		600	*mV*	
Input termination		50		*Ohm*	
Data output (qXX)					
Interface		SSTL-12			
Data rate	DC		1.6	*Gb/s*	
Low-speed clock output (clop/n)					
Interface		SSTL-12			two complementary outputs
Data rate	DC		800	*MHz*	
Reference clock input (crp/n)					
Interface		LVDS			
Data rate	DC		800	*MHz*	
3-Wire Interface					
Clock frequency	0.1		50	*MHz*	
In/out low logic level	vee		vee+0.1	*V*	
In/out high logic level	vee+1.1		vee+1.3	*V*	
Input current			9	*uA*	For each input

PACKAGE INFORMATION

The chip die is housed in a custom, 100-pin CQFP package shown in Fig. 16. The package provides a center heat slug located on the back side of the package to be used for heat dissipation. ADSANTEC recommends using extreme caution when soldering this section to the board to avoid overheating. It should be connected to the vccd plain.

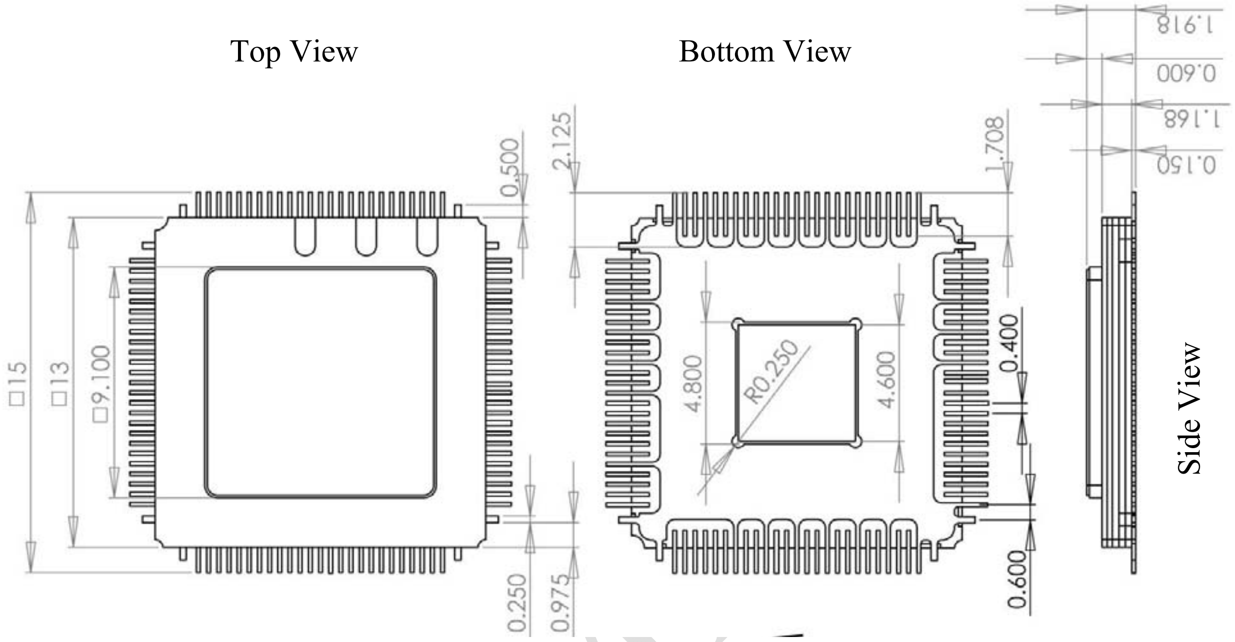


Fig. 16. CQFP100 Package Drawing (All Dimensions in mm)

The part's identification label is ASNT8763-KMT. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
0.0.1	03-2025	Initial draft