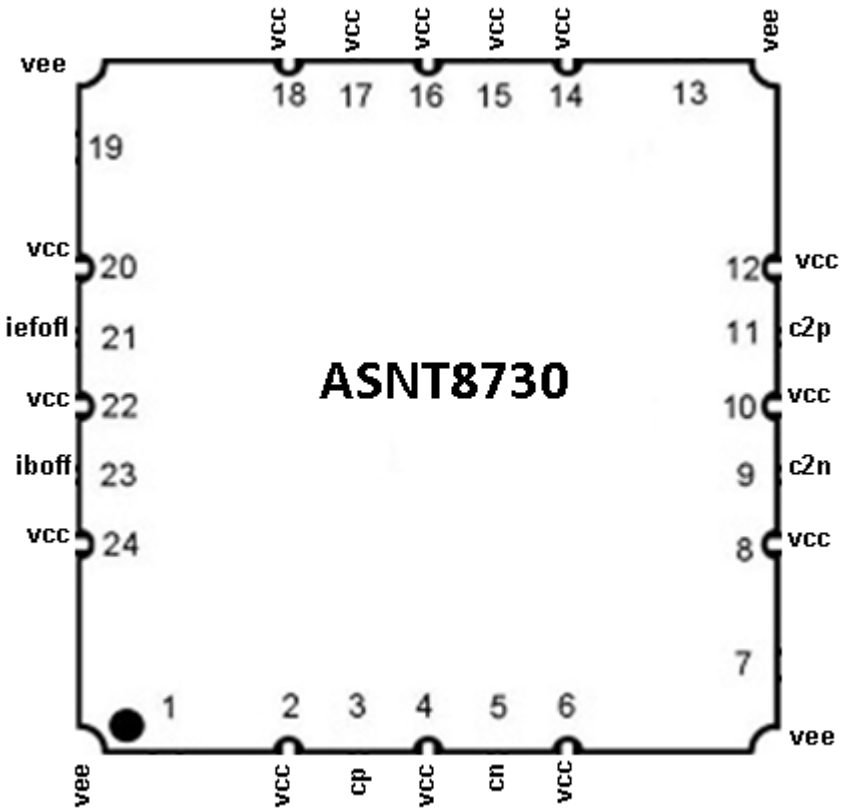
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ASNT8730-KHC
DC-64*GHz* Broadband Clock Divider by 2

- High speed broadband clock divider by 2
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Fully differential CML input interface
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +3.3 *V* or -3.3 *V* power supply
- Power consumption: 460 *mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFN 24-pin package



Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505
Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

DESCRIPTION

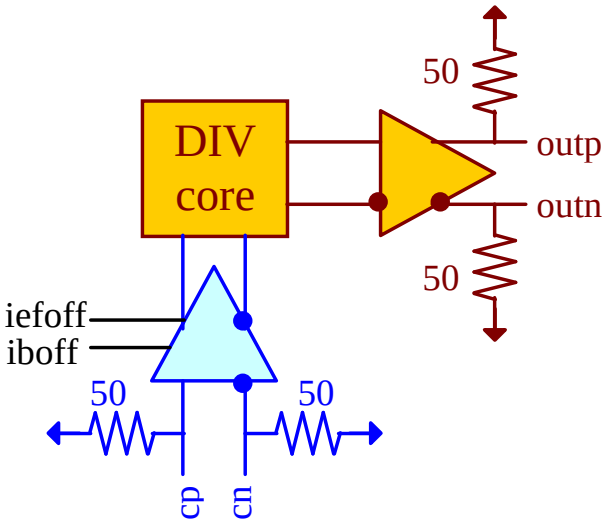


Fig. 1. Functional Block Diagram

The temperature stable ASNT8730-KHC SiGe IC provides broadband clock divide-by-2 functionality, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can process a high-speed clock input signal cp/cn and deliver a high-speed clock output signal qp/qn with 50% duty cycle.
Static control signals iboff and iefoff provide option to increase device bandwidth by slightly increasing power consumption. In default (unconnected) state control signals are pulled-up to vcc to save power consumption. To activate boost mode low level voltage should be provided to both or just one of control inputs.

The part's I/O's support the CML logic interface with on chip 50 *Ohms* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0 *V* = ground and vee = −3.3 *V*), or positive supply (vcc = +3.3 *V* and vee = 0.0 *V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50 *Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0 *V* and vee = -3.3 *V*.

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505
Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.36	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cp	3	CML input	Differential clock inputs with internal SE 50 *Ohms* termination to vcc
cn	5		
qp	11	CML output	Differential clock outputs with internal SE 50 *Ohms* termination to vcc. Require external SE 50 *Ohm* termination to vcc
qn	9		
Low-Speed I/Os			
ieoff	21	CMOS Input	Static control CMOS33 signal. High level (default) saves power, low level increases input buffer slew.
iboff	23	CMOS Input	Static control CMOS33 signal. High level (default) saves power, low level increases input buffer gain.
Supply and Termination Voltages			
Name	**Description**		**Pin Number**
vcc	Positive power supply (+3.3 *V* or 0 *V*)		2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24
vee	Negative power supply (0 *V* or -3.3 *V*)		1, 7, 13, 19

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		140		*mA*	
Power consumption		460		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Clock (cp/cn)					
Frequency	DC	64		*GHz*	
Swing	0.2	0.4	1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Clock (qp/qn)					
Frequency	DC	32		*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.4		*V*	With external 50 *Ohms* DC termination
Latency	38		50	*ps*	
Rise/Fall times	8.0	8.5	9.5	*ps*	20%-80%
Output Jitter		0.02	0.1	*ps*	Peak-to-peak
Duty cycle	45	50	55	*%*	

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFN package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part’s identification label is ASNT8730-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package’s manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

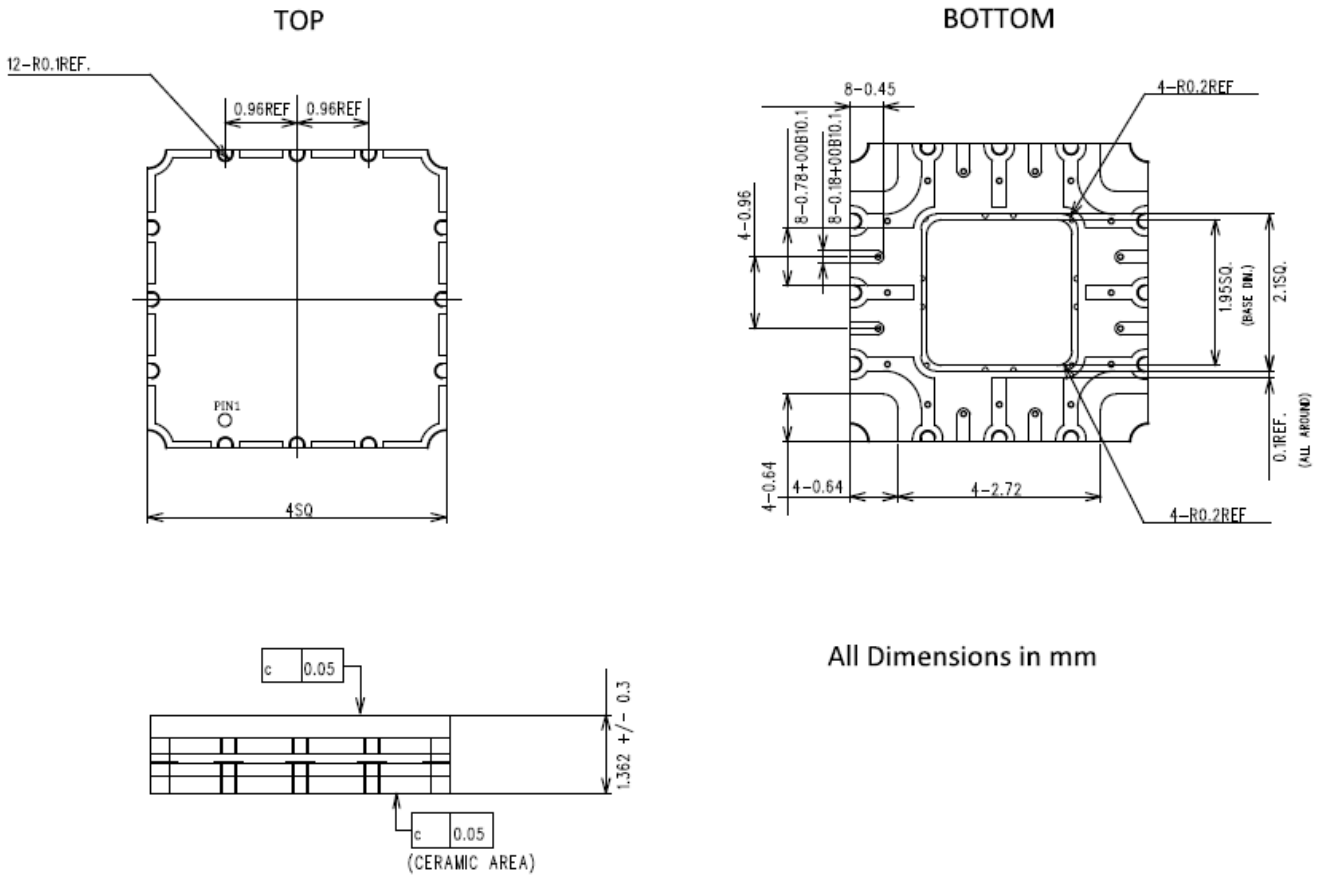


Fig. 2. CQFN 24-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.0.2	04-2025	Added latency information
0.0.2	02-2023	First release