ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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ASNT_PRBS20D_V2
PRBS9/10 Generator Featuring Jitter Insertion, Selectable Sync, Output Amplitude Control and USB Control

- Broadband operation from 20*Mbps* – 22.0*Gbps*
- Fast rise and fall times
- Two PRBS data outputs with output amplitude control
- Up to 140*ps* delay variation on each output
- Built-in Programmable Clock Generator
- External high-speed clock input capability (AC-coupled on board)
- Differential high-speed clock output
- 50% duty cycle for sync output on all divide ratios
- USB Software GUI Control Interface via USB 2.0
- Single positive 5*V* supply

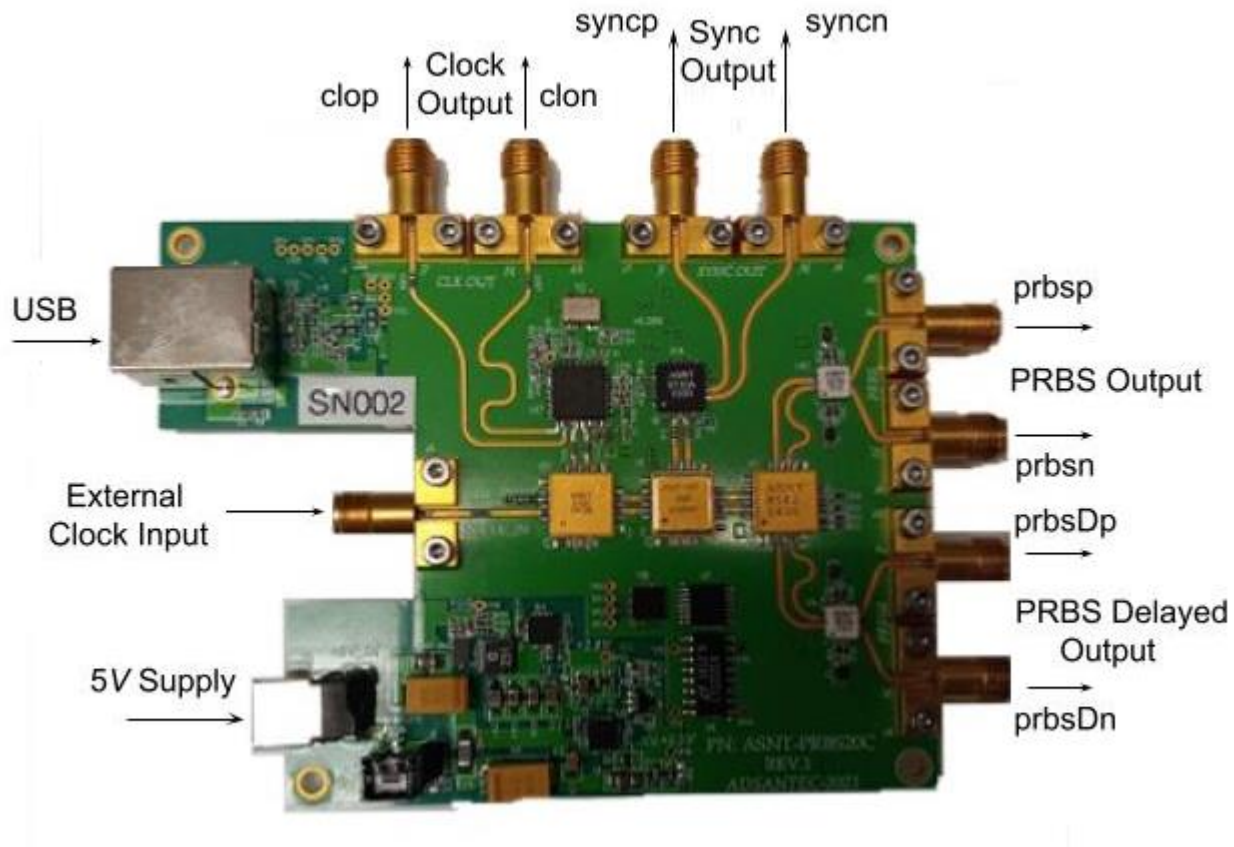

Fig. 1 ASNT_PRBS20D_V2 board

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DESCRIPTION

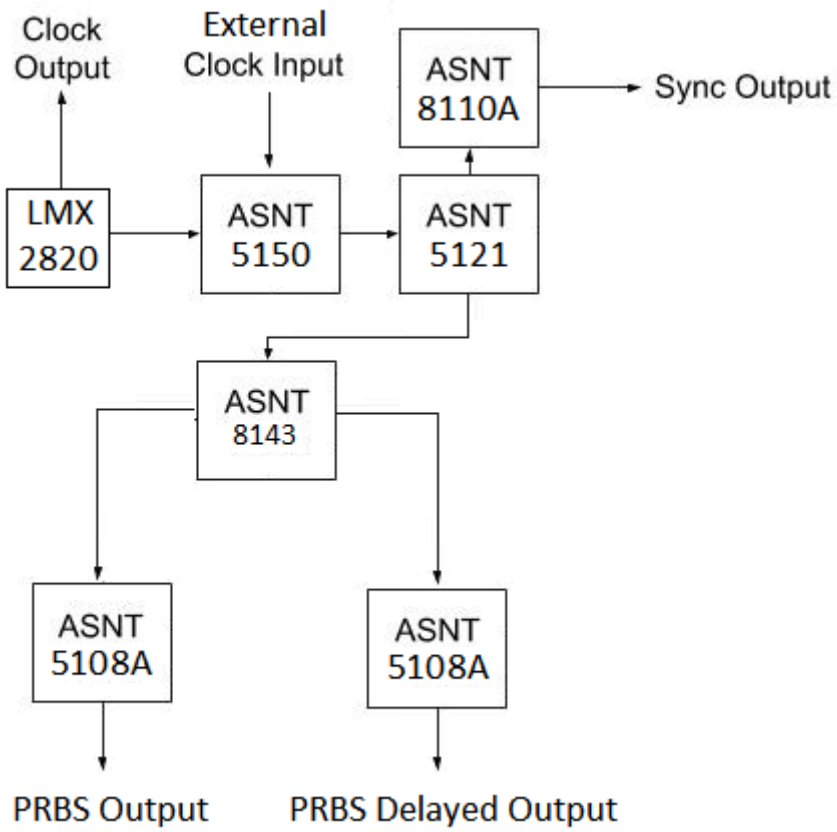

Fig. 2 PCB Block Diagram

The ASNT_PRBS20D_V2 is a broadband 2^9-1, or 2^{10}-1 PRBS generator intended for test, and prototyping of microwave communication applications. The board features a programmable clock synthesizer up to 22GHz, while also supporting an external clock input. The PRBS data amplitude is adjustable from 50mV to 800mV single-ended peak to peak, and its phase is adjustable up to 140*ps* for both differential outputs. A single-ended clock from 20*MHz* to 22*GHz* with an amplitude as low as 50*mV* peak to peak may be applied to the high-speed clock input. An independent differential clock output from the internal programmable clock generator is provided. A programmable differential Sync Output provides a divided copy of the input clock with a division ratio from 1 to 256. The Sync Output is mainly used to trigger a high-speed oscilloscope. The system is capable of triggering an eye diagram for PRBS9/PRBS10. The USB 2.0 port allows the board to connect to any compatible PC for a simplified software-based operation.

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OPERATION

1. Measure the output traces of all I/O's aside from the sync outputs in reference to the 3.3*V* test point; all should measure 50*Ohms*. Measure the sync output traces in reference to the 2.8*V* test point; these should also measure 50*Ohms*. Due to on-board capacitors, it is not possible to measure all outputs at the connectors.
2. Connect the power supply (provided) to the board, and connect to any PC via an USB cable.
3. Install the included software on the connected PC following the software installation dialog box as shown in **Fig. 3**.

   (This step will not need to be repeated unless switching PC's).

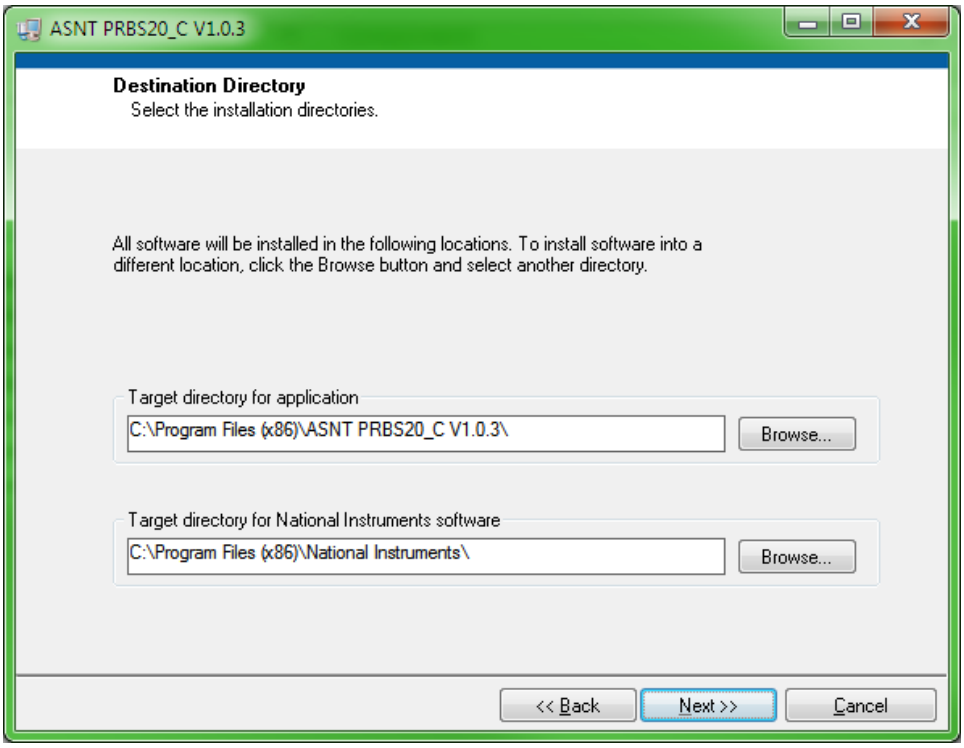

Fig. 3 Software Installation Dialog

4. After the installation is complete, initiate the GUI software and confirm its connection by ensuring that the USB Connection Indicator light is green as it's depicted in **Fig. 4**.
5. The Clock Input Control can be used to select the use of either on-board synthesized, or externally generated clock when desired. If using an external input clock signal, a DC block is not required due to on-board integrated AC coupling.
6. When connecting sync outputs or data outputs from the board, DC blocks are required.
7. Set the frequency as desired either via the software GUI, or through manipulation of the external clock signal.

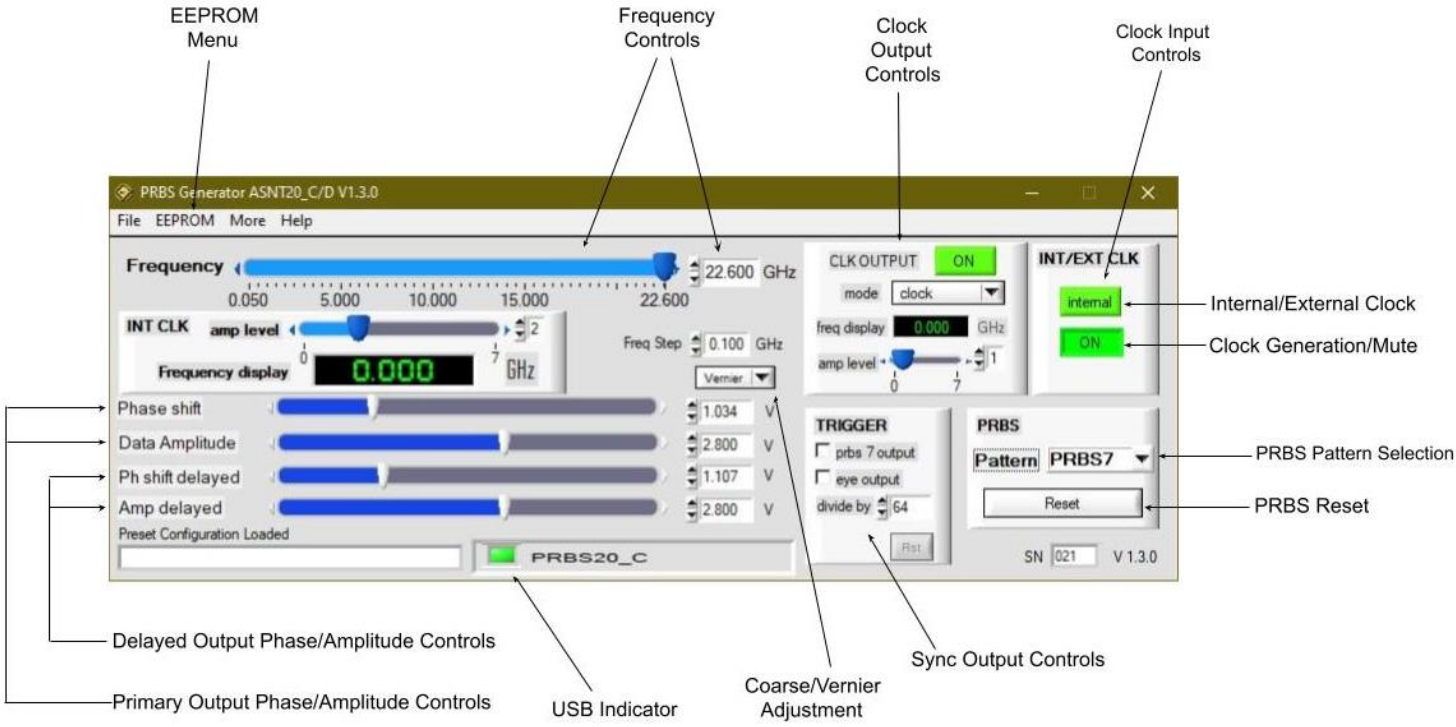

Fig. 4 Software GUI

NOTE: The latest software is now capable of auto-detection of the PRBS pattern types available and will change to PRBS20D upon connection of the USB cable once power is applied and the software is running.

7. The PRBS Selection/Reset Control can be used to select the desired output pattern (PRBS9/PRBS10), and to provide a PRBS reset when necessary (The board is equipped with automatic reset).

8. The Clock Output Control can be used to enable/disable the clock output from the built-in frequency synthesizer used for data generation. The amplitude of the output clock can also be controlled from here. Using the "**mode**" drop down window, the controls will allow for a divided clock output when desired. Note that these clock outputs are also AC coupled on-board.

9. The Sync Controls (Trigger) can be used to manipulate the division ratio used for the sync signal output; it can also be used to set a manual division ratio when desired. Note that the sync output does not provide a high enough division ratio to view PRBS9/PRBS10 output as a pattern; one data output can be divided by 256 or 512 respectively to view these patterns if necessary.

10. The Amplitude Controls (Data Amplitude and Amp delayed) can be used to adjust the amplitude of both the PRBS Output, and the Delayed PRBS Output. The Phase Shift (Phase Shift and Ph shift delayed) controls can also be used to adjust the phase of each data output by up to 140*ps*.

11. Configuration settings, by default, are saved to a cfg file within the installation directory; when desired, settings can also be saved (or loaded) directly from the EEPROM menu.

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12. The PRBS Drift (Jitter Insertion) Controls can be used to inject jitter into the output signal if desired. The Step Value and Step Count can both be used to create jitter in different ways, or be used in combination, with higher values corresponding with greater inserted jitter. This option can be found under the "More" tab (labeled as Additional Controls in the diagram above).

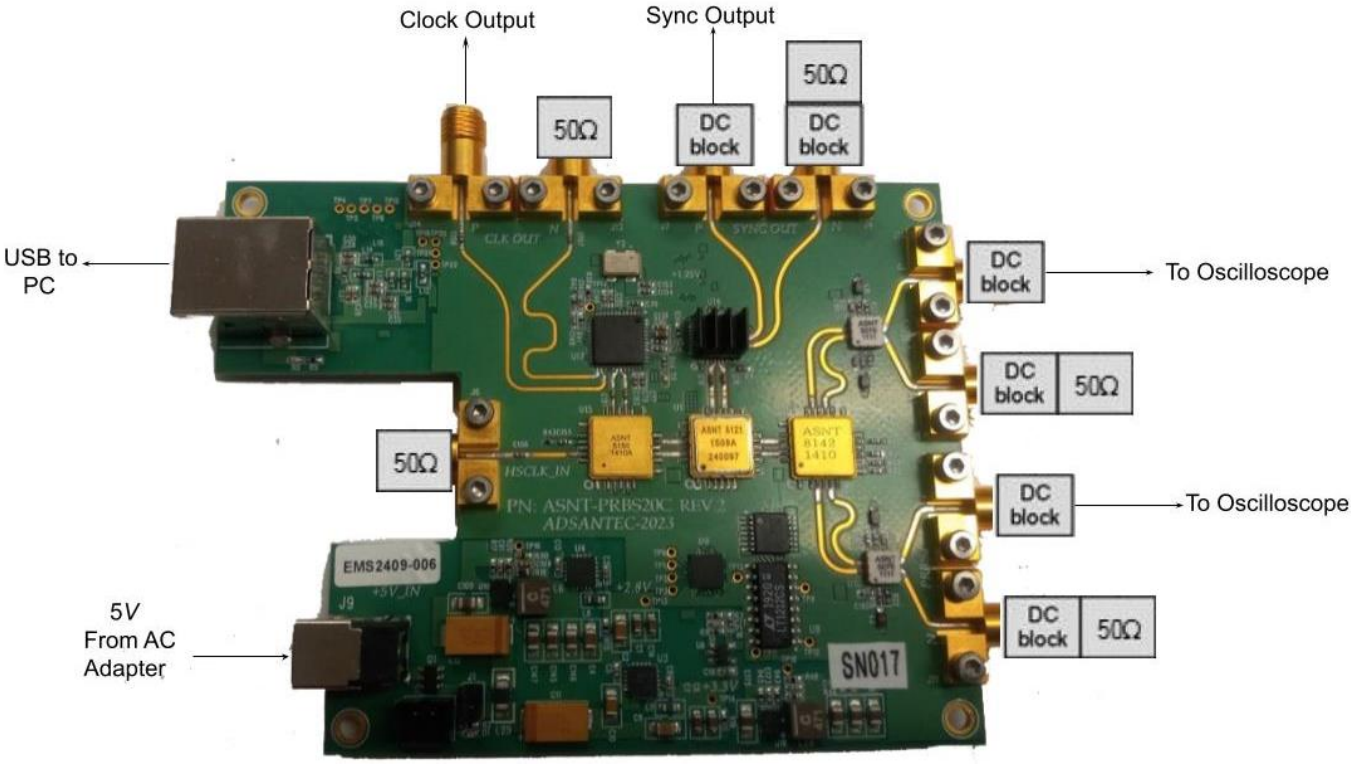

Fig. 5 Recommended Board Configuration Diagram

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
vee		0		*V*	External ground
vcc		5.0		*V*	Provided
I_{VCC}	1.7	2.2	2.6	*A*	
Power		13		*W*	
Operating Temperature	-25	50	85	*°C*	
External Clock Input					
Frequency	0.02		22	*GHz*	
Single-Ended Swing	50	400	1000	mV_{PP}	
Clock Output (clop/clon)					
Frequency	0.02		22	*GHz*	
Single-Ended Swing	50		1000	mV_{PP}	
High-level output voltage		2.4		*V*	
Low-level output voltage			0.4	*V*	
Duty Cycle	45	50	55	%	For Clock Signal
Sync Output (Trigger) (syncp/syncn)					
Frequency	0.01		22	*GHz*	Programmable Divider
Single-Ended Swing	500	600	1000	mV_{PP}	
Rise/Fall Times	15	17	19	*ps*	20%-80%
Duty Cycle	45%	50%	55%		
PRBS Output (prbsp/prbsn)					
Single-Ended Voltage Level	50	500	800	mV_{PP}	
Common Mode Level	vcc -0.3	vcc -0.25	vcc -0.2	*V*	
Duty Cycle	45	50	55	%	
PRBS Delayed Output (prbsDp/prbsDn)					
Single-Ended Voltage Level	50	500	800	mV_{PP}	
Common Mode Level	vcc -0.3	vcc -0.25	vcc -0.2	*V*	
Duty Cycle	45%	50%	55%		

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BOARD DIMENSIONS DIAGRAM

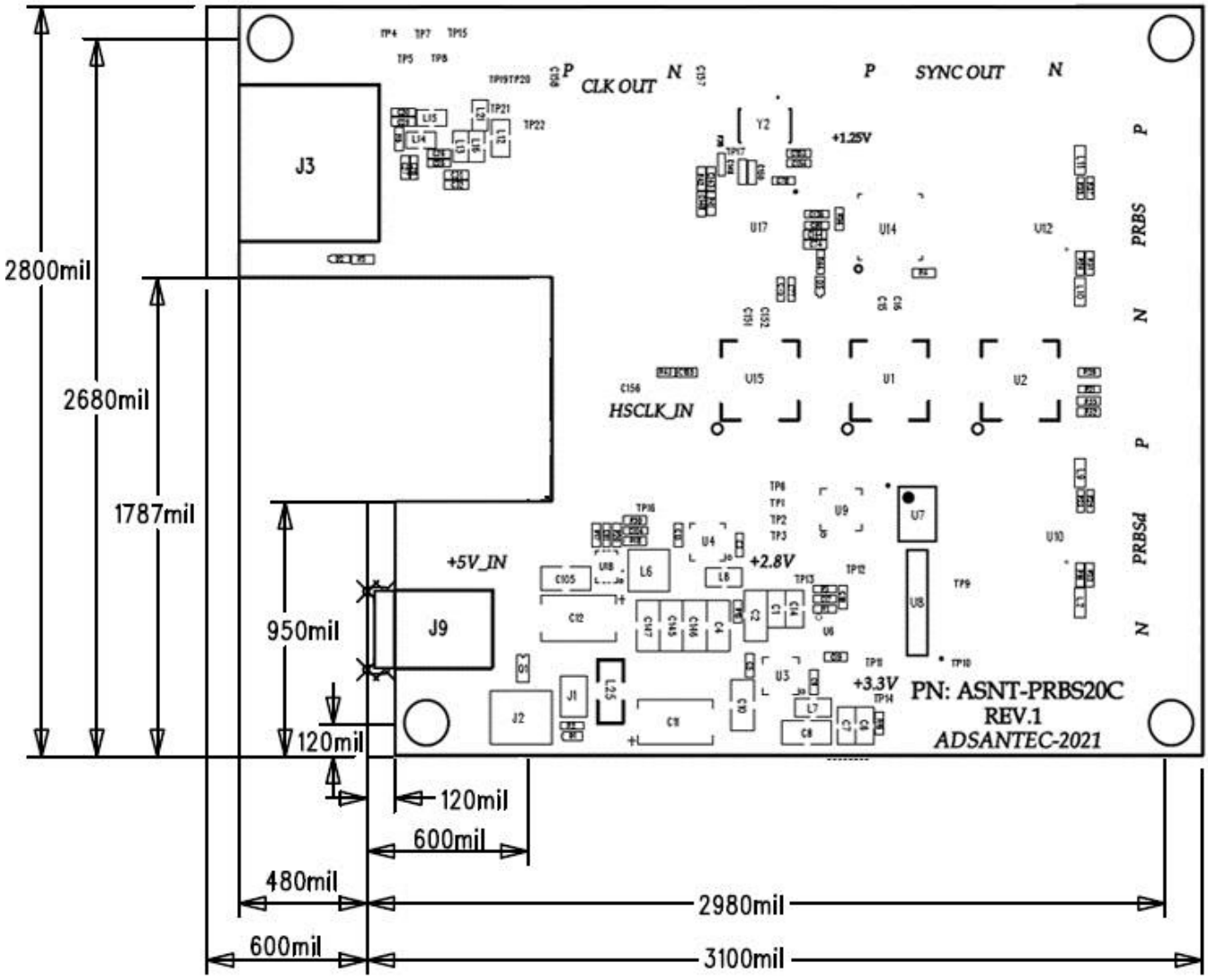

Fig. 6 Board Dimensions Diagram

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REVISION HISTORY

Revision	Date	Changes
1.2.2	04-2025	Updated ohmic check description Added requirement for DC blocks on sync and data outputs Added Fig. 5 Recommended Configuration Diagram
1.1.2	11-2024	Updated for use with latest software features
0.1.2	08-2024	Preliminary Release