ADSANTEC
Ultra High-Speed Mixed Signal ASICs
Advanced Science And Novel Technology Company, Inc.
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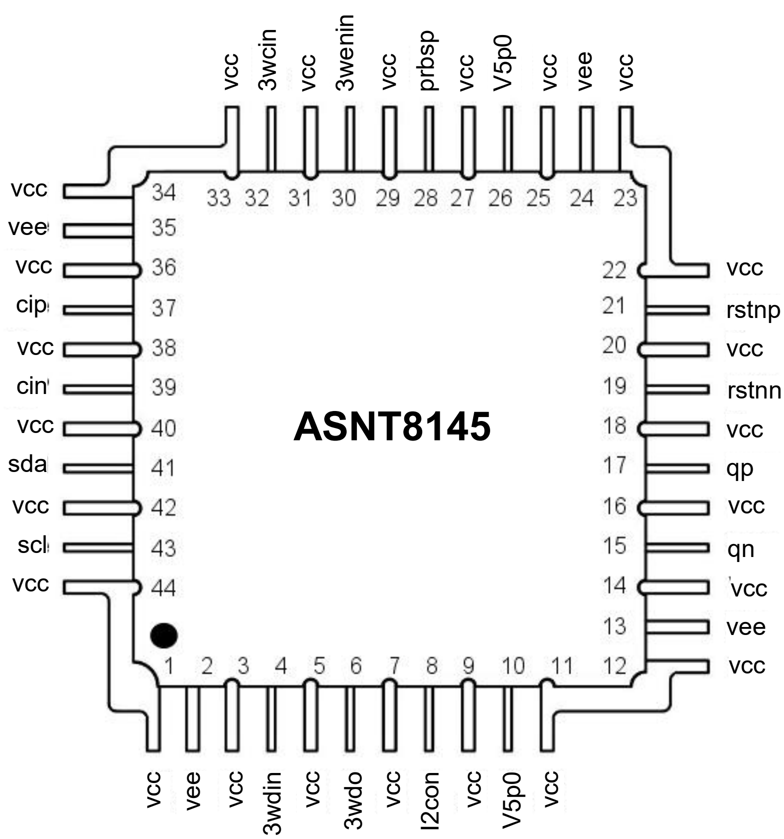
ASNT8145-KMM
Generator of DC-to-32*Gb/s* PRBS with Equalizer

- Full-length selectable (2^9-1) or (2^{10}-1) pseudo-random binary sequence (PRBS) generator
- DC to 32*Gb/s* output data rate
- Asynchronous reset signal for elimination of the "all zeros" initial state
- High-speed adjustable output linear equalizer with independently adjustable 3 zeros and 2 poles
- Fully differential CML output interface with adjustable single-ended swings up to 1.0*V* pk-pk
- Additional non-equalized single-ended CML output with a 440*mV* pk-pk swing
- Fully differential CML input interface
- SPI or I2C interface for chip control
- Limited temperature variation over industrial temperature range
- Separate power supplies for the data paths and AC control circuitry
- Power consumption: under 1.65*W*
- Custom CQFP 44-pin package



DESCRIPTION

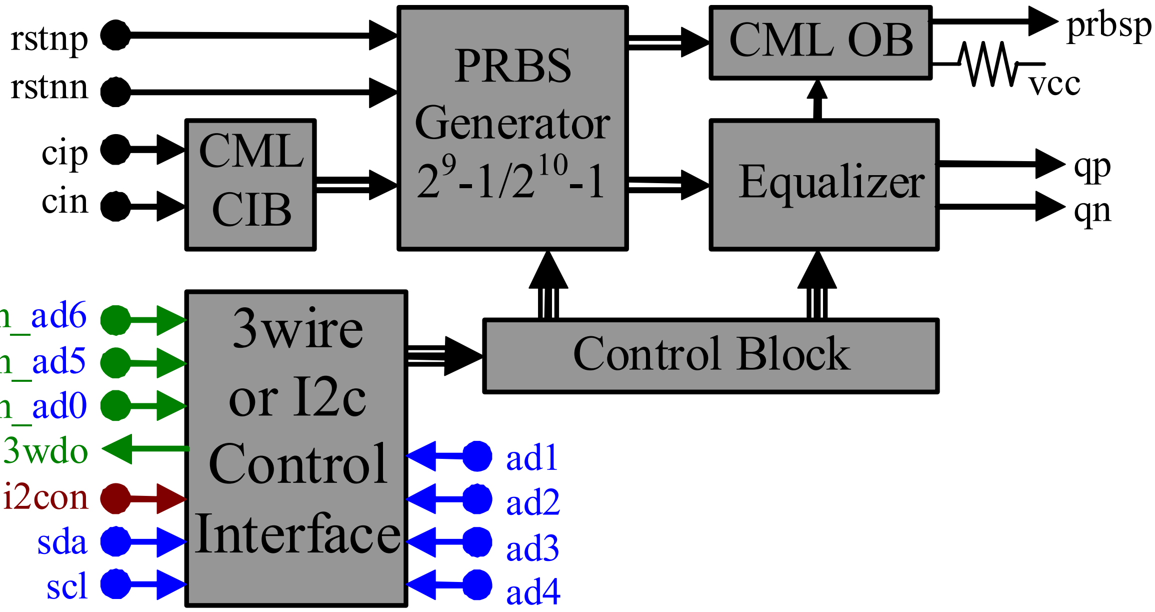


Fig. 1. Functional Block Diagram

The part shown in Fig. 1 is a PRBS generator with an additional output equalizer. The generator provides a selectable full 511-bit or 1023-bit long pseudo-random binary sequence (PRBS) signal according to either a $(x^9 + x^4 + 1)$, or a $(x^{10} + x^7 + 1)$ polynomial respectively, where x^D represents a delay of D clock cycles. An external high-speed clock is delivered to the PRBS generator through a differential CML input port cip/cin. The part provides two outputs: the main differential output from the Equalizer block and an additional non-equalized single-ended output from the differential CML_OB buffer. The second output of the buffer is internally terminated to vcc. The additional PRBS output is provided for control only and can be disabled to save power.

The equalization path has 8 controls: adjustable DC gain, adjustable linearity, 3 independently adjustable zeros, 2 independently adjustable poles, and additional high-frequency bandwidth control.

All equalizer controls, as well as the polynomial selection and the CML OB activation are delivered through a selectable 3-wire or I^2C digital interface. The type of active interface is defined by the external CMOS signal i2con.

PRBS Generator

The generator is implemented as a linear feedback shift register (LSFR) shown in Fig. 2, where the outputs of either the ninth and fourth, or tenth and seventh flip-flops are combined together by an XOR function, and provided as an input to the first flip-flop of the register. The generated 2^9-1 or 2^{10}-1 polynomial is defined by the digital control bit off10="1" or "0" respectively. The register is clocked by the external signal cip/cin.

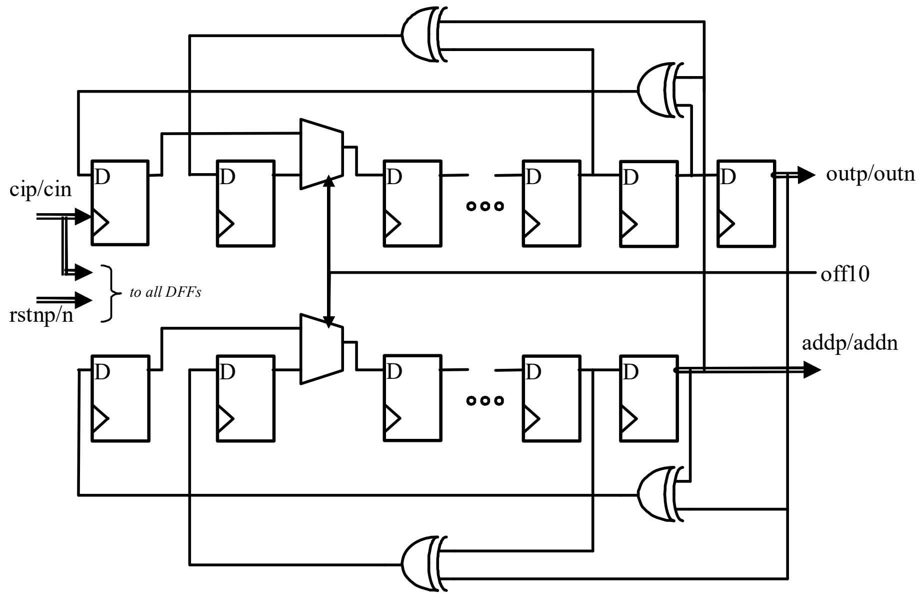


Fig. 2. PRBS Generator Functional Block Diagram

The LSFR-based PRBS generator produces binary states, excluding the "all zeros" state that is illegal for the XOR-based configuration. To eliminate this state that locks the LSFR and prevents PRBS generation, an asynchronous external active-low preset signal rstnp/rstnn is implemented in the circuit. When the preset is asserted, LSFR is set to the All-"1" state that is enough for activation of the PRBS generation.

The main outputs outp/outn of the generator are sent to the following Equalizer. The additional output addp/addn are processed by the CML OB and delivered to the direct output port prbsp, while the inverted output is internally terminated to keep the balance of the buffer.

Equalization Path

Typical AC responses of the Equalization Path are shown in Fig. 3.

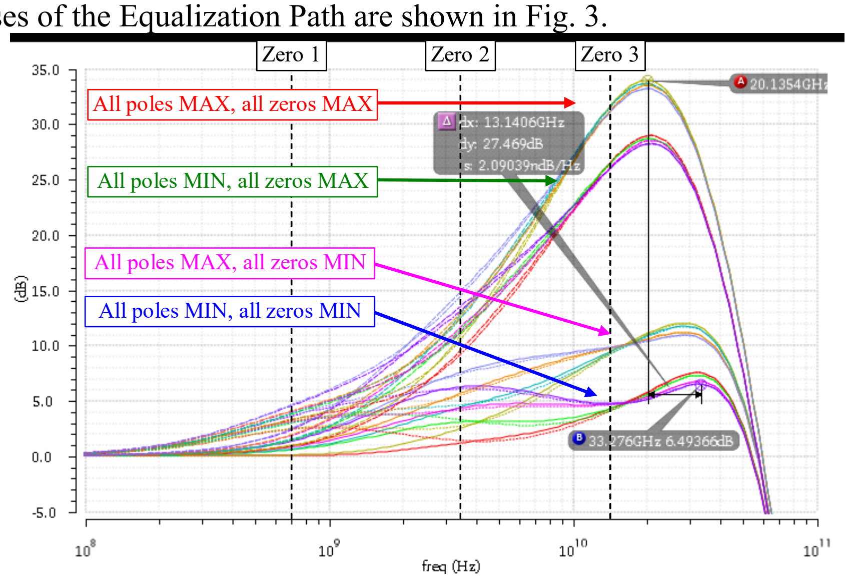


Fig. 3. Typical AC responses of the Equalization Path

The path has 3 independent adjustable Zeros, and two independent adjustable Poles. For each setting, the DC gain can be adjusted between -3dB and +5dB.

Additionally, the path's bandwidth (BW) can be also adjusted using EF controls as shown by the red and magenta curves in Fig. 4 that are plotted for the Min Pole, and Min Zero setting.

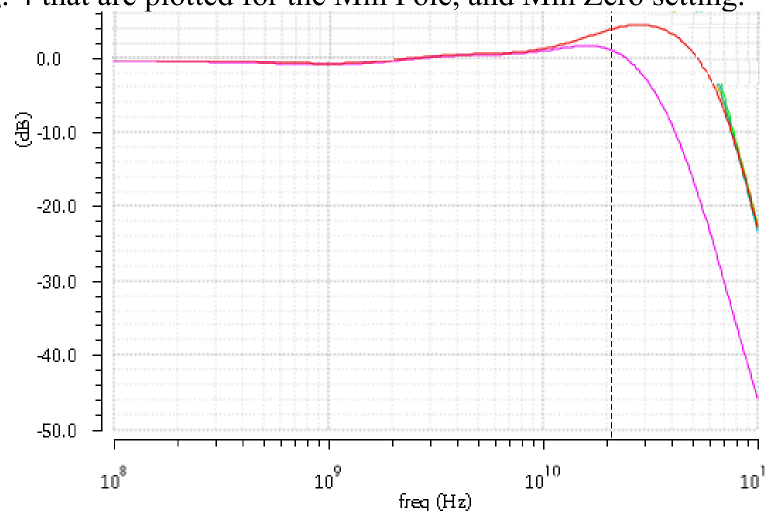


Fig. 4. BW Control Characteristics

If required, the channel's linearity can be adjusted using Ibuf controls. The higher values of the code correspond to higher linearity and higher power consumption of the IC. They also increase the channel's gain for any gain settings other than maximum.

Corresponding controls are detailed in Table 1. Increase of any control results in gain increase within a certain frequency range around the specified frequency as shown in the corresponding drawings.

Table 1. Data Channel Controls

Control function	**Frequency, *GHz***	**SPI name**	**GUI Slider name**	**Corresponding drawing**
Low-frequency zero	1	zcl	Zero at f / Lo	Fig. 3
Mid-frequency zero	5	zcm	Zero at f / M	Fig. 3
High-frequency zero	16	zch	Zero at f / Hi	Fig. 3
First pole	16	pc1	Pole / 1	Fig. 3
Second pole	16	pc2	Pole / 2	Fig. 3
Gain	DC	gc	Gain	
Output EF	>20	efc	Out BW	Fig. 4
Ibuf	DC	bufc	Linearity	

Digital Control Interface

All functions of the IC are controlled through a Digital Control Interface. The interface includes a 9-byte Control Register and operates with 3.3*V* CMOS signals (Fig. 5).

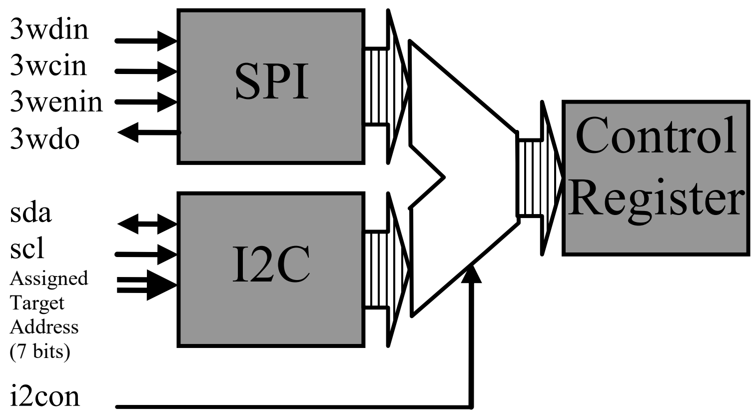


Fig. 5. Digital Interface Block Diagram

The Interface can operate either as SPI or as I^{2}C using different input ports: 3wdin, 3wcin, and 3wenin for the SPI, or sda and scl for the I^{2}C. A 7-bit chip address must be also assigned in the I^{2}C mode. The SPI or I^{2}C interface modes are selected by an external signal i2con equal "0" (default state) or "1" respectively. The bit map of the interface is shown in Table 2:

Table 2. Digital Interface Bit Map

SPI Byte Numbers or I2C Register Addresses	Bit Number	Bit order	Signal name	Default Value	Signal function
1	From 7 to 0	MSB LSB	zcl	10000000	Low-frequency zero control
2	From 7 to 0	MSB LSB	zcm	10000000	Middle-frequency zero control
3	From 7 to 0	MSB LSB	zch	01000000	High-frequency zero control
4	From 7 to 0	MSB LSB	gc	10000000	Gain control
5	From 7 to 0	MSB LSB	pc1	10000000	First pole control
6	From 7 to 0	MSB LSB	pc2	10000000	Second pole control
7	From 7 to 0	MSB LSB	efc	10000000	BW control
8	From 7 to 0	MSB LSB	bufc	10010010	Linearity control through stages current adjustment
9	7		oboff	1	Switch off prbsp output
	From 6 to 2		--	0000	
	1		sw_9_10	0	Select PRBS9 or PRBS10
	0		--	0	Constant "0"

Control registers are preset to the above default states at the time of the chip's power supply activation.

SPI Mode (i2con =”0”, default state):

The input data should switch at a falling edge of the clock signal 3wcin and are sampled by its rising edge. Control Register values update at a rising edge of the chip select signal 3wenin. The additional three-state output pin 3wdo can be used for reading the register contents. It goes to a high impedance state when the select signal is not active (high). A timing diagram of the SPI mode is shown in Fig. 6.

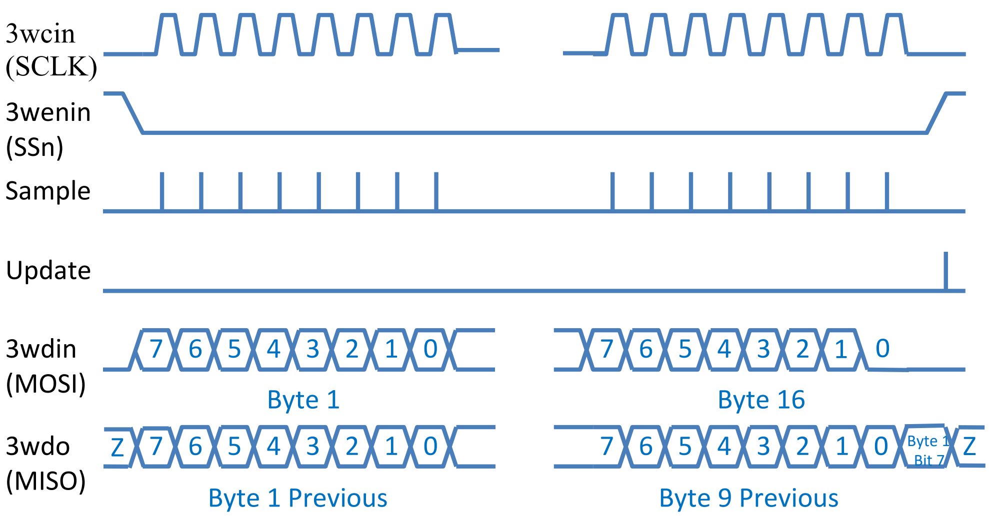


Fig. 6. SPI Timing Diagram

I²C Mode (i2con =”1”):

In the I²C mode, the two wires sda (serial data) and scl (serial clock) carry information between transmitters and receivers. Each target is recognized by a unique 7-bit address assigned by applying logic “0” or “1” to pins ad(0,5,6) pins corresponding to address bits 0,5,6 respectively, while the address bits 1-4 are internally set to “0”. It can operate as either a transmitter or receiver, depending on the function required (write or read). In both cases, an off-chip Controller generates scl for timing and starts or terminates each transfer.

All transactions begin with a START and are terminated by a STOP condition generated by the Controller. Data is transferred between a transmitter and a receiver synchronously to scl on the sda line on a byte-by-byte basis (Fig. 7). There is one scl clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of scl. The number of bytes that can be transmitted per transfer is unrestricted.

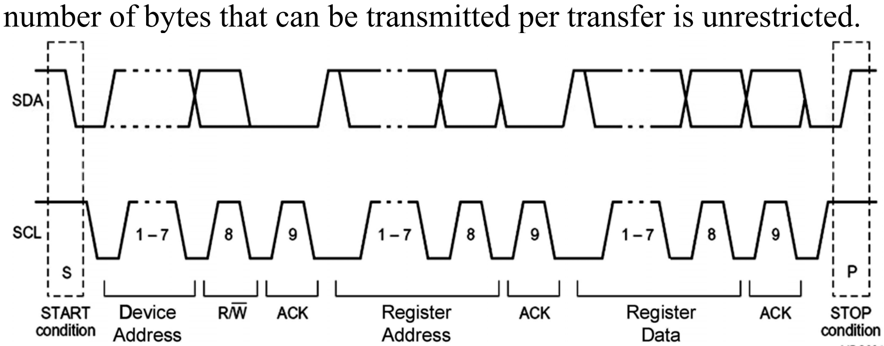


Fig. 7. I2C Timing Diagram

At the beginning of every transfer, the Controller sends a byte containing 7-bit target address followed by an eighth data direction bit that defines the operation (Read or Write). If the address sent by the Controller does not match the target's address, the target ignores the data transmission and stays in the idle state.

If the addresses match and the 8th bit is equal to "0", the target generates an acknowledge bit (ACK) and switches to write operational mode. After that, the target receives 2 more bytes from the Controller, acknowledging each one as shown in Fig. 8.

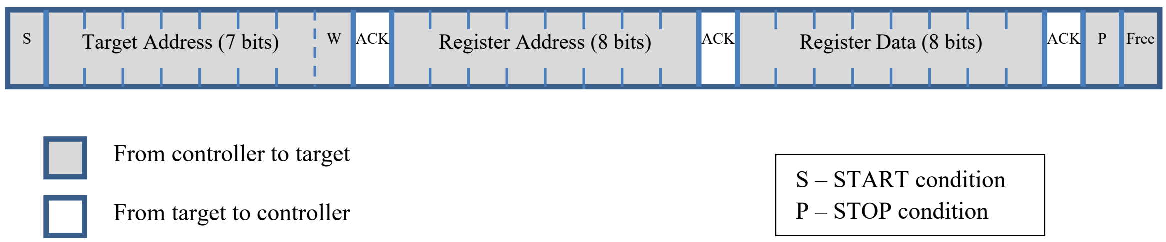


Fig. 8. I2C Control Register Write Sequence Transfer Directions

The first received byte represents the Control Register address (see Table 2). Only the four LSBs of the byte are used to represent the address while the four MSBs are ignored. The second received byte contains Data to be written into the corresponding Control Register when the transfer is completed. If the transfer contains more than 3 bytes, each next byte will be treated as Data and will overwrite the Control Register. The target interface does not check the Address validity, but if the received Register Address is out of range, no write operation is performed.

According to the I^{2}C-bus operation standard UM10204, the direction of transmission cannot be voluntary changed during a transfer. In this case, to read data from a particular Control Register, the Controller must use the so-called combined communication format as shown in Fig. 9.

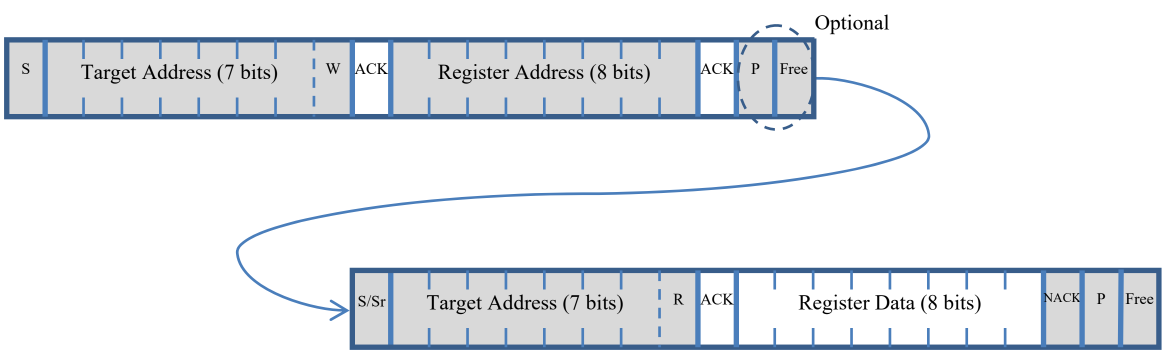


Fig. 9. I2C Control Register Read Sequence Transfer Directions

Before the actual reading, the Controller must initiate a standard write operation with the corresponding target address, followed by one byte representing the Control Register address to read from. The target receiver with the matching address will generate ACK for the received address and the following byte. After that, the Controller can generate a START/STOP (or a repeated START) condition and send the same target address again with the 8th bit set to "1". In response, the target receiver generates another

ACK and both the Controller and the target switch to opposite read/write modes. The controller-transmitter becomes a controller-receiver, and the target-receiver becomes a target-transmitter.

From this moment, the target controls the bus and sends data from Control Register to the Controller. All clock pulses must be still generated by the Controller, including the acknowledge bit 9th clock pulse. At the 9th clock of the Data byte, the Controller must generate Not Acknowledge (NACK), telling the target to stop the transfer and free the bus, allowing the controller to send the STOP condition.

If the Controller sends ACK instead of NACK at the 9th bit of the Data byte, this represents a request for sequential read access to the target's Control Registers. In this case, the target interface maintains an auto-increment of the previously provided register address and outputs data from the next register. To terminate the sequential read access, the Controller must NACK the last byte.

TERMINAL FUNCTIONS

TERMINAL			Description
Name	**No.**	**Type**	
			High-Speed I/Os
cip	36	CML Inputs	Differential high-speed clock inputs with internal SE 50*Ohm* termination to vcc
cin	38		
rstnp	16		Differential high-speed reset inputs with internal SE 50*Ohm* termination to vcc
rstnn	14		
qp	20	CML-type Outputs	Differential high-speed analog outputs with internal SE 46*Ohm* terminations to vcc. Require matching external terminations to vcc.
qn	18		
prbsp	27	CML Output	Differential high-speed output with internal SE 50*Ohm* termination to vcc. Requires a matching external termination to vcc.
			Low-Speed and DC I/Os
i2con	5	3.3*V* CMOS Inputs	I2C/3-wire interface activation input with internal 474*KOhm* pull-down to vee (default – low: 3-wire is on, active – high: I2C is on).
3wenin	31		3-wire interface enable input with internal 474*KOhm* pull-up to vcc
ad5			I^2C DC binary chip address bit, default "1"
3wcin	33		3-wire interface clock input with internal 474*KOhm* pull-down to vee
ad6			I^2C DC binary chip address bit, default "0"
3wdin	1		3-wire interface data input with internal 474*KOhm* pull-down to vee
ad0			I^2C DC binary chip address bit, default "0"
3wdo	3		3-wire interface data output
sda	40		I^2C data input signal
scl	42		I^2C clock input signal
ad1	7		I^2C DC binary chip address bits, default "0"
ad2	9		
ad3	25		
ad4	29		

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
v5p0	+5.0*V* positive power supply Negative pin to vee	11, 23
vee	Ground	12, 22, 34, 44
vcc	+3.3*V* positive power supply Negative pin to vee	2, 4, 6, 8, 10, 13, 15, 17, 19, 21, 24, 26, 28, 30, 32, 35, 37, 39, 41, 43

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Main Supply Voltage (vcc)		3.6	*V*
Additional Supply Voltage (v5p0)		5.5	*V*
RF Input Voltage Swing (SE)		750	*mV*
Case Temperature		+85	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee		0.0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	vcc in relation to vee
v5p0	4.8	5.0	5.3	*V*	v5p0 in relation to vee
I_{v5p0}	4.5		8.0	*mA*	Depending on the state of digital control bytes
I_{vcc}	380		460	*mA*	
Power Consumption	1.2		1.65	*W*	
vcc ramp length			10	*ms*	For reliable SPI preset
Junction temperature	0	50	125	*°C*	
Clock Input (cip/cin)					
Data Rate	DC		32	*GHz*	
Swing	0.15		0.8	*V*	Differential or SE, peak-peak
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Equalized Data Output (qp/qn)					
Data rate	DC		32	*Gb/s*	
Output swing			1000	*mV*	peak-peak, each SE output
CM Level		vcc-0.35		*V*	for DC output termination
Max peaking frequency	20		33	*GHz*	Depending on the digital controls
Peak value	6		34	*dB*	Depending on the digital controls
PRBS Control Data Output (prbsp)					
Data rate	DC		32	*Gb/s*	
Output swing		440		*mV*	peak-peak
CM Level		vcc-0.22		*V*	for DC output termination
Reset Signal (rstnp/rstnn)					
Frequency	DC		15	*GHz*	
Rise time			20	*%*	of the clock period
Recovery time	36			*ps*	
Swing	0.05		0.8	*V*	Differential peak-peak
CM Voltage Level	vcc-0.8		vcc	*V*	
3-Wire Interface					
Clock frequency	0.1		50	*MHz*	
Input low logic level	vee		vee+0.4	*V*	
Input high logic level	vcc-1.3		vcc	*V*	
Output low logic level	vee		vee+0.2	*V*	
Output high logic level	vcc-0.3		vcc	*V*	
Input current			9	*uA*	For each input
I²C Interface					
Clock frequency			3.4	*MHz*	
Input low logic level	vee		vee+0.4	*V*	
Input high logic level	vcc-0.4		vcc	*V*	

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OUTPUT EYE EXAMPLES

Fig. 10 and Fig. 11 demonstrate typical output signal eye diagrams at 20*Gb/s* and 25*Gb/s* respectively.

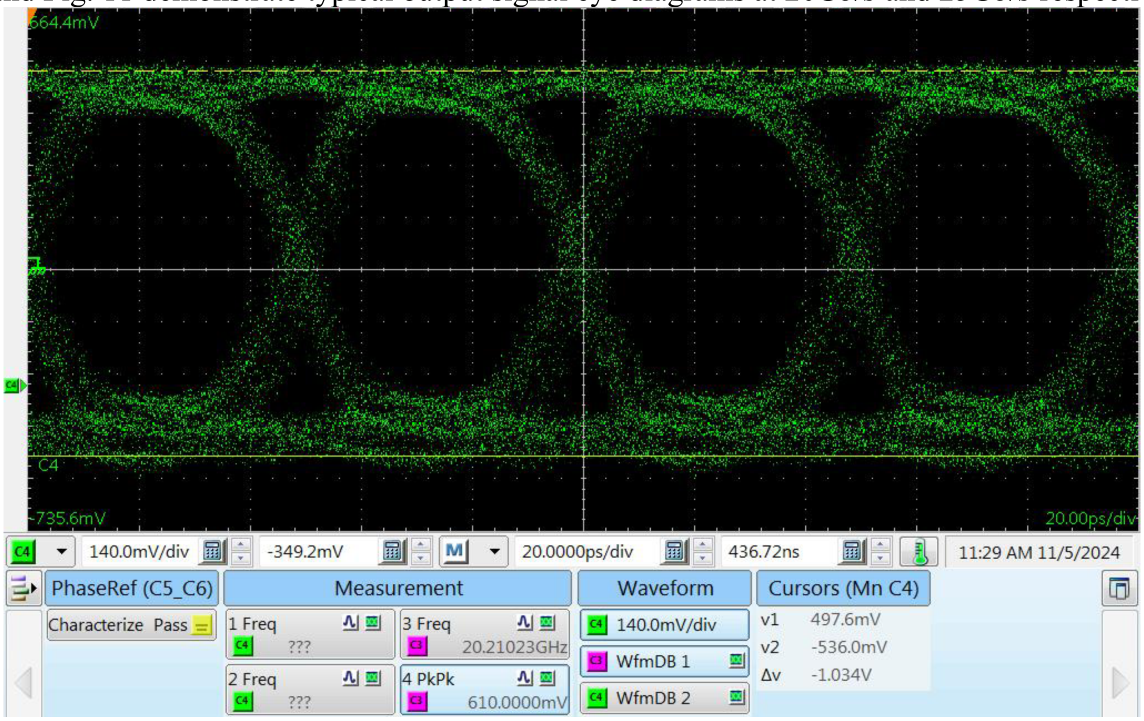

Fig. 10. Output Eye at 20Gb/s

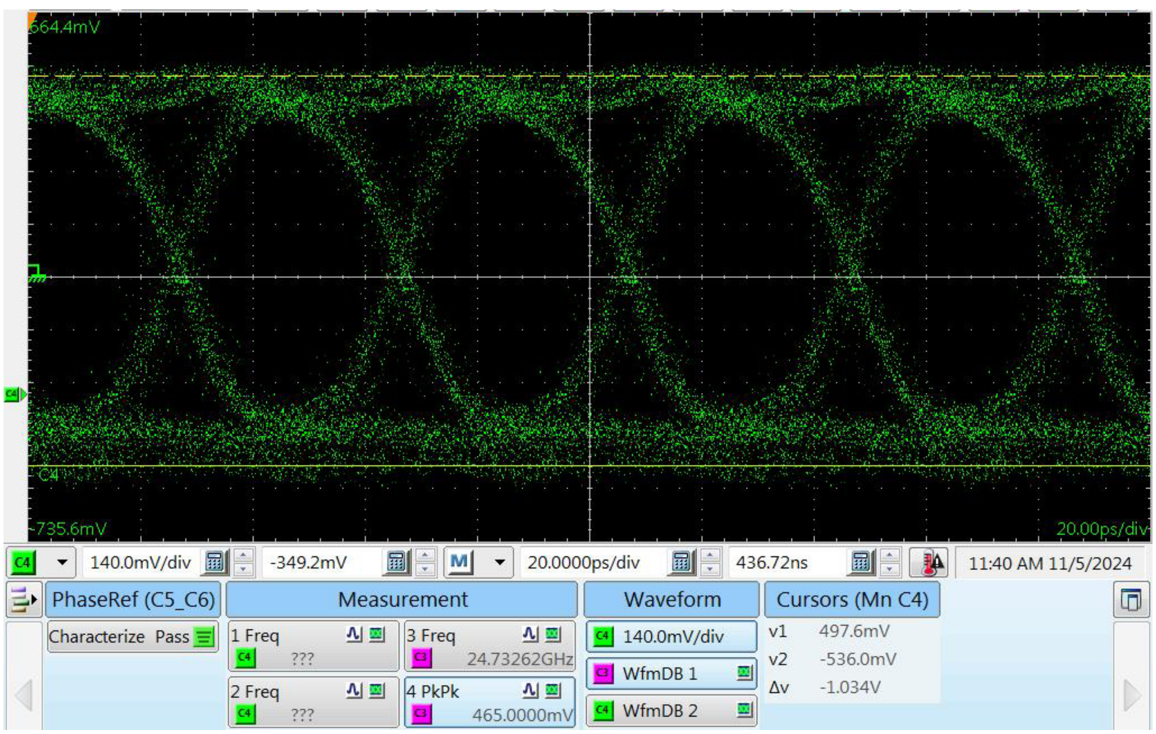

Fig. 11. Output Eye at 25Gb/s

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PACKAGE INFORMATION

The die is housed in a custom, 44-pin CQFP package shown in Fig. 12. The package provides a center heat slug located on the back side of the package to be used for heat dissipation. ADSANTEC recommends using extreme caution when soldering this section to the board to avoid overheating. It should be connected to the vcc plain that is ground for the negative supply, or power for the positive supply.

The part's identification label is ASNT8145-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

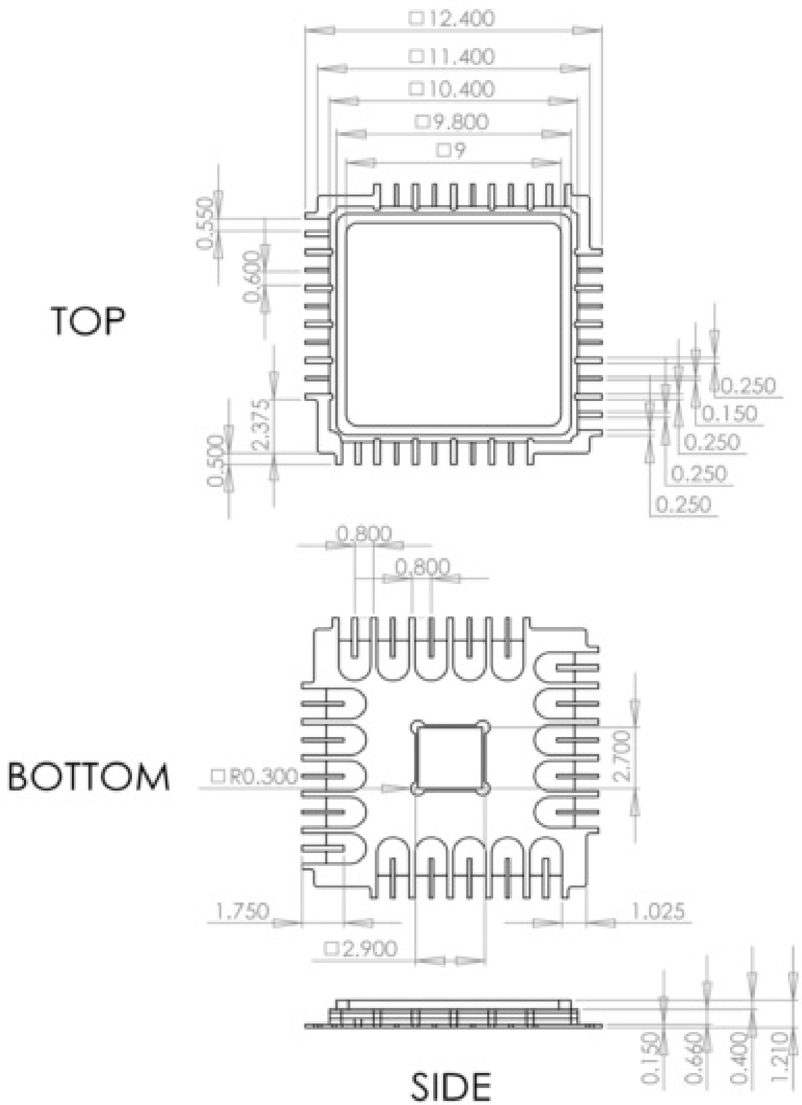

Fig. 12. CQFP44 Package Drawing (All Dimensions in mm)

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This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.1.1	11-2024	Corrected output swing value Output eye diagrams added
1.0.1	10-2024	First release
0.0.1	03-2022	Preliminary release