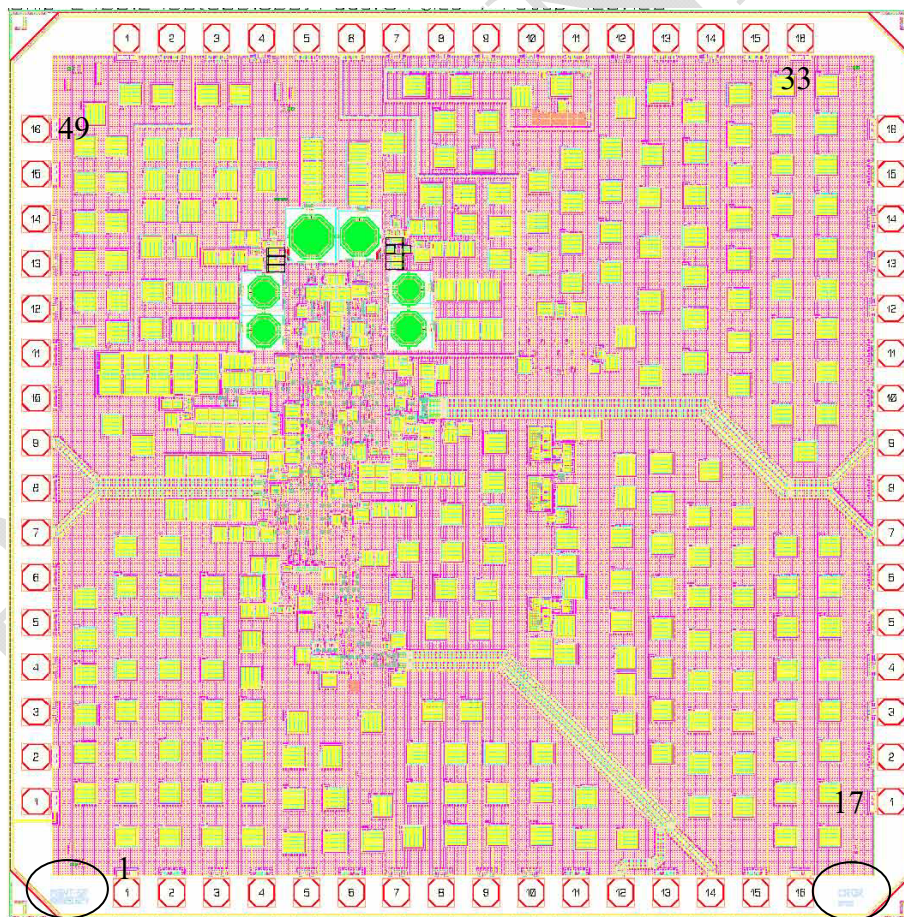




ASNT8762-BD Programmable CR with Peaking Adjustment

- Up to 128Gb/s quarter-rate clock recovery circuit
- Input data range from 80Gb/s to 128Gb/s
- NRZ and PAM4 input data format
- Input data and output clock peaking adjustment
- CML compliant differential input and output high-speed data and clock interfaces
- CML compliant differential input reference clock interface
- Quarter-rate clock output up to 32GHz for a 128Gb/s input data signal
- Single +3.3V or -3.3V power supply
- Power consumption of 2.2W at the maximum operational speed
- Industrial temperature range
- Bare die



Text markings

Text markings

DESCRIPTION

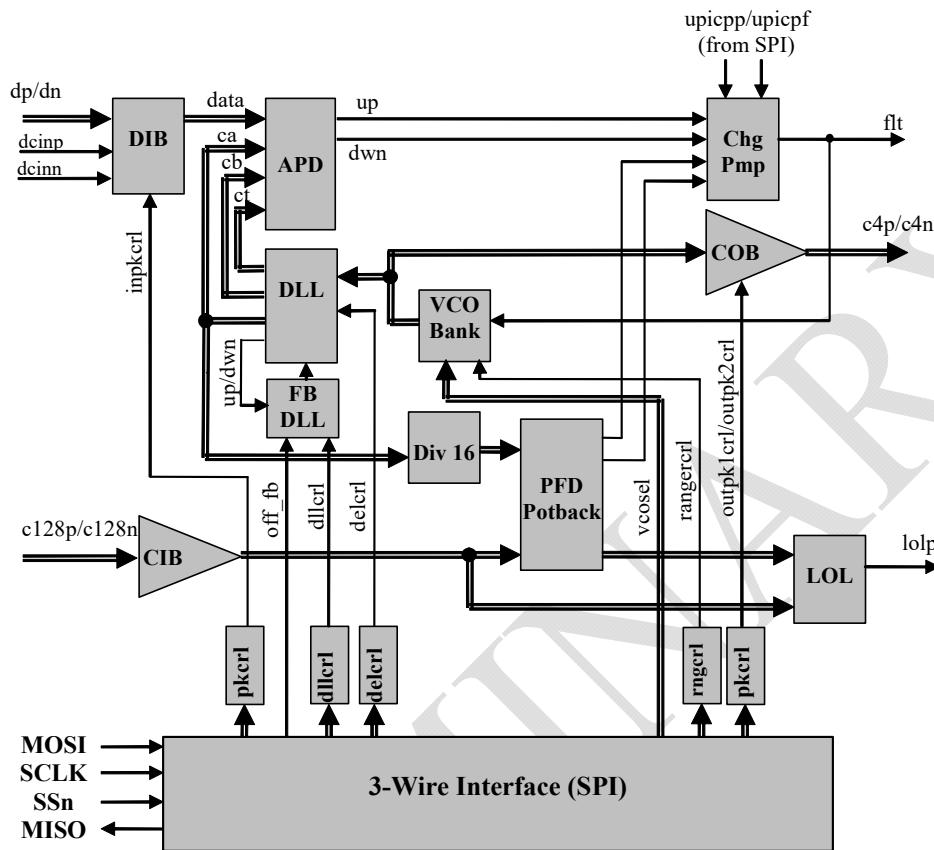


Fig. 1. Functional Block Diagram

This part is a quarter-rate integrated clock recovery (CR) circuit. The IC shown in Fig. 1 covers a wide range of input data rates (f_{bit}) by utilizing its six on-chip VCOs (voltage-controlled oscillators). To reduce the physical number of control inputs to the chip, a shift register with a 3-wire input interface (SPI) has been included on chip. The SPI block provides all the digital controls for the chip. It also provides digital controls for digital-to-analog converters (DACs) that handle internal analog DC voltage adjustments.

Selection of the desired working data rate of the CR is accomplished through the digital control $vcosel$ (see Table 2). An external low-speed system clock $c128p/c128n$ running at 1/32 the frequency of the active VCO must be applied to the low-speed clock input buffer (CLK IB).

The main function of the chip is to recover from an NRZ or PAM4 input data signal dp/dn with a bit rate of f_{bit} accepted by CML buffer (Data IB) a quarter-rate clock $c4p/c4n$ that is delivered to the output by the CML clock output buffer (COB). For example, a 28GHz clock signal will be generated from a 112Gb/s input data signal.

The internal DLL feedback circuit automatically adjusts phases of internal clock signals that are required in the phase detector for correct clock recovery. If needed, the automatic feedback can be disabled by the digital bit fb_off of SPI. In the manual mode ($fb_off=“1”$), the digital bytes of SPI $dllcr1$ and $delcr1$ can be used to set delays between phases of the internal clock signals manually.



Data IB can operate with either differential or single-ended input signals. The buffer can provide a controlled peaking for the input signal (through the SPI). The buffer also includes tuning pins `dcinp/dcinn` for DC offset of the input signals in case of AC termination. When the buffer is operating with a DC-terminated single-ended input signal, a correct threshold voltage should be applied to the unused input pin.

All CML I/Os provide on chip 50Ω termination to `VCC` and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION).

A loss of lock CMOS alarm signal `lolp` is generated by the CR to indicate its locking state. An off chip passive filter is required by the CR, and should be connected to pin `flt` (see Core section).

The clock recovery circuit is characterized for operation from 0°C to 125°C of junction temperature. The package temperature resistance is $15^{\circ}\text{C}/\text{W}$.

Data IB

The Data Input Buffer (Data IB) can process an input CML data signal `dp/dn` in NRZ or PAM4 format. It provides on-chip single-ended termination of 50Ω to `VCC` for each input line. The buffer can also accept a single-ended signal to one of its input ports `dp`, or `dn` with a threshold voltage applied to the unused pin in case of DC termination. In case of AC termination, tuning pins `dcinp/dcinn` allow for data common mode adjustment. The tuning pins have $1\text{K}\Omega$ terminations to `VCC`, and allow the user to change the slicing level before the data is sent to the clock recovery section. Tuning voltages from `VCC` to `VEE` deliver 150mV of DC voltage shift. SPI digital control byte `inpkrl` may be used to linearly control DC currents of the input emitter followers. Higher values of the control result in greater peaking of the signal at the input of the phase detector. Fig. 2 shows the dependence of DC currents of two input emitter followers on the control `inpkrl`.

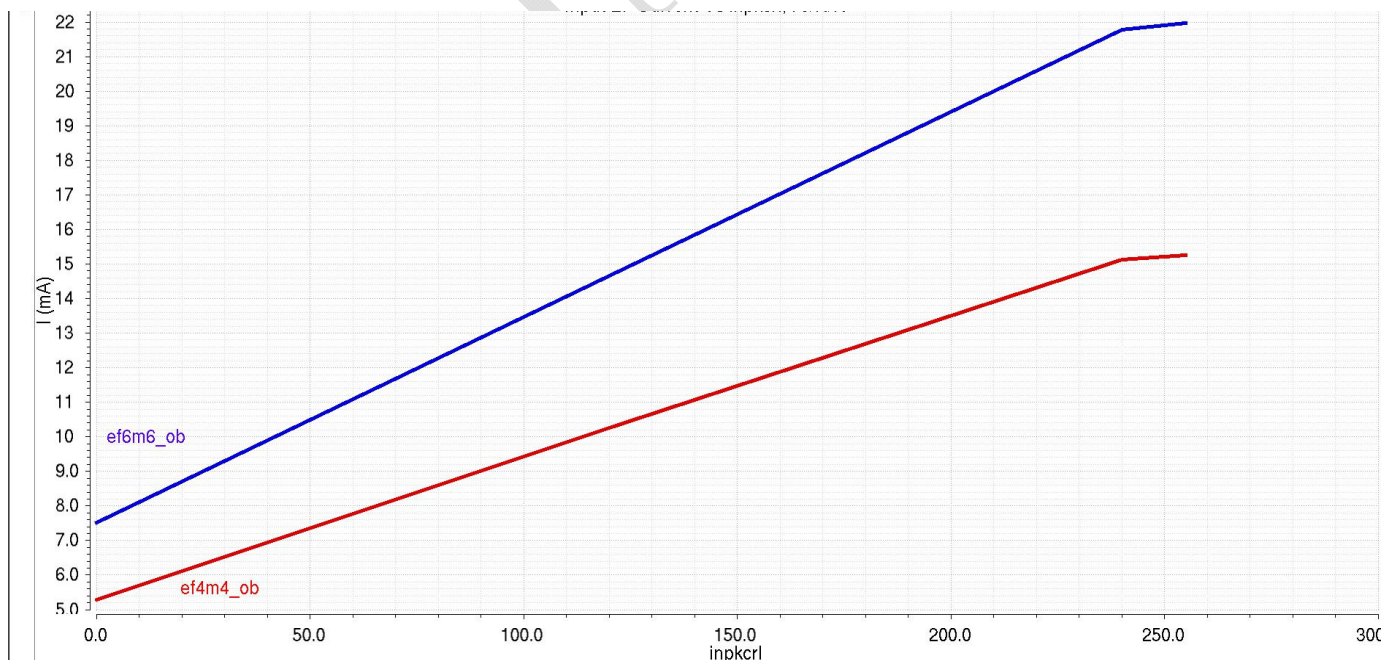


Fig. 2. Input EF Current Vs `inpkrl`

CLK IB

The Clock Input Buffer (CLK IB) is a CML differential buffer with a 50Ω single-ended termination to VCC at each of the two input pins. The buffer is designed to accept reference clock signals with a speed up to 1.4GHz.

DLL

The purpose of the internal delay-locked loop (DLL) block is to automatically adjust phase delays of the three copies of the clock, generated by VCO, which are used by the core of the chip to match output clock frequency to precisely quarter-rate of the input data. For normal operation, the DLL should remain in automatic mode (`off_fb="0"`) and the byte `delcrl` should remain at its default value of 0. If needed, the byte `delcrl` can be used to adjust the delay between the first and the second clock signals. Fig. 3 shows the control range of the middle clock generated by DLL.

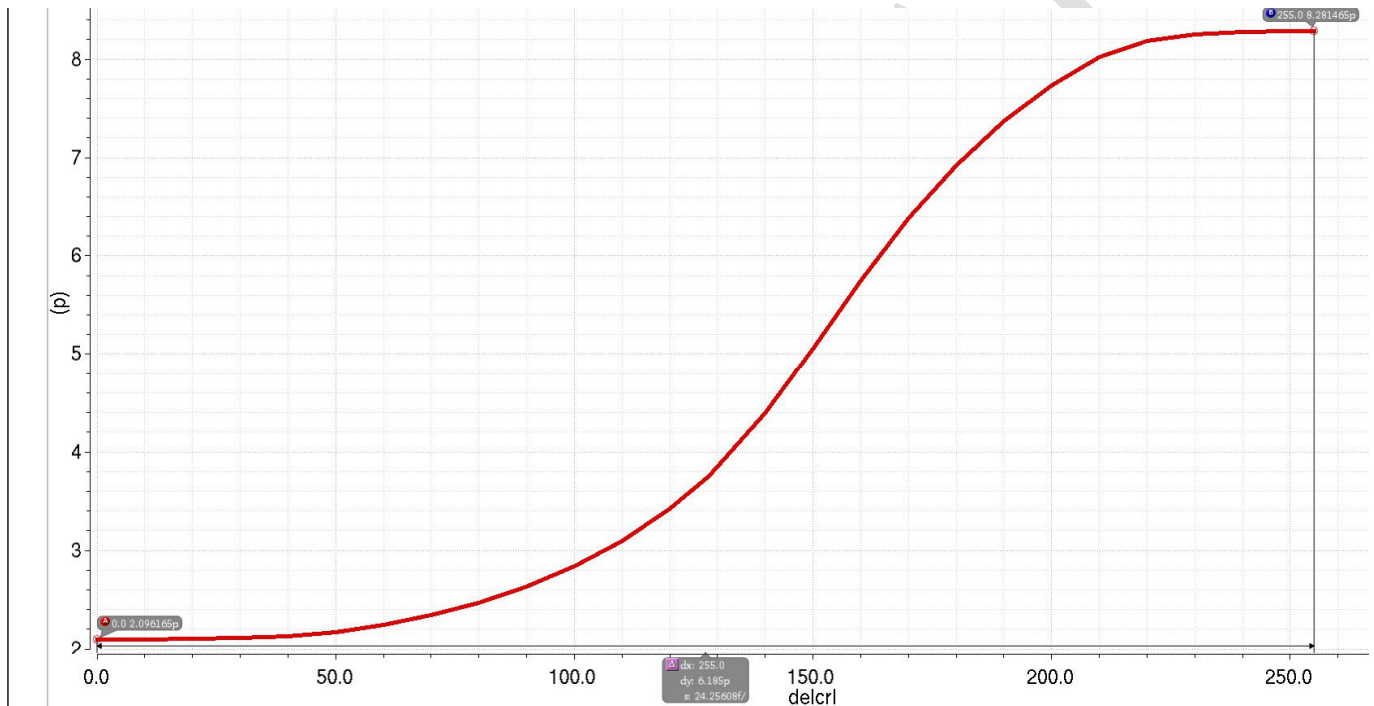


Fig. 3. Delay between 1st and 2nd DLL Clock Signals Vs `delcrl`

Also, the DLL can be switched into manual mode (`off_fb="1"`), in which the phase delay between the first and the third internal clock signals can be manually adjusted through the digital control byte `dllcrl`. Fig. 4 shows the dependence of phase delay between the 1st and the 3rd DLL clock signals on the control `dllcrl` when automatic feedback is off.

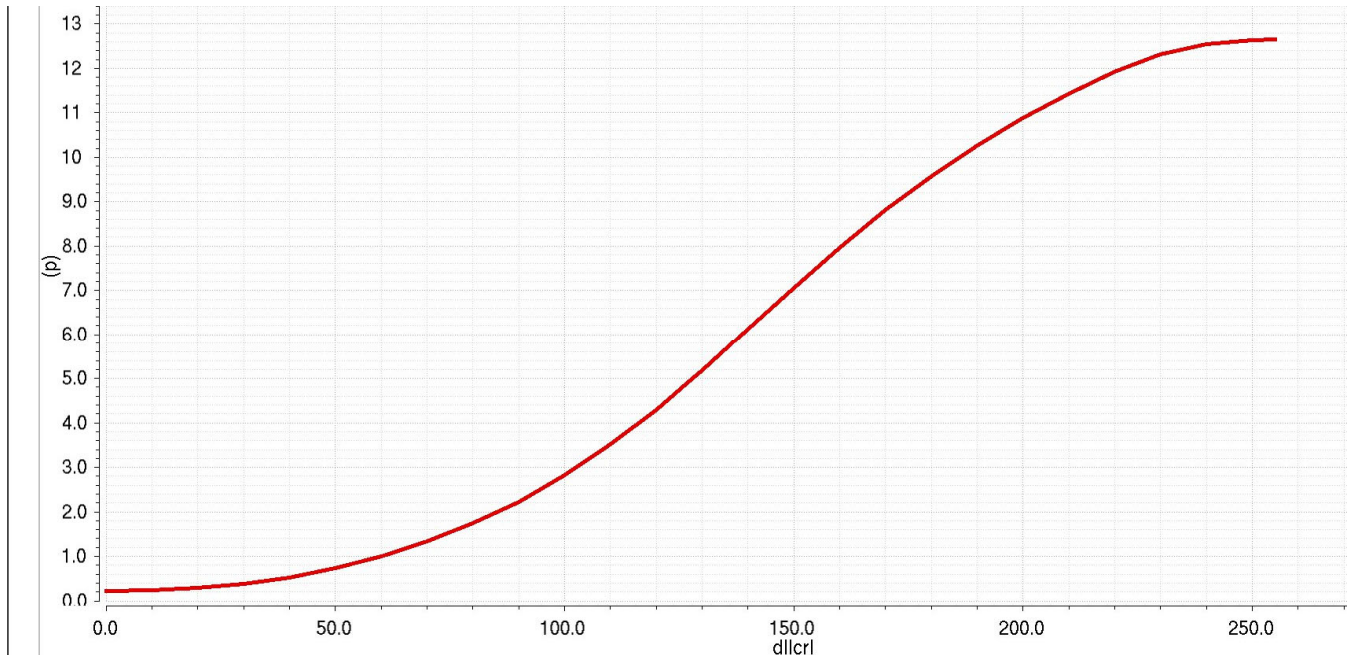


Fig. 4. Delay between 1st and 3rd DLL Clock Signals Vs dllcr1

Core

The main function of the clock recovery (CR) core is to frequency-lock the selected on-chip VCO to the input data signal. The CR core contains a phase acquisition loop, and a frequency acquisition loop. The phase acquisition loop includes a high-speed Alexander Phase Detector (APD) that processes the input data stream dp/dn , and three shifted clock signals that are provided by DLL. The frequency loop consists of a clock divider-by-16, and a PFD Potback block. The frequency acquisition loop works in concert with low-speed clock $c128p/c128n$. Both acquisition loops generate signals that control a single charge pump. The charge pump in combination with a filter generates an analog signal that controls the active VCO. The on-chip filter is small, so the CR requires a single off-chip filter shown in Fig. 5 to be connected to pin flt .

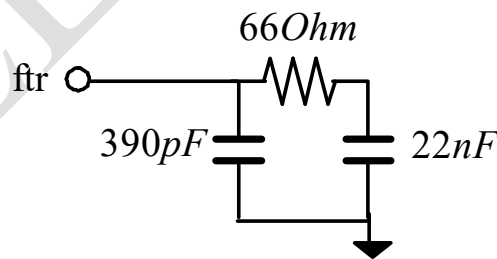


Fig. 5. External Loop Filter

By utilizing the 3-bit digital control $vcosel$, the desired working frequency of the CR can be selected in accordance with Table 1 below.



Table 1. CR Mode Selection

vcosel<2>	vcosel<1>	vcosel<0>	vco #	Frequency Range (GHz)
0	0	0	-	-
0	0	1	1	$f_{min}=17.9, f_{max}=21.1$
0	1	0	2	$f_{min}=20.8, f_{max}=24.6$
0	1	1	3	$f_{min}=23.8, f_{max}=28$
1	0	0	4	$f_{min}=26.9, f_{max}=31.4$
1	0	1	5	$f_{min}=30.2, f_{max}=35$
1	1	0	6	$f_{min}=33.6, f_{max}=38.1$
1	1	1	-	-

The loop gain can be adjusted by two control bits `upicpp` and `upicpf` that control the charge pump current as shown in Table 2.

Table 2. CR Mode Selection

0	0	$I_{max}-0.31$
0	1	$I_{max}-0.27$
1	0	$I_{max}-0.04$
1	1	I_{max}

By utilizing the control byte `rangectrl`, the DC current of the control emitter follower of the active VCO can be adjusted linearly. Higher values of the control result in higher emitter follower currents. Higher emitter follower currents result in a more linear VCO frequency dependence on the control voltage at the expense of the frequency range.

The lock detect circuitry signals an alarm through the 1.2V CMOS signal `lolp` when a frequency difference exists between an applied system reference clock `c128p/c128n`, and a recovered quarter-rate clock divided-by-32 that is greater than $\pm 1000ppm$. When the signal is at level "0" output clock is locked to input data. When it is at level "1" there is no lock.

COB

The Clock Output Buffer (COB) receives a quarter-rate clock signal from CR, and converts it into CML output signal `c4p/c4n`. The buffer requires 50Ohm external termination resistors connected between `vcc`, and each output (usually supplied by the downstream chip that the buffer is driving). SPI digital control bytes `outpk1ctrl`, and `outpk2ctrl` may be used to linearly control DC currents of the two emitter followers of the COB. Higher values of the control result in greater peaking of the output signal.

Fig. 6 shows the dependence of DC current of the 1st output emitter follower on the control `outpk1ctrl`. Fig. 7 shows the dependence of DC current of the 2nd output emitter follower on the control `outpk2ctrl`.

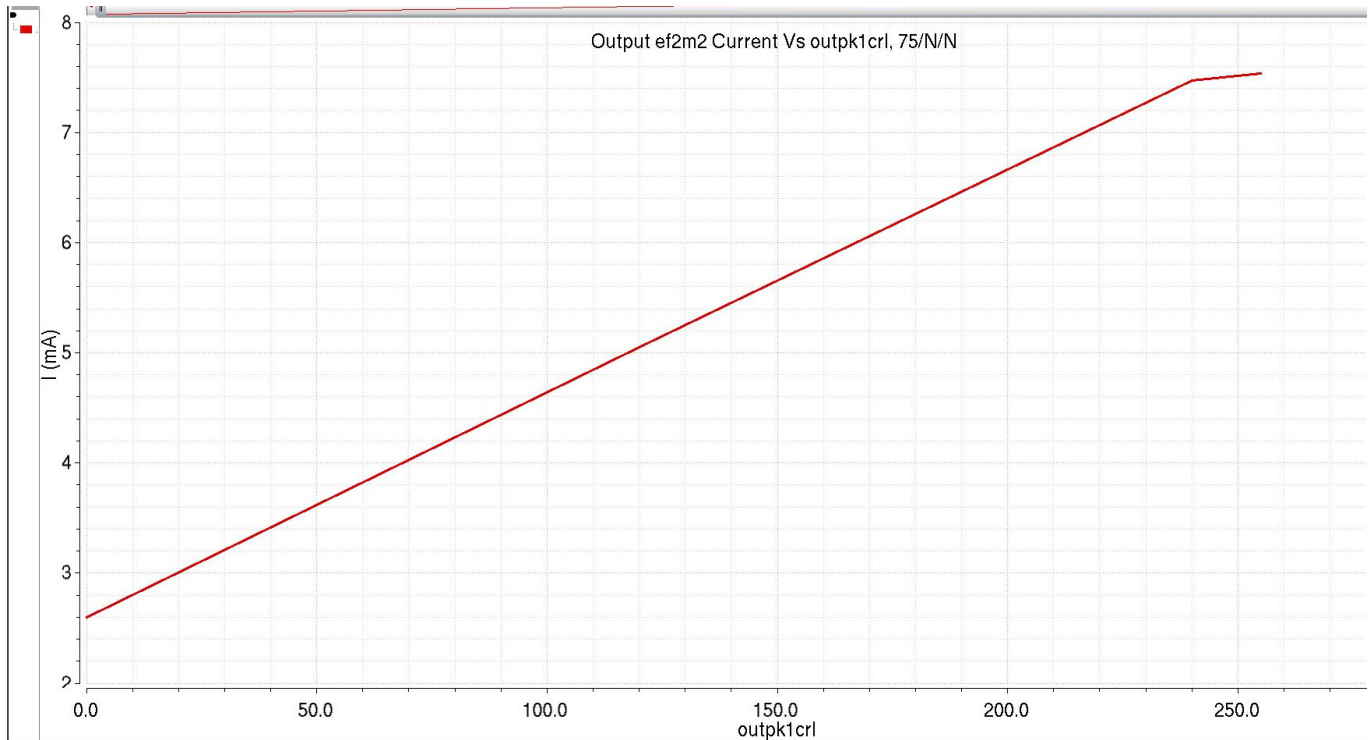


Fig. 6. DC Current of the 1st Output Emitter Follower Vs output1crl

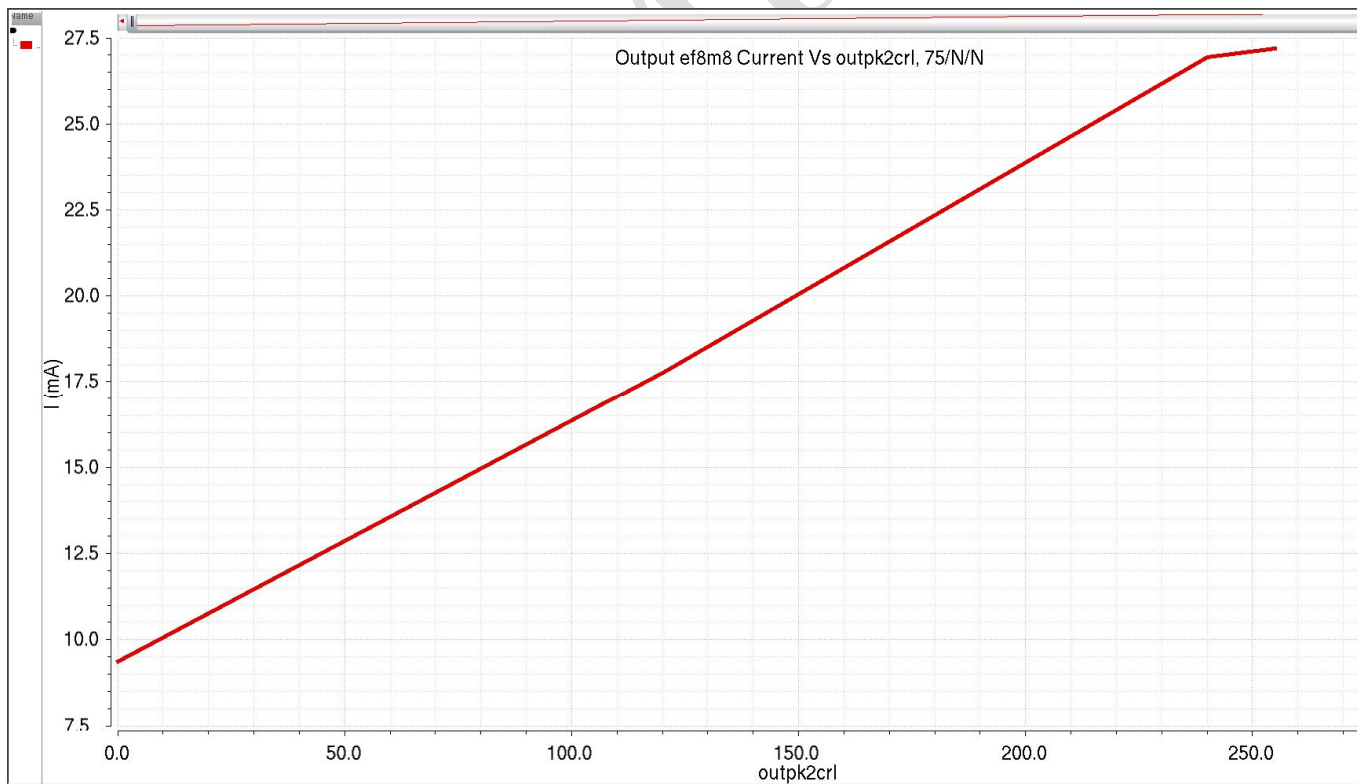


Fig. 7. DC Current of the 2nd Output Emitter Follower Vs output2crl



3-Wire Interface Control Block

To reduce the physical number of control inputs to the chip, a 7-byte shift register with a 3-wire input interface has been included on chip. The SPI block is powered by an internally generated supply voltage of +1.2V from **vee**. The digital control bits applied through MOSI input are latched in, and shifted down the register with clock SCLK. Write enable signal **SSn** must be set to logic “0” during the data read-in phase. The SPI data can be monitored through the output MISO. Table 3 presents the byte order of the 3-wire interface block.

Table 3. Control Bytes

Byte Number	Bit Number							
	7	6	5	4	3	2	1	0
1	vcosel(2:0)			X	X	upicpf	off_fb	upicpp
2	delcrl(7:0)							
3	inpkcrl(7:0)							
4	rangecrl(7:0)							
5	outpk2crl(7:0)							
6	outpk1crl(7:0)							
7	dllcrl(7:0)							

The SPI load order is illustrated in Fig. 8.

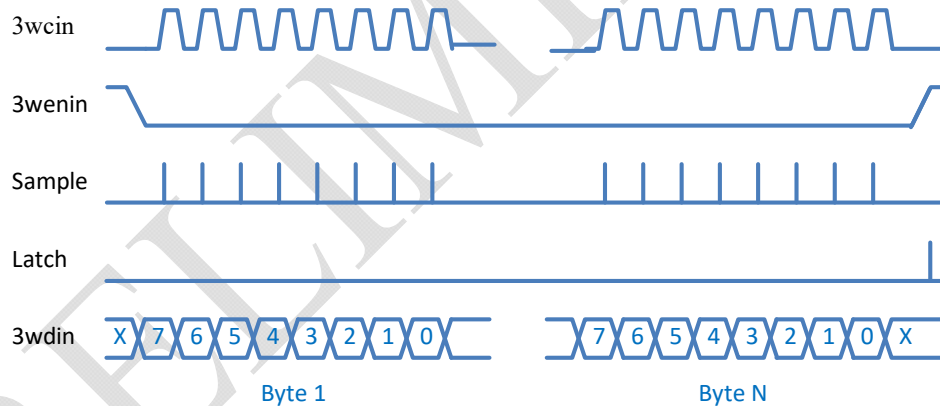


Fig. 8. SPI Load Order

POWER SUPPLY CONFIGURATION

The ASNT8762-KMF can operate with either a negative supply (**vcc** = 0.0V = ground, and **vee** = -3.3V), or a positive supply (**vcc** = +3.3V, and **vee** = 0.0V = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50Ohms termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 3.3V and vee = 0V (external ground)



ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 4 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed **vee**).

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (VCC)		+3.8	V
Power Consumption		2.2	W
Input Voltage Swing (SE)		1.0	V
Die Temperature ^{*)}		+125	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

Table 5. Chip Pad Names

Chip Pad No.	Function	Chip Pad No.	Function	Chip Pad No.	Function	Chip Pad No.	Function
1	vee	17	vee	33	vee	49	vee
2	vcc	18	vcc	34	vcc	50	vee
3	n/c	19	n/c	35	n/c	51	n/c
4	vcc	20	n/c	36	vcc	52	n/c
5	n/c	21	vcc	37	n/c	53	dcinp
6	vcc	22	vcc	38	vcc	54	vcc
7	n/c	23	c4n	39	SSn	55	vcc
8	flt	24	vcc	40	SCLK	56	dp
9	n/c	25	c4p	41	MOSI	57	vcc
10	lolp	26	vcc	42	MISO	58	dn
11	vcc	27	vcc	43	vcc	59	vcc
12	c128p	28	n/c	44	vcc vco	60	vcc
13	vcc	29	n/c	45	n/c	61	dcinn
14	c128n	30	n/c	46	vcc vco	62	n/c
15	vcc	31	vcc	47	vcc	63	vee
16	vee	32	vee	48	vee	64	vee



Table 6. Terminal Functions

Pad			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
c4p	25	Output	CML differential quarter-rate clock outputs. Require external SE 50Ohm termination to VCC
c4n	23		
dp	56	Input	CML differential data inputs with internal SE 50Ohm termination to VCC
dn	58		
Low-Speed I/Os			
c128p	12	Input	CML differential clock inputs with internal SE 50Ohm termination to VCC
c128n	14		
SSn	39	1.2V CMOS input	Enable input signal for 3-wire interface
SCLK	40		Clock input signal for 3-wire interface
MOSI	41		Data input signal for 3-wire interface
MISO	42	1.2V CMOS output	Data output signal of 3-wire interface
lolp	10	1.2V CMOS output	Loss-of-lock signal
Controls			
dcinp	53	LS IN	Input data common mode voltage adjustment
dcinn	61		
flt	8	I/O	External CR filter connection

Supply and Termination Voltages		
Name	Description	Pin Number
vcc	Positive power supply (+3.3V)	2, 4, 6, 11, 13, 15, 18, 21, 22, 24, 26, 27, 31, 34, 36, 38, 43, 45, 47, 54, 55, 57, 59, 60
vcc_vco	Positive power supply for VCO (+3.3V)	44, 46
vee	Negative power supply (GND or 0V)	1, 16, 17, 32, 33, 48, 49, 50, 63, 64
nc	Not connected pins	3, 5, 7, 9, 19, 20, 28, 29, 30, 35, 37, 51, 52, 62



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.0	+3.3	+3.6	V	±9%
vee		0.0		V	
I _{vcc}		655		mA	All functions active
Power Consumption		2.2		W	
Junction Temperature	-25	50	125	°C	
Case temperature			75	°C	Recommended value
HS Input Data (dp/dn)					
Data Rate	80		128	Gbps	NRZ
Swing p-p (Diff or SE)	0.3		0.6	V	
CM Voltage Level	vcc-0.8		vcc	V	
LS Input Reference Clock (c128p/c128n)					
Frequency	0.625		1.0	GHz	For LOL operation it must be ±10KHz from the selected VCO frequency
Swing p-p (Diff or SE)	0.3		0.6	V	
CM Voltage Level	vcc-0.8		vcc	V	
Duty Cycle	40	50	60	%	
HS Output Quarter-rate Clock (c4p/c4n)					
Clock Rate	20		32	GHz	80 to 128Gbps input
Logic "1" level		vcc		V	
Logic "0" level	vcc -0.6		vcc -0.15	V	
Jitter		5	8	ps	p-p
Input Data Common Mode Control (dcinp/dcinn)					
Input DC Voltage	vee		vcc	V	
Input Data Voltage Shift	0		-150	mV	Referenced to vcc
3-Wire Inputs (3wdin, 3wcin, 3wenin)					
High voltage level	vee+1.1		vee+1.35	V	
Low voltage level	vee		vee+0.35	V	
Clock speed		350	400	MHz	

DIE INFORMATION

The chip die has 11mills (0.28)mm thickness and 2.43 x 2.43mm² external dimensions. Its pad frame contains 44 octagonal pads with metal dimensions of 80 x 80μm² and 74 x 74μm² pad openings. The pad coordinates in relation to the chip's bottom-left corner are presented in Table 7.



Table 7. Chip Pad Coordinates

<i>Chip Pad No.</i>	<i>X mkm</i>	<i>Y mkm</i>	<i>Chip Pad No.</i>	<i>X mkm</i>	<i>Y mkm</i>
1	315	72	33	2115	2358
2	435	72	34	1995	2358
3	555	72	35	1875	2358
4	675	72	36	1755	2358
5	795	72	37	1635	2358
6	915	72	38	1515	2358
7	1035	72	39	1395	2358
8	1155	72	40	1275	2358
9	1275	72	41	1155	2358
10	1395	72	42	1035	2358
11	1515	72	43	915	2358
12	1635	72	44	795	2358
13	1755	72	45	675	2358
14	1875	72	46	555	2358
15	1995	72	47	435	2358
16	2115	72	48	315	2358
17	2358	315	49	72	2115
18	2358	435	50	72	1995
19	2358	555	51	72	1875
20	2358	675	52	72	1755
21	2358	795	53	72	1635
22	2358	915	54	72	1515
23	2358	1035	55	72	1395
24	2358	1155	56	72	1275
25	2358	1275	57	72	1155
26	2358	1395	58	72	1035
27	2358	1515	59	72	915
28	2358	1635	60	72	795
29	2358	1755	61	72	675
30	2358	1875	62	72	555
31	2358	1995	63	72	435
32	2358	2115	64	72	315

REVISION HISTORY

Revision	Date	Changes
1.0.1	11-2024	Preliminary release