ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Dr., Ste #112, Torrance, CA 90505

Office: (310) 530-9400 Fax: (310) 530-9402
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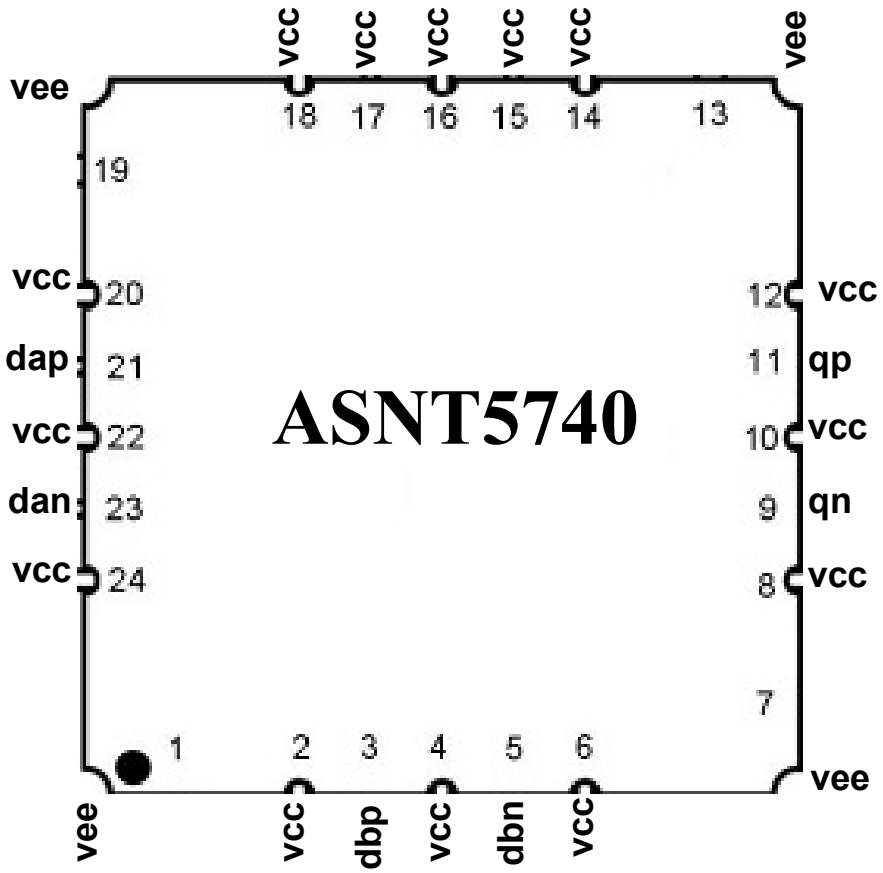
ASNT5740-KHC
DC - 64*Gbps* XOR Logic Gate

- High speed broadband Exclusive-OR (XOR) Boolean logic gate
- Fully differential CML input interfaces
- Fully differential CML output
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 345 *mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom 24-pin CQFN package



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DESCRIPTION

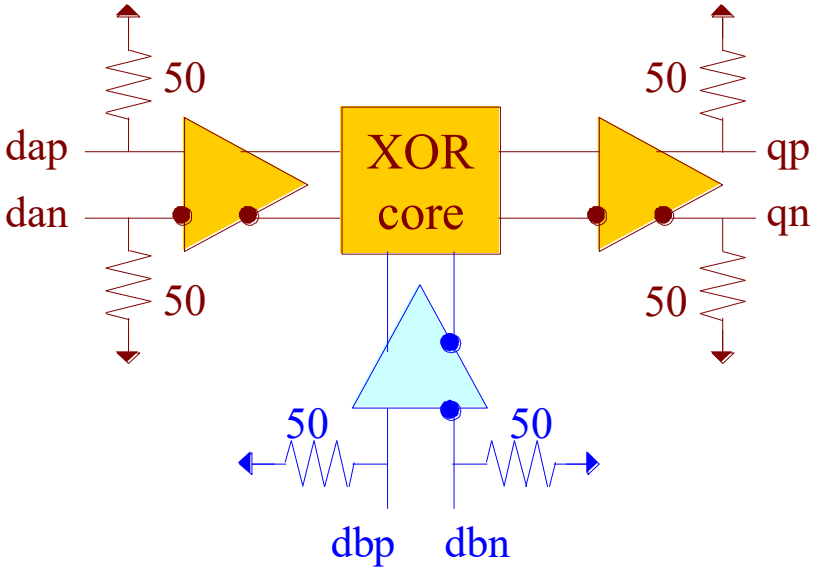

Fig. 1. Functional Block Diagram

This SiGe IC provides broadband Exclusive-OR (XOR) Boolean logic functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can perform an XOR operation with a high-speed data or clock input signal dap/dan and another high-speed data or clock input signal dbp/dbn. The resulting high-speed output signal is delivered to the output port qp/qn. If the input signals have a half bit or half period phase shift, the resulting output signal will be at double-rate or double-frequency.

The part's inputs and outputs support the CML logic interface with on chip 50*Ohm* termination to vcc, and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS.

In the input AC-coupling mode, the input termination provides the required common mode voltage automatically. In this case, the output can be used in DC-coupling mode and its common mode voltage can be adjusted using floating power supplies as described in the POWER SUPPLY CONFIGURATION section below.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0 *V* = ground), or positive supply (vee = 0.0 *V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0 *V* and vee = -3.3 *V*.

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dap	21	CML input	Differential data/clock inputs with internal SE 50*Ohm* termination to vcc
dan	23		
dbp	3	CML input	Differential data/clock inputs with internal SE 50*Ohm* termination to vcc
dbn	5		
qp	11	CML output	Differential data outputs with internal SE 50 *Ohm* termination to vcc. Require external SE 50 *Ohm* termination to vcc.
qn	9		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply. (+3.3 *V* or 0)		2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24
vee	Negative power supply. (0 *V* or -3.3 *V*)		1, 7, 13, 19

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Positive supply voltage (vcc)	0	3.6	*V*
Negative supply voltage (vee)	vcc-3.6	0	*V*
RF Input voltage swing (SE)		0.8	*V*
Case temperature		+100	*°C*
Storage temperature	-40	+100	*°C*
Operational/storage humidity	10	98	*%*

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc		0.0		*V*	External ground
vee	-3.47	-3.3	-3.14	*V*	±5%
*I*vcc		105		*mA*	
Power consumption		345		*mW*	
Junction temperature	-40		125	*°C*	
HS Input Data (dap/dan, dbp/dbn)					
Data rate	0.0		64	*Gbps*	
	0.0		38	*GHz*	For 50% duty cycle signals
Voltage swing, pk-pk	50	400		*mV*	Single ended, unused input not connected or AC terminated
CM Voltage Level	vcc-0.4		vcc-sw/2	*V*	Must match for both inputs
Input return loss		TBD		*dB*	In bandwidth
HS Output Data (qp/qn)					
Data rate	0.0		64	*Gbps*	
	0.0		56	*GHz*	For 50% duty cycle signals in XOR mode, output swing down to 100*mV*
Logic “1” level	vcc-0.05	vcc-0.03	vcc-0.01	*V*	
Logic “0” level	vcc-0.46	vcc-0.44	vcc-0.42	*V*	With external 50*Ohms* DC termination
Latency	35		48	*ps*	
Rise/Fall time			8	*ps*	
Jitter for 50% duty cycle signals			1.1	*ps*	Peak-to-peak at 64*Gbps*; Buffer mode
			1.8	*ps*	Peak-to-peak at 64*Gbps*; XOR mode
Output return loss		TBD		*dB*	In bandwidth

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MEASURED DATA

The following screenshots present output eyes with an input signal applied to one differential input port and a DC signal applied to the other differential input port.

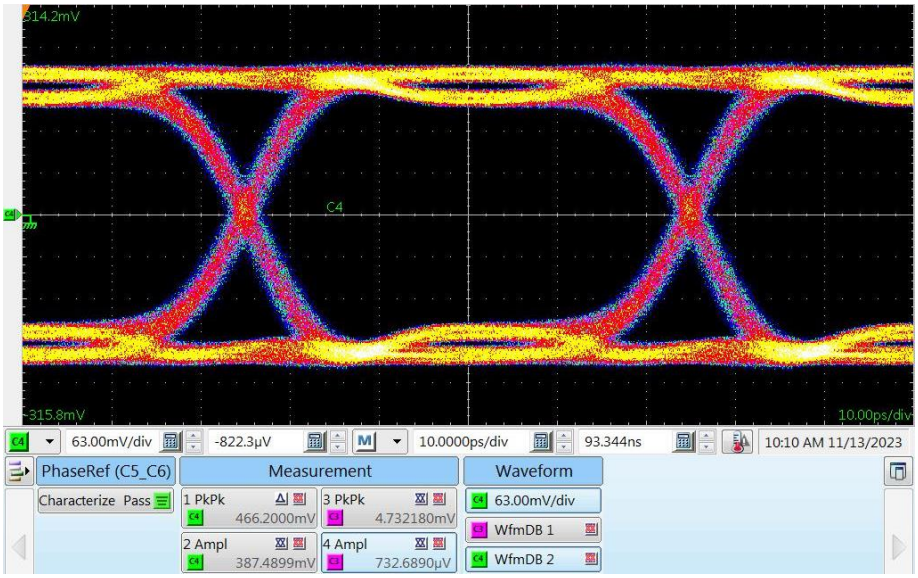

Fig. 2. 20Gb/s Output PRBS Signal

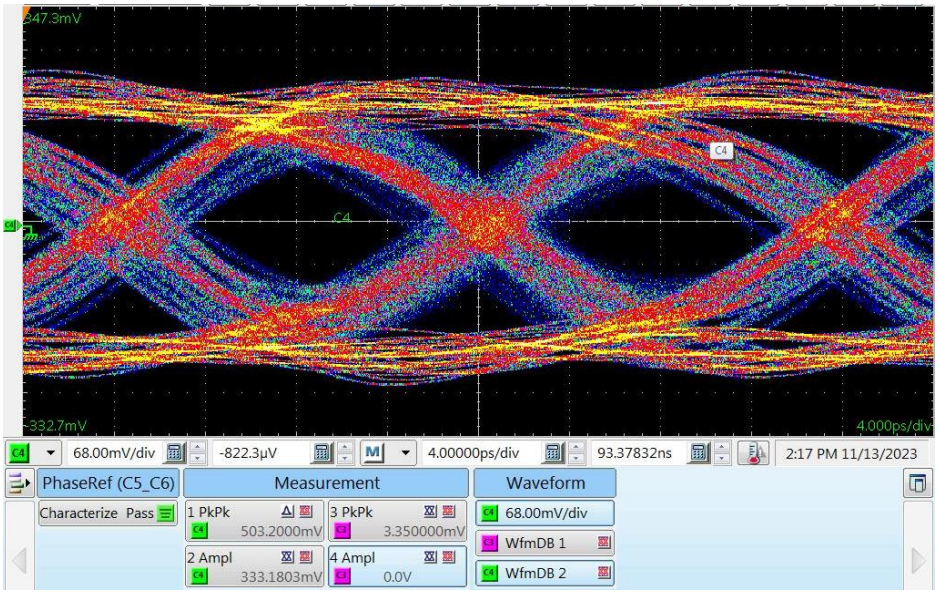

Fig. 3. 64Gb/s Output PRBS Signal

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PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFN package shown in Fig. 4. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5740-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

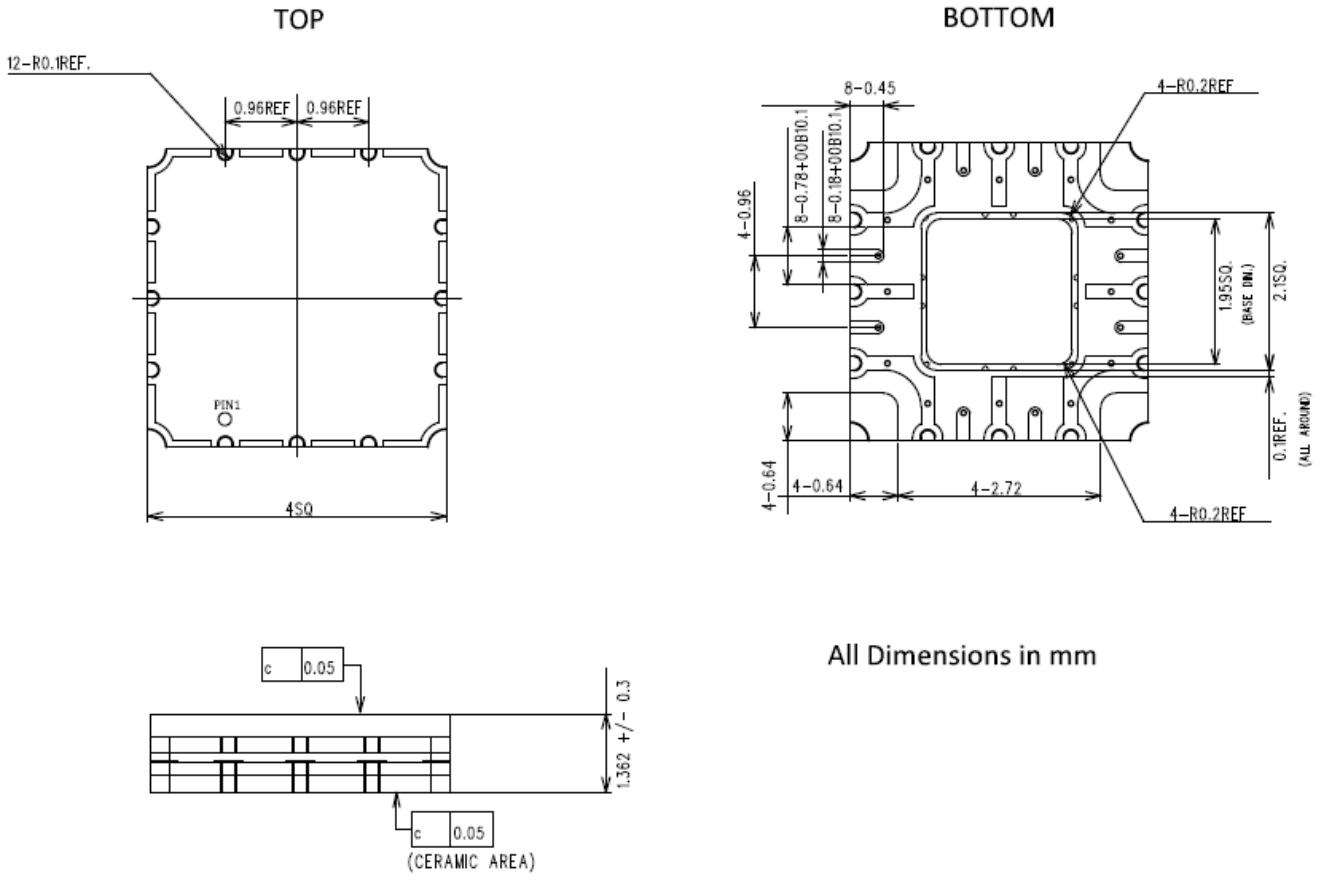

Fig. 4. CQFN 24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.2.2	05-2026	Updated Electrical Characteristics
1.1.2	04-2025	Updated format
1.1.1	04-2025	Added latency information
1.0.1	11-2024	First release.
0.0.1	02-2023	Preliminary release