ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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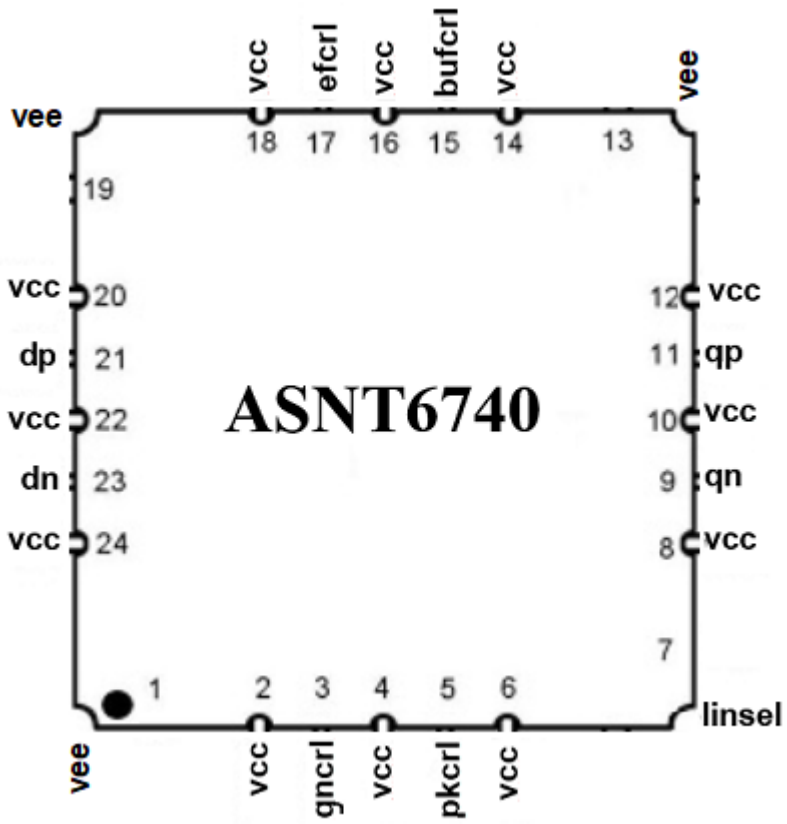
ASNT6740-KHC
DC-34*GHz* Analog Amplifier, -8*dB* to 19*dB* Gain

- DC to 34*GHz* broadband analog amplifier
- Exhibits an extra-flat frequency response ideal for PAM3 and PAM4 applications
- Differential CML-type input/output interfaces
- Single ended output linearity range up to $0.75V_{pk\text{-}pk}$ and differential output linearity up to $1.5V_{pk\text{-}pk}$
- Adjustable gain from -8*dB* to 19*dB*
- Adjustable high-frequency peaking
- Adjustable internal currents for power consumption and bandwidth control
- Single +3.6*V* or -3.6*V* power supply
- Power consumption: 900*mW* typical
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFN 24-pin package



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DESCRIPTION

The temperature stable ASNT6740-KHC analog amplifier is intended for use in any applications demanding high gain, bandwidth, and linearity while maintaining low noise and power consumption. Its extra-flat frequency response is ideal for PAM3 and PAM4 signals. The IC shown can receive a broad-band analog signal at its differential input dp/dn and return an amplified output at differential pins qp/qn with gain of up to 19*dB*. Low-speed analog control gncrl is available for gain adjustment from -8dB to 19dB. Digital control linsel allows to choose between higher-gain/lower-linearity and lower-gain/higher-linearity modes. Low-speed analog current controls efcrl and bufcrl are available for power consumption and bandwidth adjustments. A low-speed analog control pkcrl is available for peaking adjustments at higher frequencies (above 25*GHz*). A relatively flat frequency response with variation of no more than ±0.5*dB* within DC-to-34*GHz* can be achieved with these control voltages.

The part's I/O's support the CML logic interface with on chip 50*Ohms* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically.

For optimal performance, DC coupling is recommended for the output data ports!

For most applications, the recommended values of efcrl and bufcrl for the optimal output eye quality are shown below. However, deviating from these settings may be beneficial for some signals.

Table 1. Recommended values of efcrl and bufcrl

Control Voltage	Recommended Min.	Recommended Max.	Optimal
efcrl	vee + 2.1*V*	vcc	vee + 2.1*V*
bufcrl	vee + 2.05*V*	vee + 2.2*V*	vee + 2.1*V*

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.6*V*), or positive supply (vcc = +3.6*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.6*V*.

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TYPICAL PERFORMANCE CHARACTERISTICS

At default values, the frequency responses of the ASNT6740-KHC are shown in Fig. 1.

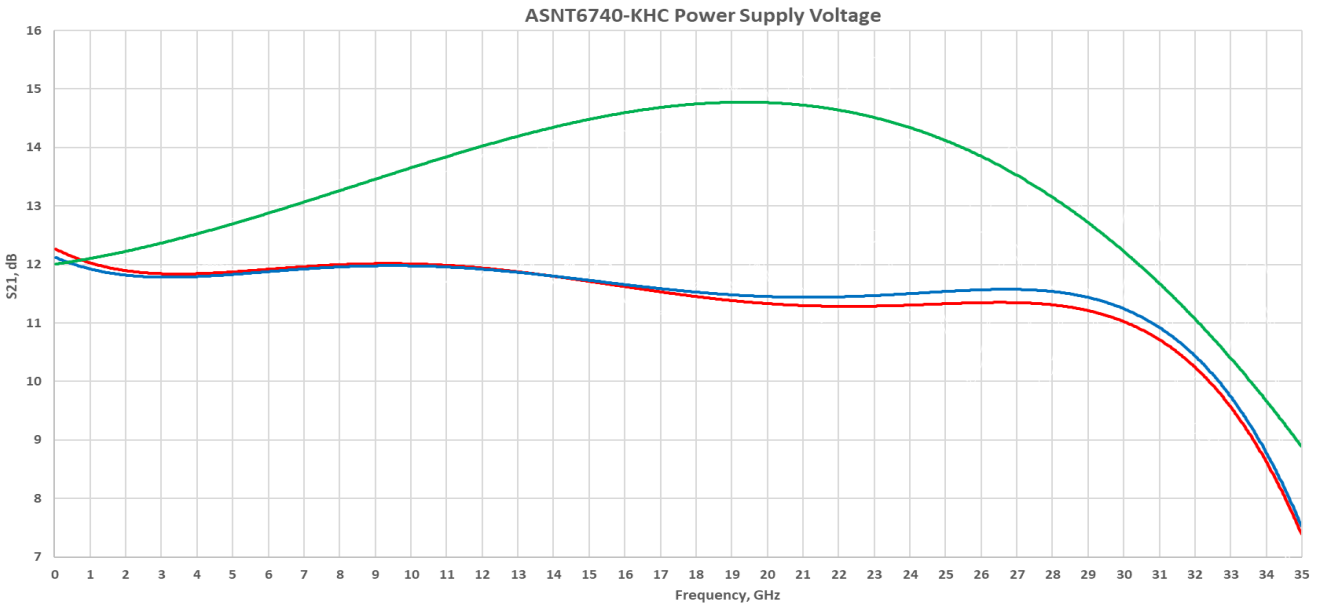

*Fig. 1. Frequency Response at Default Controls and vcc=GND with **vee=-3.6V**, **vee=-3.3V**, **vee=-3.0V***

The frequency responses at two gain/linearity digital control settings are shown in Fig. 2. All other controls are at default values.

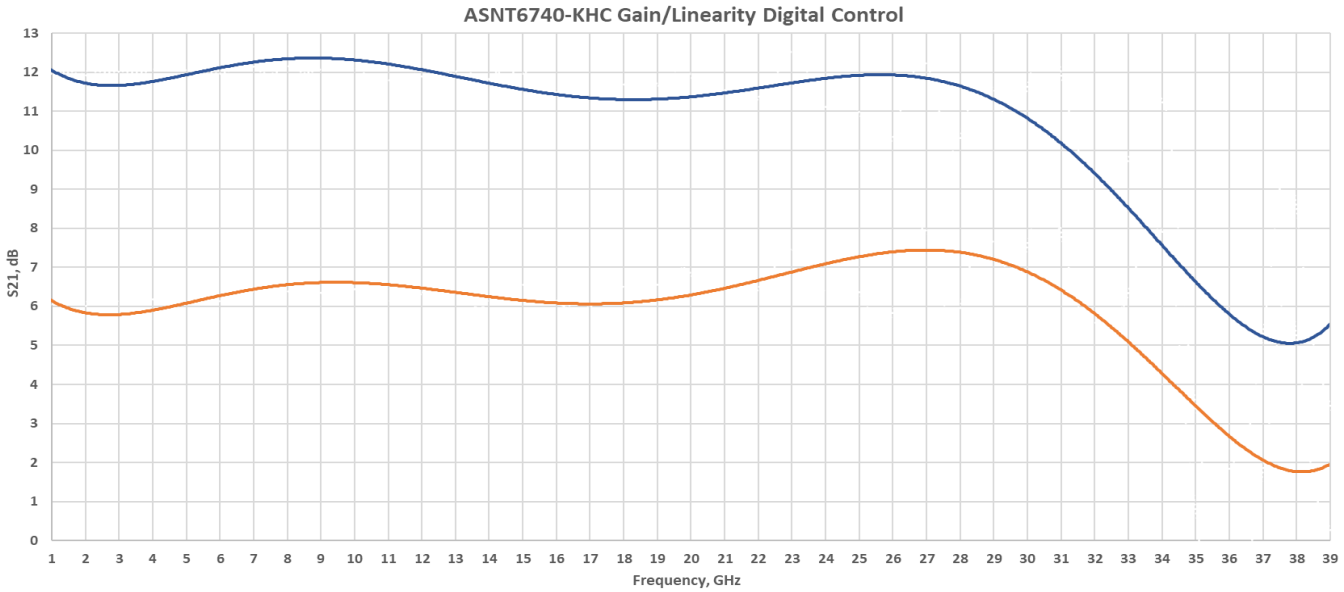

*Fig. 2. Frequency Response at **Min Gain/Max Lin** and **Max Gain/Min Lin***

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The frequency responses at various gain control settings are shown in Fig. 3. All other controls are at default values.

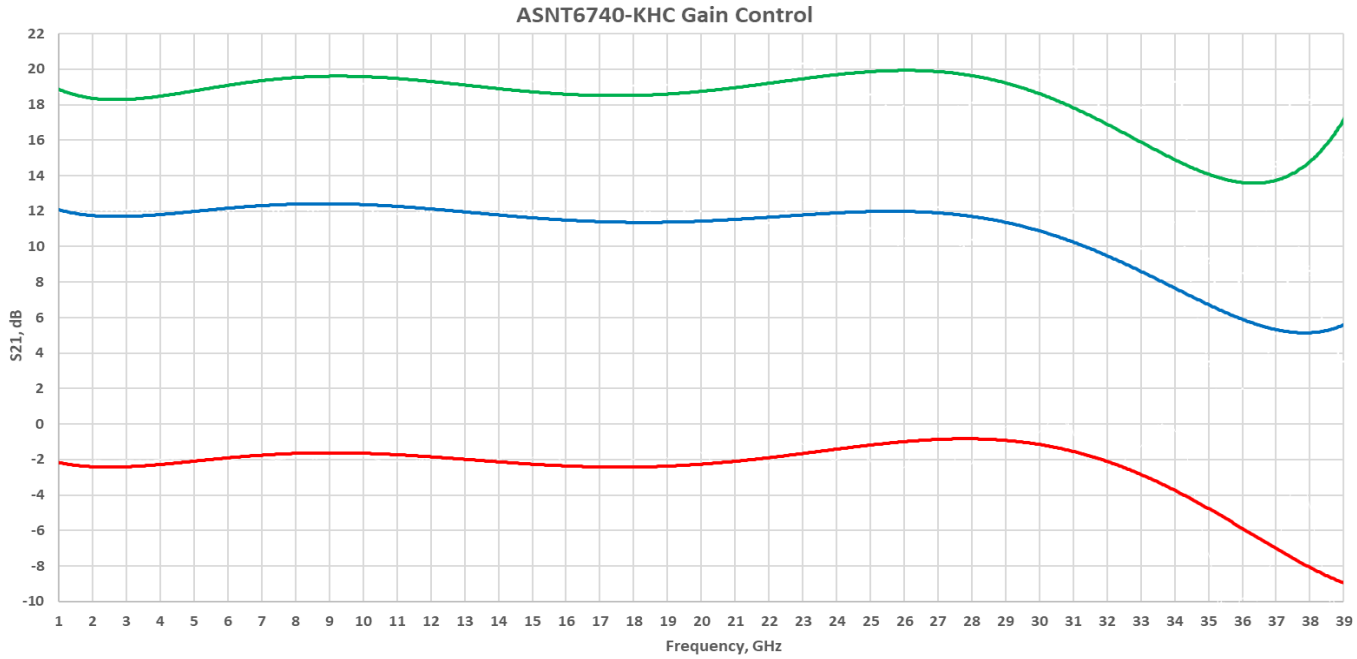

*Fig. 3. Frequency Response at **Min Gain**, **Default Gain**, and **Max Gain***

The frequency responses at different peaking controls are shown in Fig. 4. All other controls are at default values.

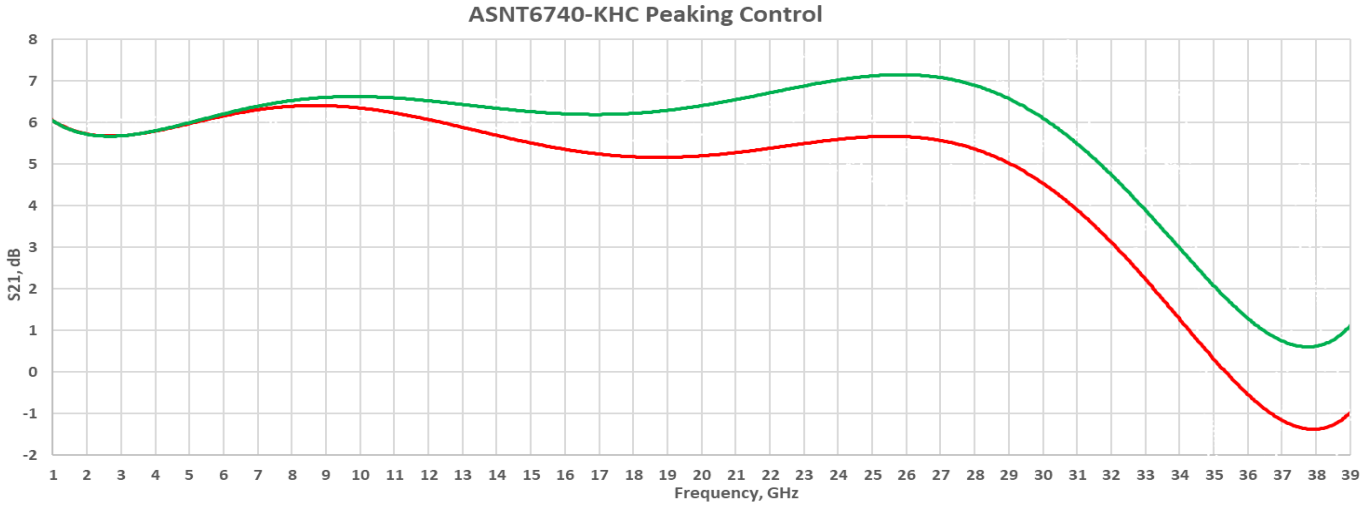

*Fig. 4. Frequency Response at **Minimum Peaking** and **Maximum Peaking***

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The frequency responses at various buffer current control settings are shown in Fig. 5. All other controls are at default values.

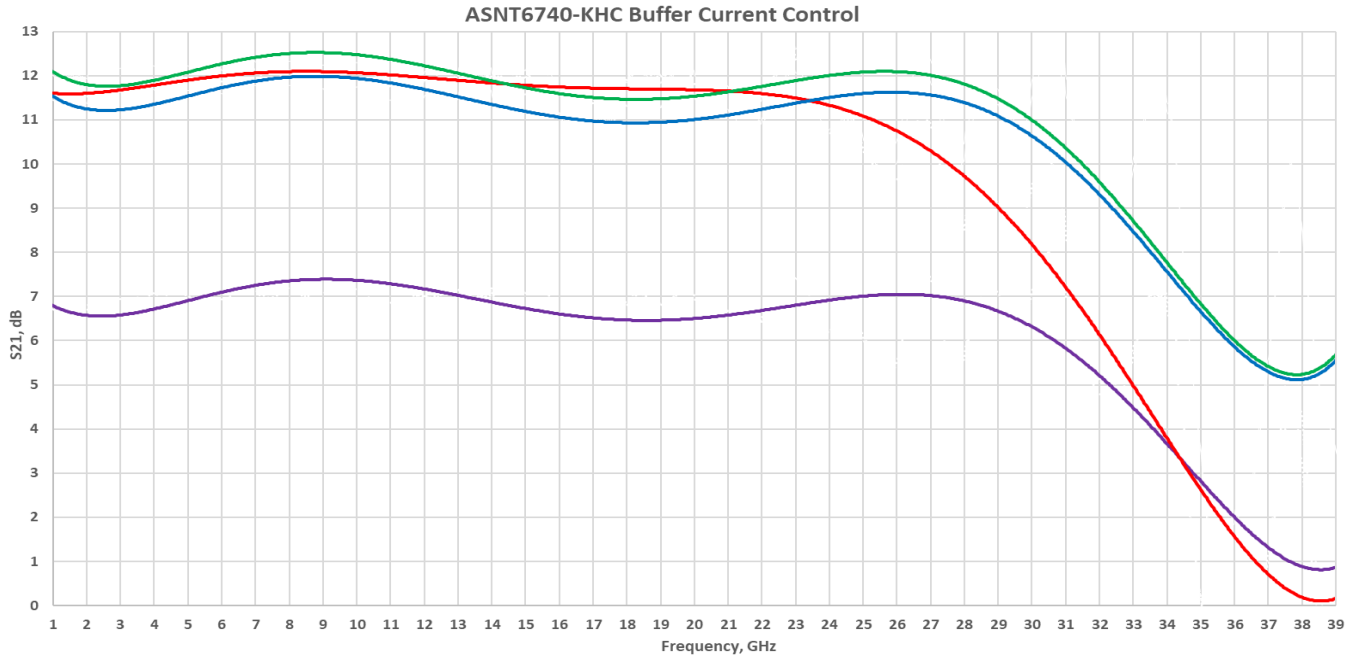

*Fig. 5. Frequency Response at **Minimal Current**, **Low Current**, **Default Current**, and **Maximum Current***

The frequency responses at various emitter follower current control settings are shown in Fig. 6. All other controls are at default values.

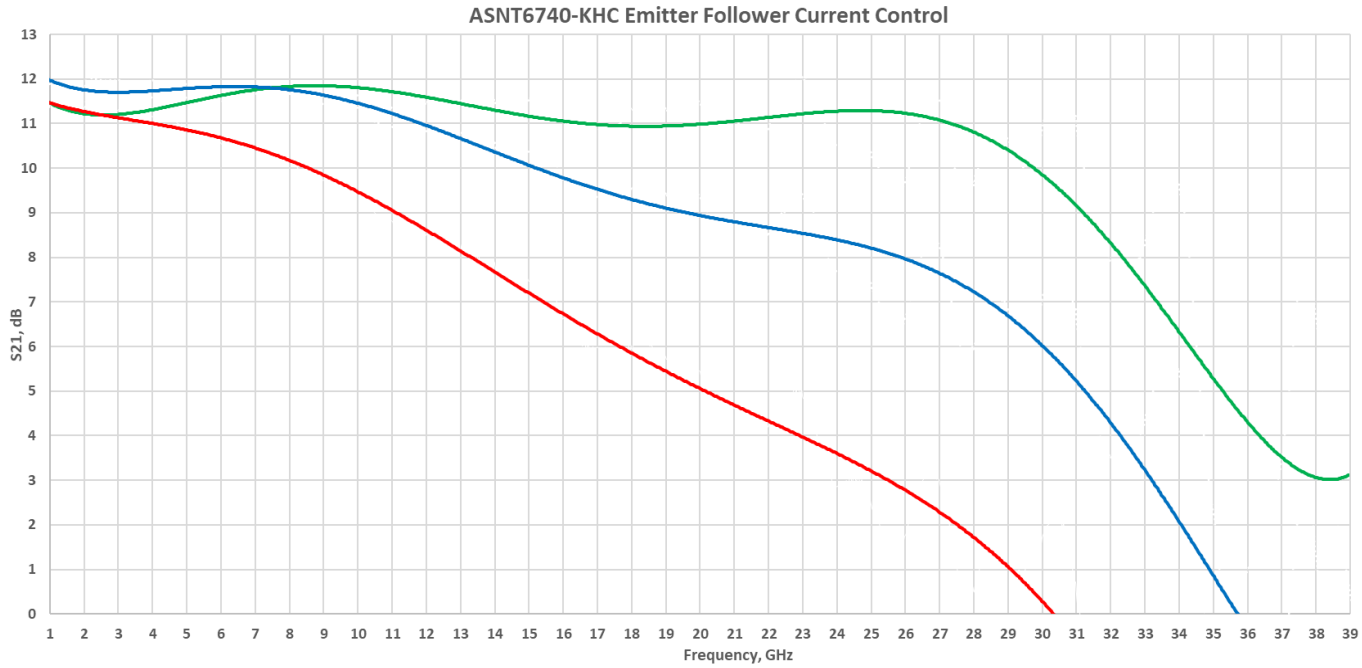

*Fig. 6. Frequency Response at **Minimum Current**, **Average Current**, and **Maximum Current***

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PAM4 SIGNAL EYE PROPAGATION EXAMPLES

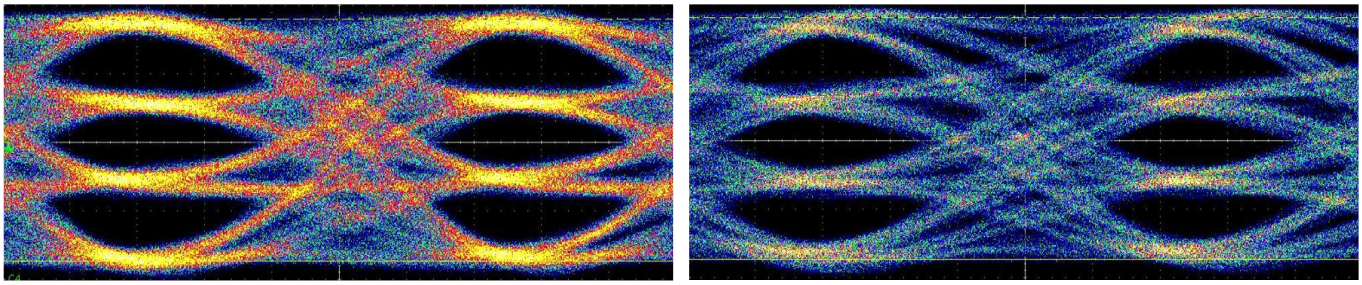

Fig. 7. PAM4 at 25.6Gbaud, Left: 100mV Diff. Pk-Pk Input, Right: 800mV Diff. Pk-Pk Output

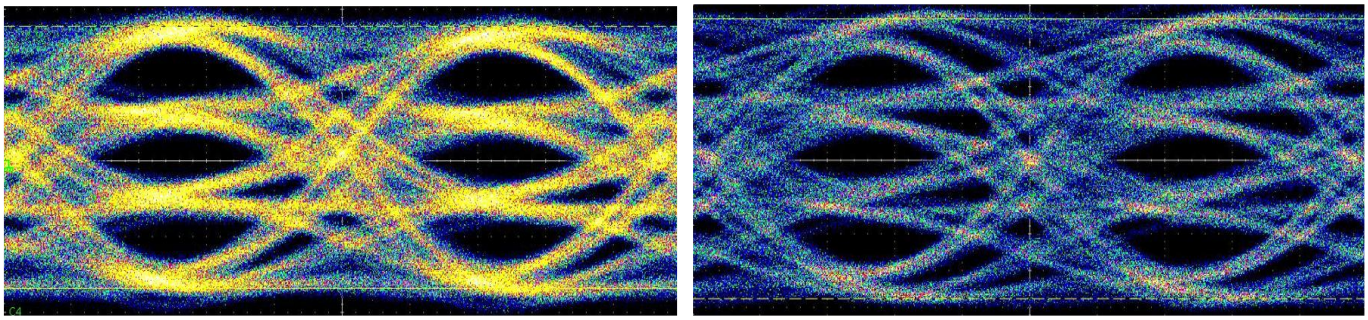

Fig. 8. PAM4 at 30Gbaud, Left: 100mV Diff. Pk-Pk Input, Right: 840mV Diff. Pk-Pk Output

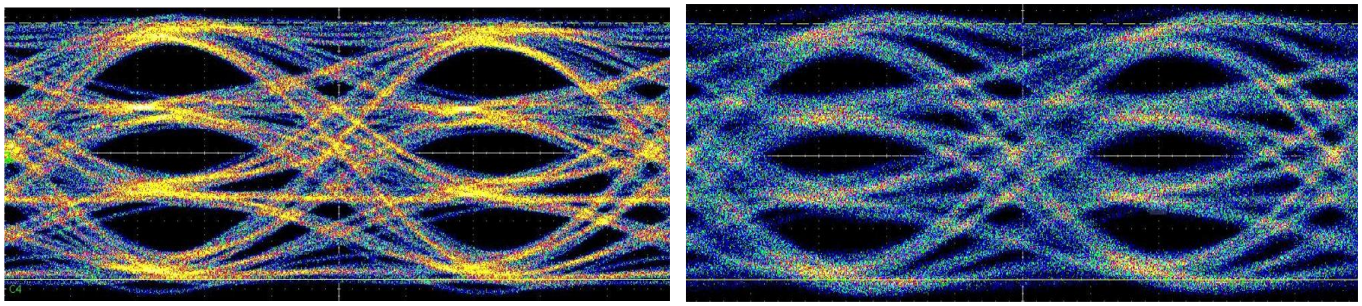

Fig. 9. PAM4 at 30Gbaud, Left: 250mV Diff. Pk-Pk Input, Right: 180mV Diff. Pk-Pk Output

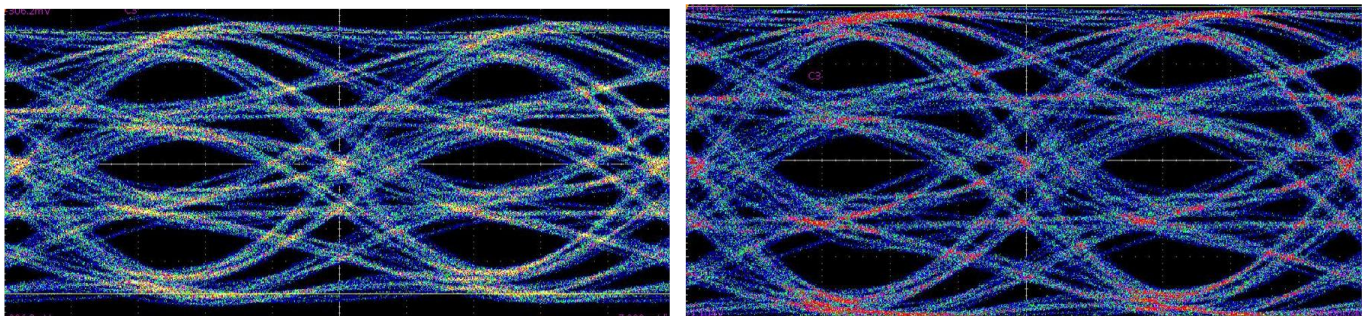

Fig. 10. PAM4 at 30Gbaud, Left: 1050mV Diff. Pk-Pk Output, Right: 1920mV Diff. Pk-Pk Output

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LINEARITY

The linearity of the ASNT6740 is detailed in Table 2. These measurements were made on single-ended outputs with recommended settings from Table 1. When the outputs are used differentially, the THD values improve.

Table 2. Linearity

Frequency, *GHz*	Input Signal Mode	Gain/Linearity Selection	Gain, dB	Output Swing, diff. pk-pk, *V*	Linearity, % THD
DC – 34	SE, Diff.	Any	13 to 19	1.0	<1
2	SE	High Gain / Low Linearity	19	1.42	2.1
	Diff.				1.8
	SE	Low Gain / High Linearity	13		1.9
	Diff.				1.8
5	SE	High Gain / Low Linearity	19		2.0
	Diff.				2.0
	SE	Low Gain / High Linearity	13		2.0
	Diff.				1.8
10	SE	High Gain / Low Linearity	19		1.2
	Diff.				1.2
	SE	Low Gain / High Linearity	13		1.3
	Diff.				1.2

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-4	*V*
Power supply current		460	*mA*
Input Voltage	vcc-1.0	vcc+0.4	*V*
RF Input Voltage Swing (SE)		1	*V*
Analog control voltages	vee	vcc	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
dp	21	CML input	Differential high-speed data inputs with internal SE 50*Ohms* termination to vcc
dn	23		
qp	11	CML output	Differential high-speed data outputs with internal SE 50*Ohms* termination to vcc. Require external SE 50*Ohms* termination to vcc
qn	9		
gncrl	3	Analog Control	Analog gain control with internal 30.5*KOhms* termination to vcc and 69.4*KOhms* termination to vee.
pkcrl	5		Analog peaking control with internal 48*KOhms* termination to vcc and 55*KOhms* termination to vee.
bufcrl	15		Analog buffer current control with internal 46*KOhms* termination to vcc and 57*KOhms* termination to vee.
efcrl	17		Analog emitter follower current control with internal 46*KOhms* termination to vcc and 57*KOhms* termination to vee.
linsel	7	CMOS	1.2V/3.3V CMOS control switch for selecting higher-gain/lower-linearity or lower-gain/higher-linearity modes. Default value: HIGH, higher-gain/lower-linearity.

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.6*V* or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.6*V*)	1, 13, 19

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.4	-3.6	-4	*V*	-12%, +6%
vcc		0.0		*V*	External ground
*I*vee	150	250	350	*mA*	At max. control range
Power consumption	510	900	1400	*mW*	At max. control range
Junction temperature	-25	50	125	*°C*	

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PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Input Analog (dp/dn)					
Bandwidth	DC		34	*GHz*	-3*dB*
Common mode voltage level		vcc		*V*	Internally generated
Input Noise Density		TBD		*nV*/sqrt*(Hz)*	
S11		TBD		*dB*	at 3*GHz*
		TBD		*dB*	at 10*GHz*
		TBD		*dB*	at 20*GHz*
		TBD		*dB*	at 25*GHz*
Output Analog (qp/qn)					
Common mode level		vcc-0.55		*V*	With external 50*Ohms* DC termination
Small signal differential gain	-8		19	*dB*	Flat up to 34*GHz*
Gain variation with optimal peaking control settings		±0.5		*dB*	Up to 34*GHz*
Total harmonic distortion		< 1	2	*%*	See Table 2
Input referred 1*dB* Compression Point		> -8		*dBm*	Single-Ended, 2*GHz* @ Maximum Gain = 19*dB*
Gain/Linearity Selection Control (linsel)					
Control value	0		1.2/3.3	*V*	0: high linearity 1.2/3.3: low linearity
Maximum Gain	13		19	*dB*	
Gain Control Signal (gncrl)					
Control range	vee+1.8		vee+3.1	*V*	at ±3.6*V* supply
Default voltage level		vee+2.5		*V*	at ±3.6*V* supply
Gain adjustment	-8 | -2		13 | 19	*dB*	at linsel = 0 | 1.2/3.3
Peak Control Signal (pkcrl)					
Control range	vee+1.2		vee+2.4	*V*	
Default voltage level		vee+1.9		*V*	at ±3.6*V* supply
Peaking adjustment	2		0	*dB*	at 28*GHz*
Current Control Signal (bufcrl)					
Control range	vee+1.5		vee+2.5	*V*	
Default voltage level		vee+2		*V*	at ±3.6*V* supply
Current adjustment	120	250	390	*mA*	
Current Control Signal (efcrl)					
Control range	vee+1.5		vee+2.5	*V*	
Default voltage level		vee+2		*V*	at ±3.6*V* supply
Current adjustment	130	265	430	*mA*	

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PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFN package shown in Fig. 11. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

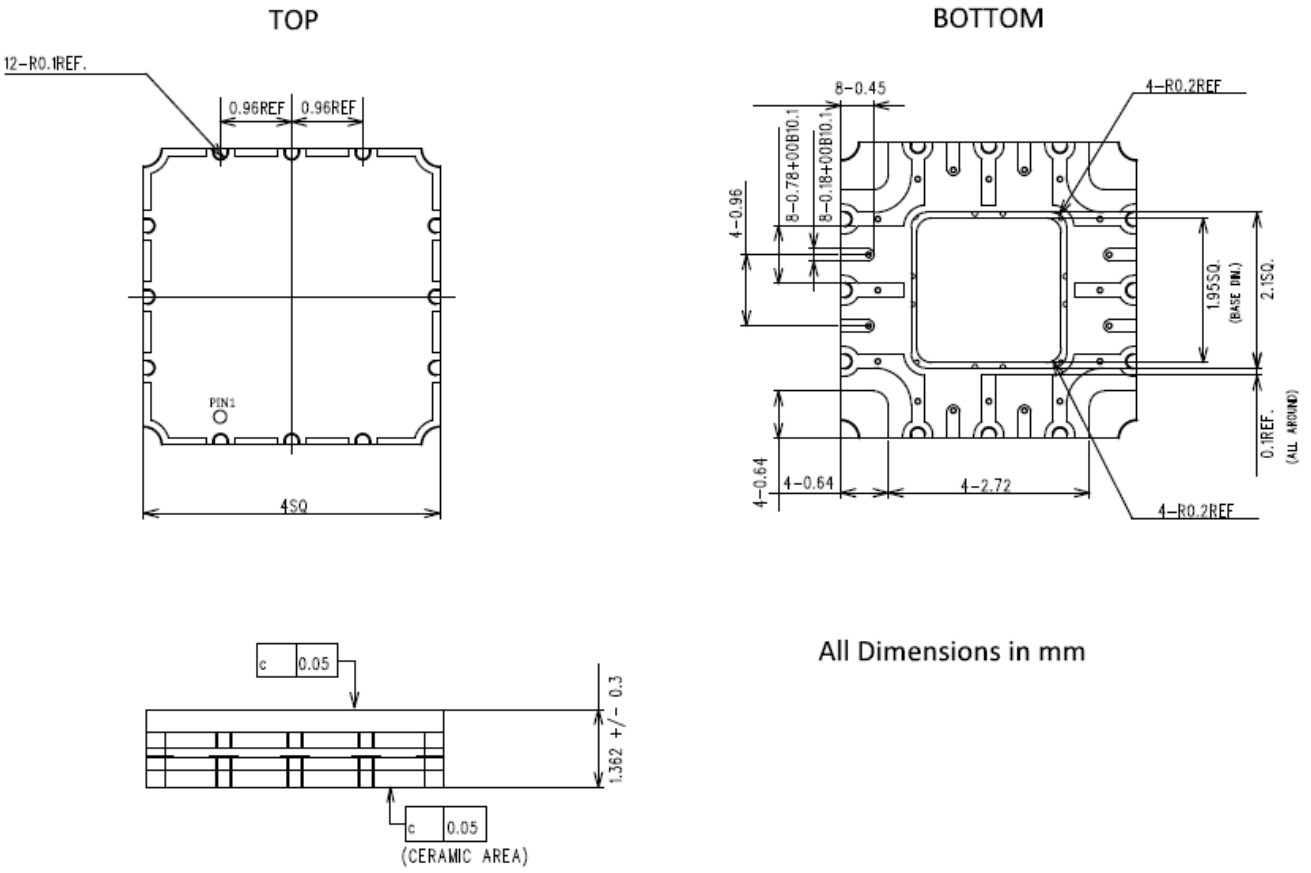

Fig. 11. CQFN 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT6740-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
1.2.2	05-2025	Corrected Pin Diagram
1.1.2	10-2024	Formatting corrections
1.0.2	10-2024	First release
0.0.2	02-2024	Preliminary release