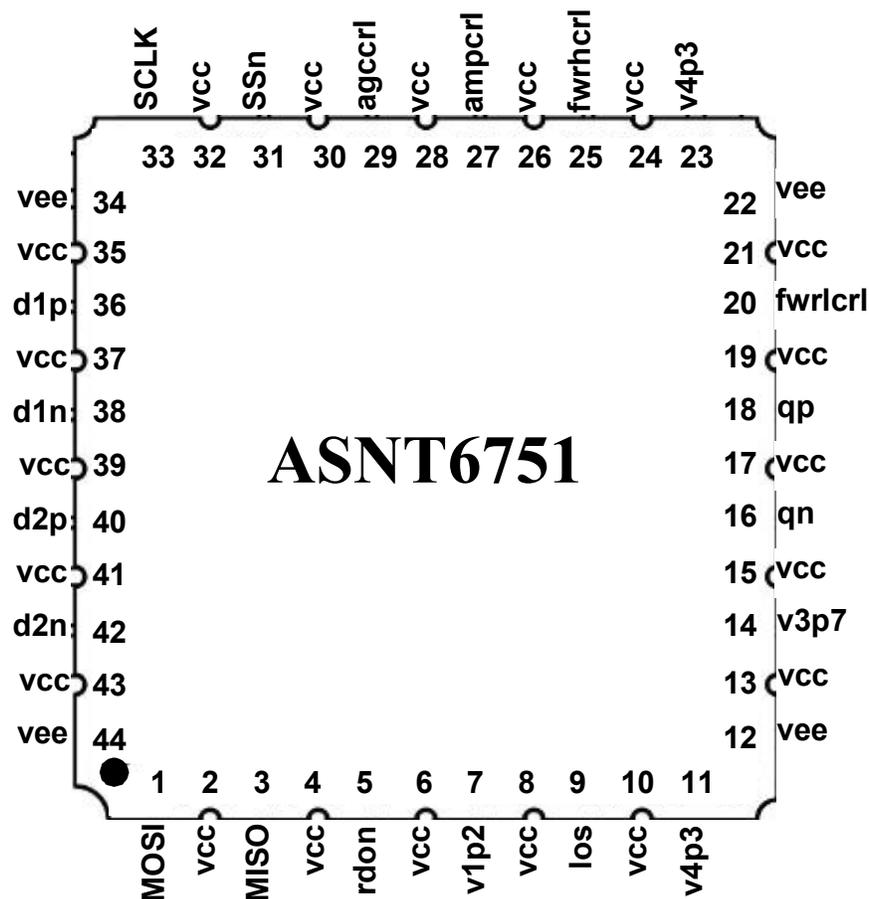


## ASNT6751-KHS

### CTLE with Selectable Automatic Adaptation or Manual Control

- High-speed adjustable linear equalizer
- Selectable automatic or manual adaptation mode
- Selectable automatic or manual AGC mode
- High-speed CMOS 3-wire interface for manual chip control
- Fully differential CML-type analog input and output interfaces
- Three power supplies for the data paths and AC control circuitry
- Average power consumption: 0.5W
- Fabricated in SiGe for high performance, yield, and reliability
- Limited temperature variation over industrial temperature range
- Die size 1.5x1.5mm<sup>2</sup>
- Custom CQFN 44-pin package



## DESCRIPTION

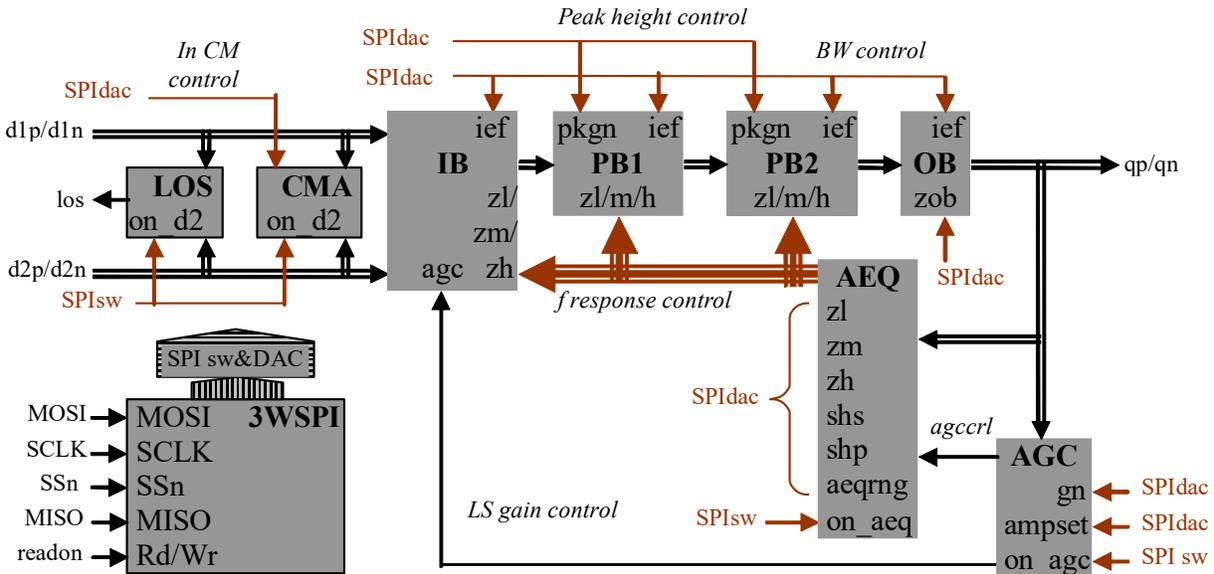


Fig. 1. Functional Block Diagram

The IC shown in Fig. 1 is an adjustable continuous-time linear equalizer (CTLE) with a possibility of manual or automatic adaptation to a user-defined frequency response. All manual adjustments are achieved through a 3-wire SPI. One of two input signal— $d1p/d1n$  or  $d2p/d2n$ —selected by the `on_d2` SPI bit, passes through an equalization data path that consists of four linear current-switching stages. The AC response of the data path can have a variable peak within a certain frequency range.

In manual mode (SPI bits `on_agc` and `on_aeq` are set to “0”), the channel’s gain can be adjusted by the SPI bytes `pkgn` (Pk in drawings below Fig. 10) and `gn` (gain in drawings below). The peak’s value, position, and shape can be adjusted by SPI bytes `zl` (LZ in drawings below), `zm` (Mz in drawings below), `zh` (Hz in drawings below), `zob` (Obz in drawings below), `pkgn` (Pk in drawings below), and `ief` (BW in drawings below).

Before activation of the automatic adaptation mode, the channel needs an initial calibration for the worst input signal conditions using manual controls `zob`, `pkgn`, and `ief`, while the SPI bits `on_agc` and `on_aeq` are set to “0”. The controls `zl`, `zm`, and `zh` should be set to maximum codes respectively. After activation of the automatic adaptation mode (SPI bytes `on_agc` and `on_aeq` are set to “1”), the part automatically adjusts to a user-defined output amplitude set by the SPI byte `ampset` and to an optimal frequency response that corresponds to the best possible eye opening of the output signal. During adaptation, the low-frequency, medium-frequency, and high-frequency zeros are gradually activated one-by-one with a certain overlap that can be controlled by the SPI byte `aeqrng`.

The part’s I/Os support a CML-type differential interface with an on-chip  $50\Omega$  termination to `vcc`. Matching external terminations are required. Critical internal voltages can be controlled through DC test points (`agccrl`, `ampcrl`, `fwrhcrl`, `fwrlcrl`) that need capacitive decoupling to `vee` on PCBs.

All operational modes of the chip are controlled through a high-speed 3-wire serial interface (3wSPI). The SPI can operate in a normal write-read mode when its internal registers are updated with every writing cycle, or in a pure reading mode when it outputs the contents of its registers without updating them. Switching between the reading mode and the writing mode of the SPI is performed by the active-low external binary signal `rdon`. The SPI supply voltage can be controlled or adjusted through pin `v1p2`.

The part operates with a positive supply  $VCC = +3.3V$  for the main data path, and additional positive supplies  $v4p3 = +4.3V$  for the AC control circuitry and  $v3p7 = +3.7V$  for the input buffer stage. The negative supply rail `vee` should be connected to external ground.

### Input Block

The values of the control switch `on_d2` determine the state of the selector that sends one of the two differential data inputs `d1p/d1n` or `d2p/d2n` to the equalization path. Table 1 describes the functionality of the control bit `on_d2`.

Table 1. Switch `on_d2` Functionality

<code>on_d2</code>	Active Input
"0"	<code>d1p/d1n</code>
"1"	<code>d2p/d2n</code>

The control `incm` can be used to adjust the input common-mode voltage level of the active differential input. Fig. 2 presents the dependence of an AC-coupled input common-mode voltage on the code of the `vcmcrl` SPI byte. Please note that in case of DC coupling, the input common-mode voltage depends on the driver's output internal termination. For a fully terminated  $50\Omega$  interconnect, the shift range is roughly half of what is presented in Fig. 2.

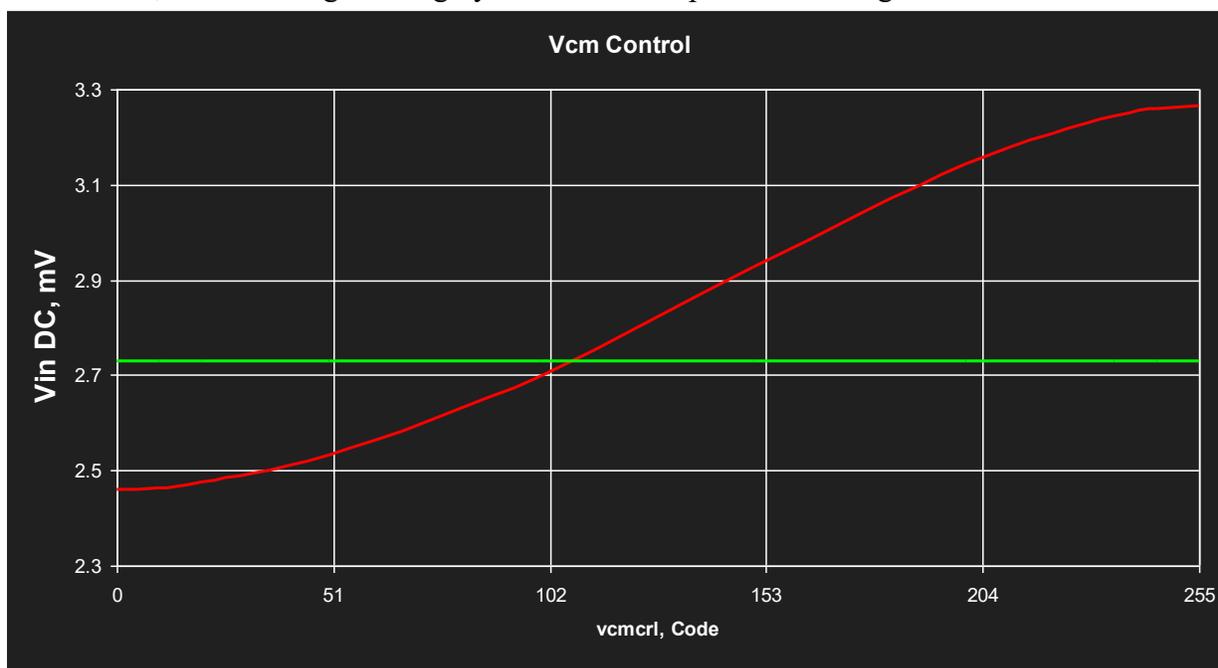


Fig. 2. Input Common-Mode Voltage Vs. `vcmcrl` Code

The loss-of-signal block (LOS) detects the d1p/d1n signal presence at the input. The detection threshold is adjustable through control loscr1 as shown in Fig. 3.

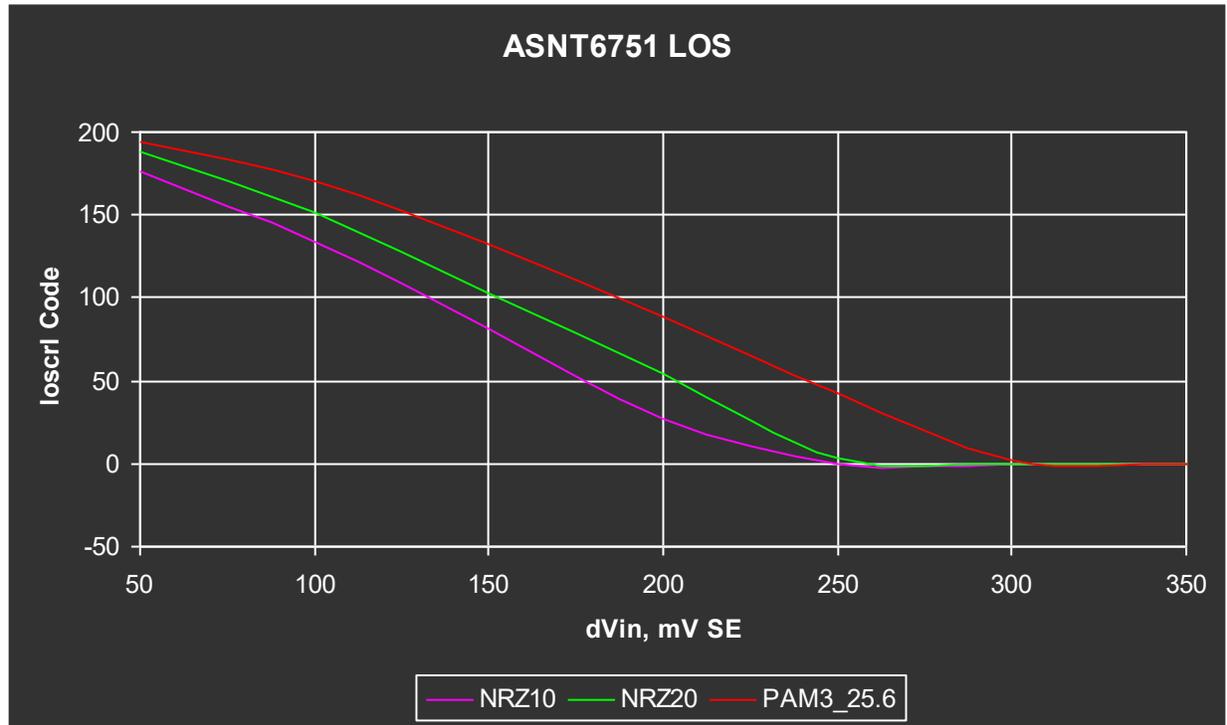


Fig. 3. LOS Threshold Control

The voltage level of the CMOS output pin los is “High” if a weak signal or no signal is present. If the input signal at d1p/d1n has an amplitude that is above the set threshold, the value of the pin los is “Low”.

### Equalization Path

The signal goes through the input selector to the equalization path. The equalization path has 4 independent adjustable Zeroes controlled by SPI signals zl, zm, zh, and zob. The corresponding controls are detailed in Table 2. Increase of any control results in an increase of the AC response gain within a certain frequency range around the specified frequency.

Table 2. Data Channel Controls

Control Function	Frequency, GHz	SPI Name
Low-frequency zero	12	zl
Mid-frequency zero	21	zm
High-frequency zero	25	zh
OB high-frequency zero	30	zob

Fig. 4 through Fig. 9 present the frequency response dependence of individual Zero control SPI bytes zl, zm, zh, or zob respectively, with all unused Zero controls in their middles of adjustment ranges (SPI code 128).

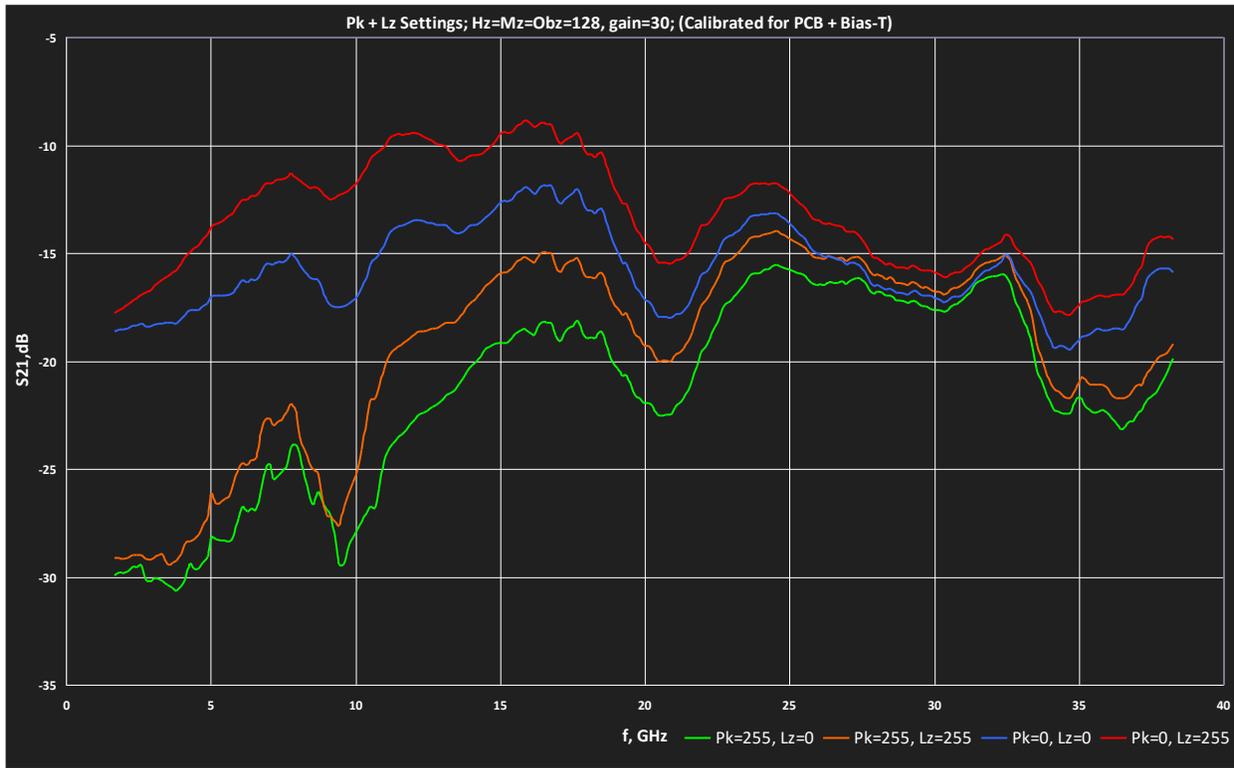


Fig. 4. CTLE Frequency Response for Various  $z1$  Values at  $gn=30$

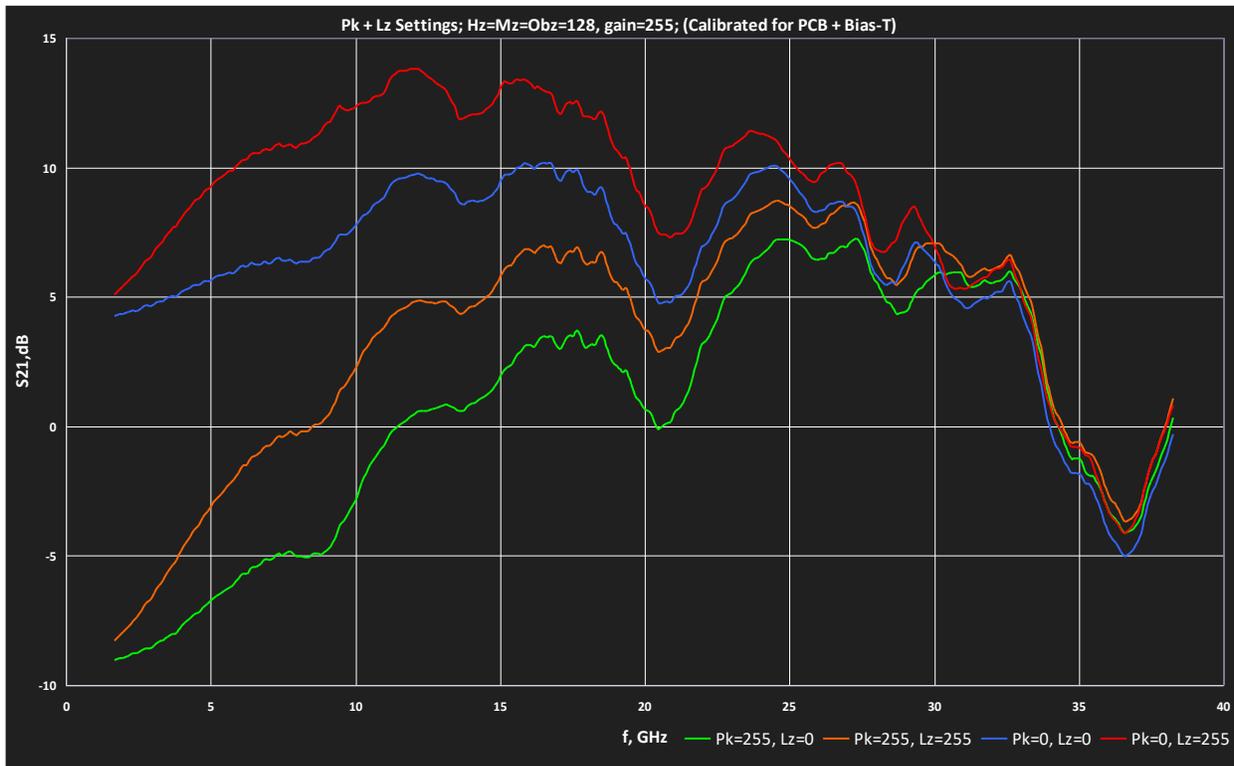


Fig. 5. CTLE Frequency Response for Various  $z1$  Values at  $gn=255$

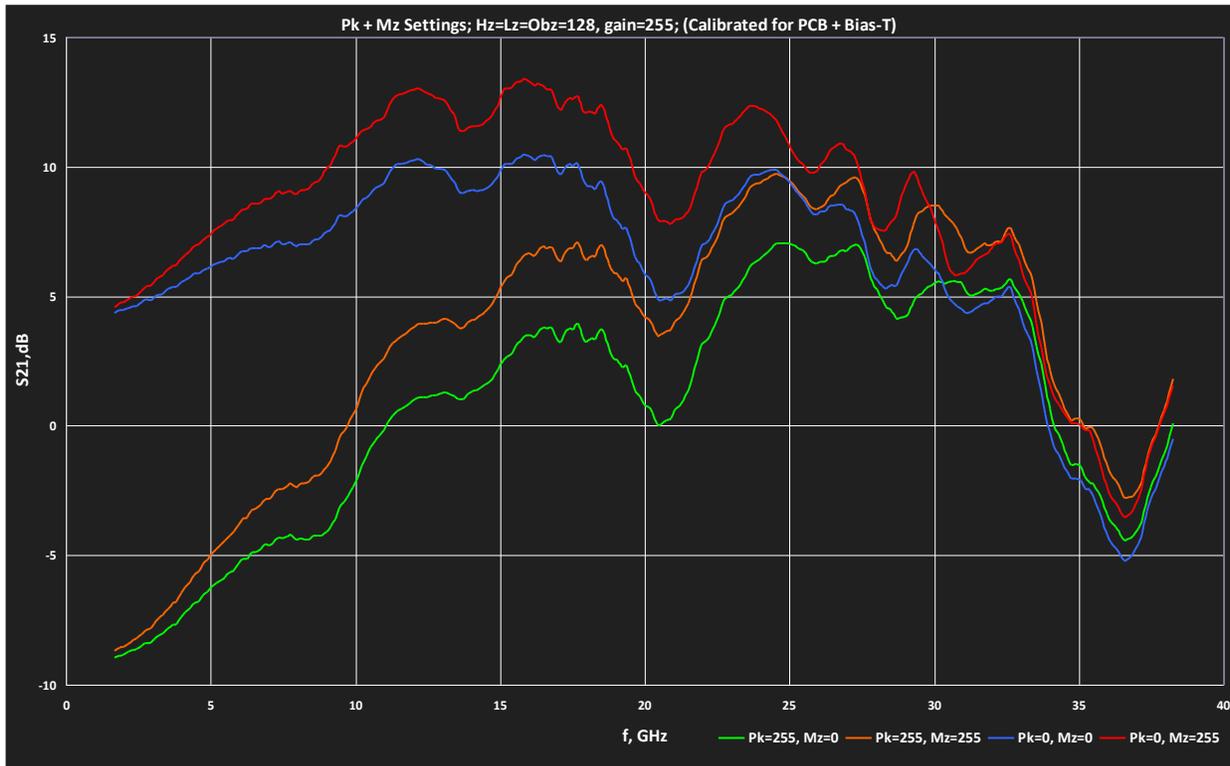


Fig. 6. CTLE Frequency Response for Various  $z_m$  Values at  $g_n=255$

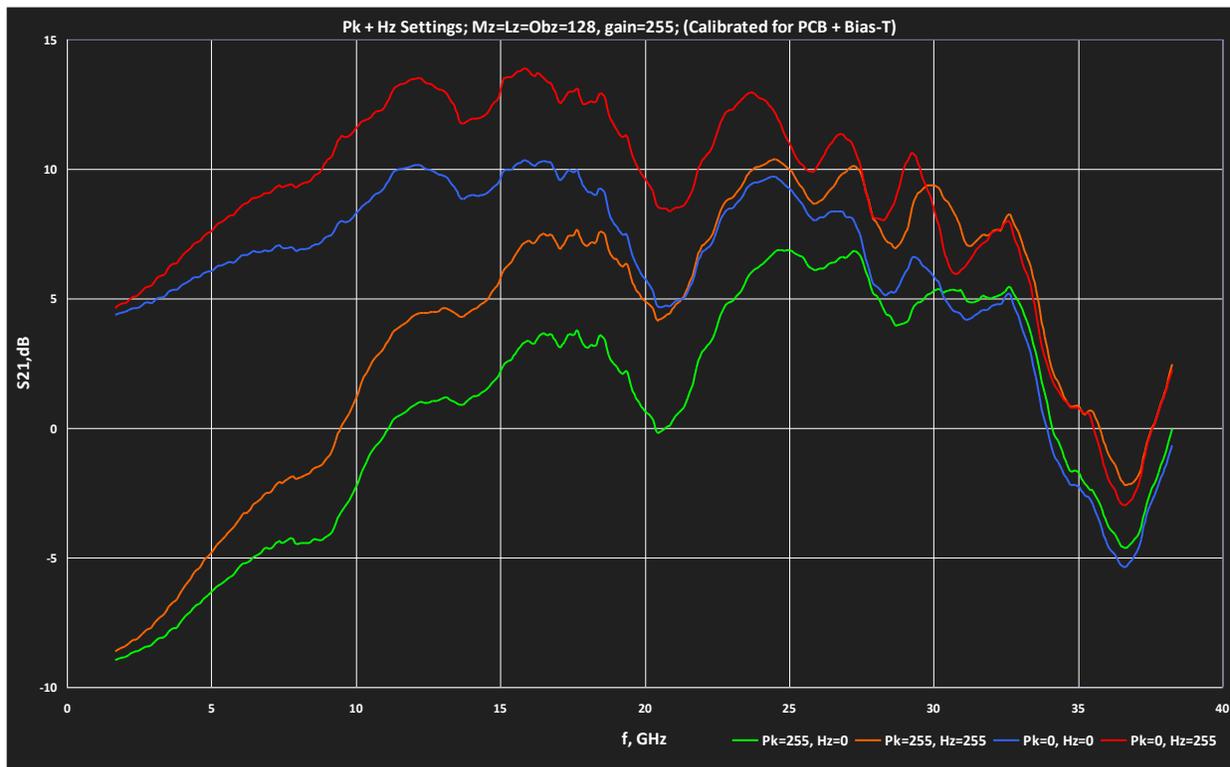


Fig. 7. CTLE Frequency Response for Various  $z_h$  Values at  $g_n=255$

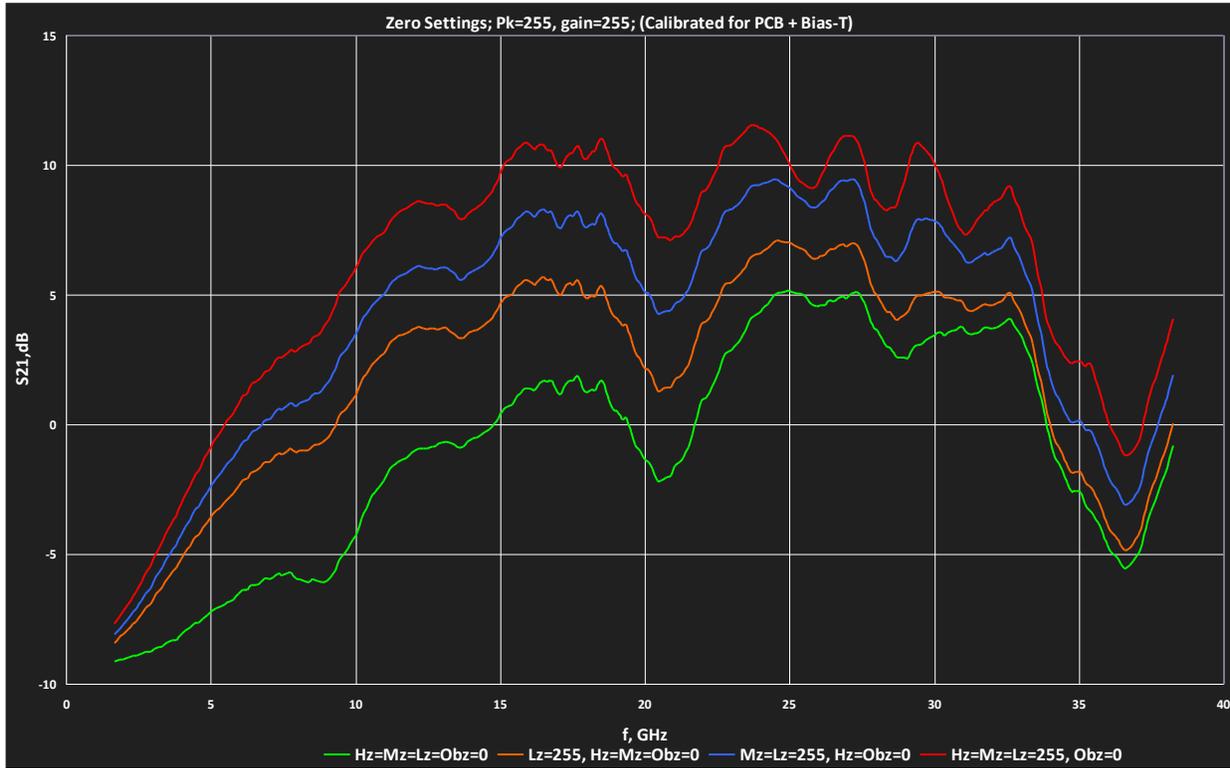


Fig. 8. CTLE Frequency Response for Various zob Values at gn=255

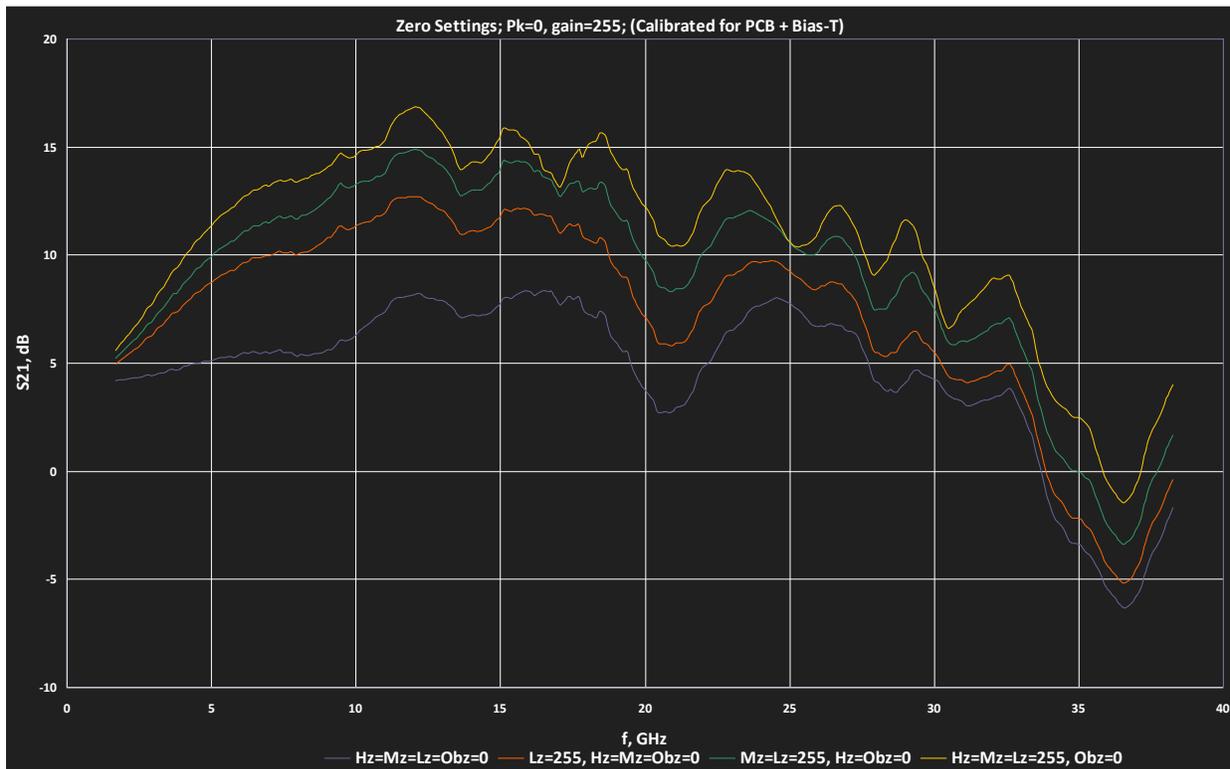


Fig. 9. CTLE Frequency Response for Various zL, zM, zH Values at zob=0, pkg=0, and gn=255

## DC Gain and Frequency Response Control

Both DC gain and frequency response of the CTLE can be adjusted either manually or automatically. The two loops are completely separate but use the same data output signal as their inputs. AGC has a lower time constant than AEQ, so it settles faster.

In manual mode (SPI bits `on_agc` and `on_aeq` are set to “0”), the channel’s gain at lower frequencies can be adjusted by the SPI byte `pkgn` as shown in Fig. 10, as well as by the SPI byte `gn` as shown in Fig. 11 through Fig. 14. It should be noted that the `pkgn` control does not affect the channels frequency response at higher frequencies as described below.

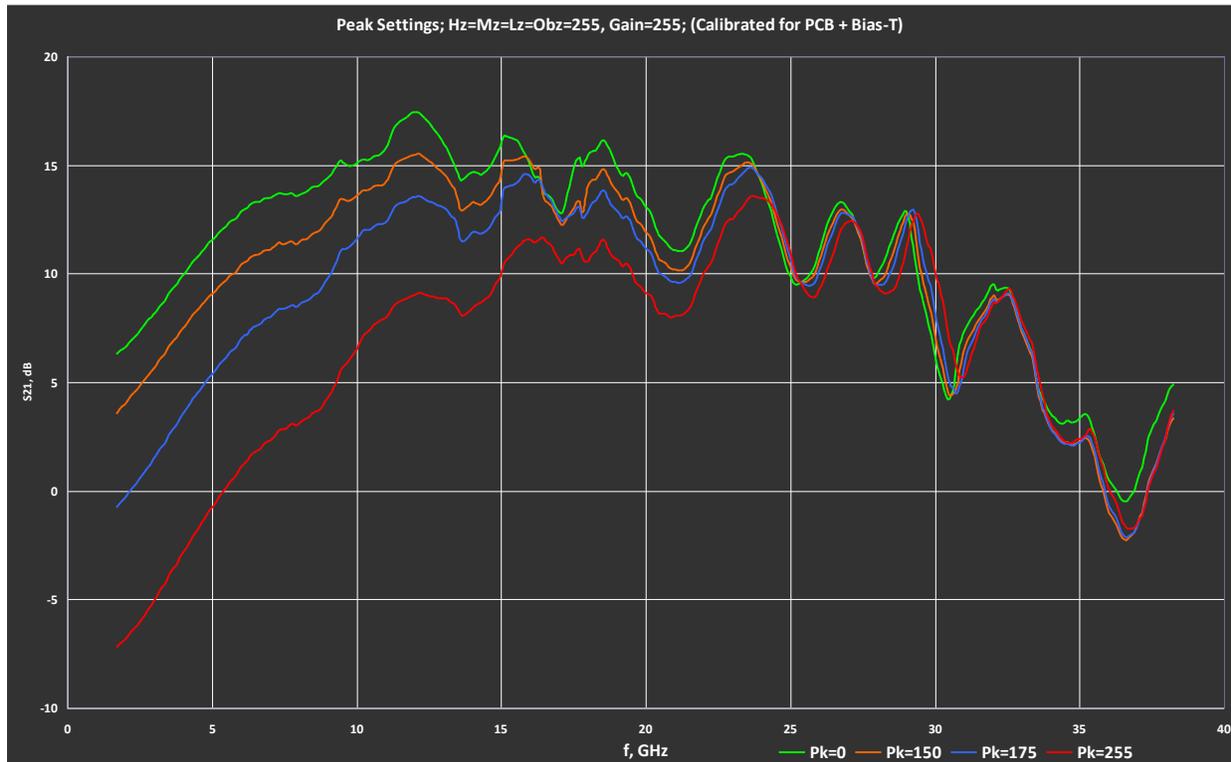


Fig. 10. CTLE Frequency Response for Various `pkgn` Values at `gn=255` and all Zeros=255

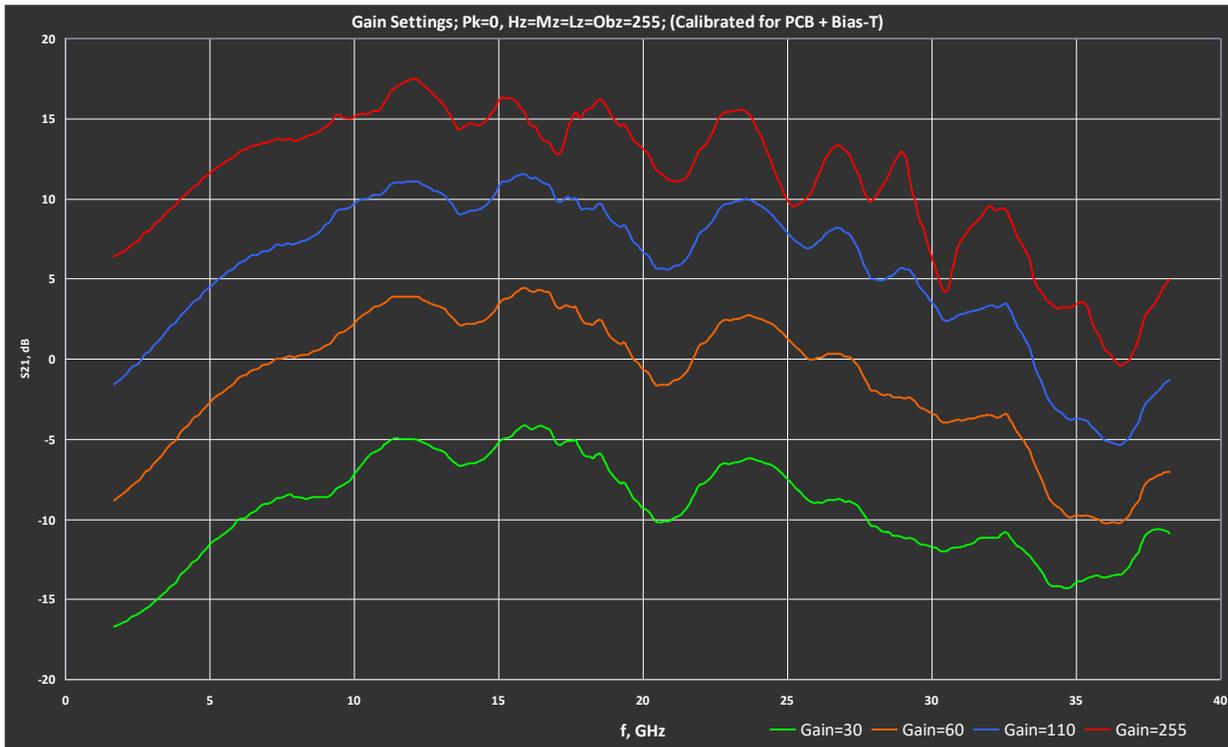


Fig. 11. CTLE Frequency Response for Various  $gn$  Values at  $pkgn=0$  and all Zeros=255

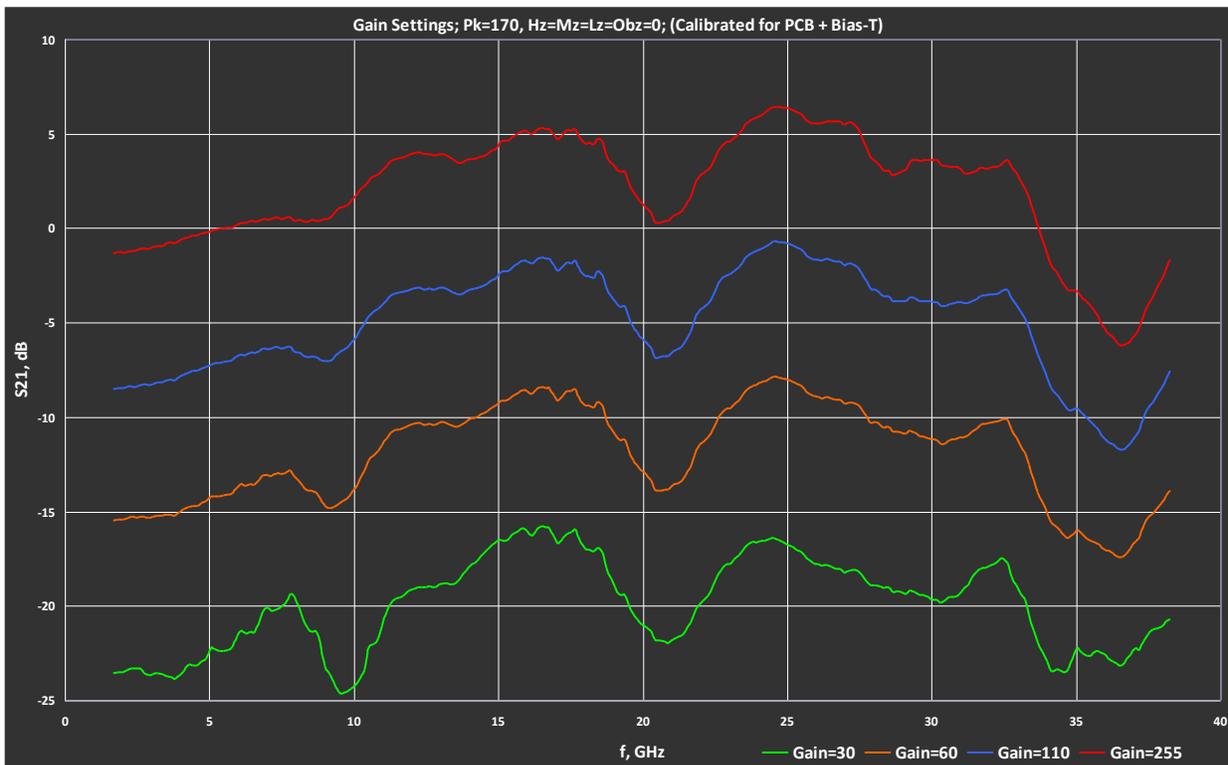


Fig. 12. CTLE Frequency Response for Various  $gn$  Values at  $pkgn=170$  and all Zeros=0

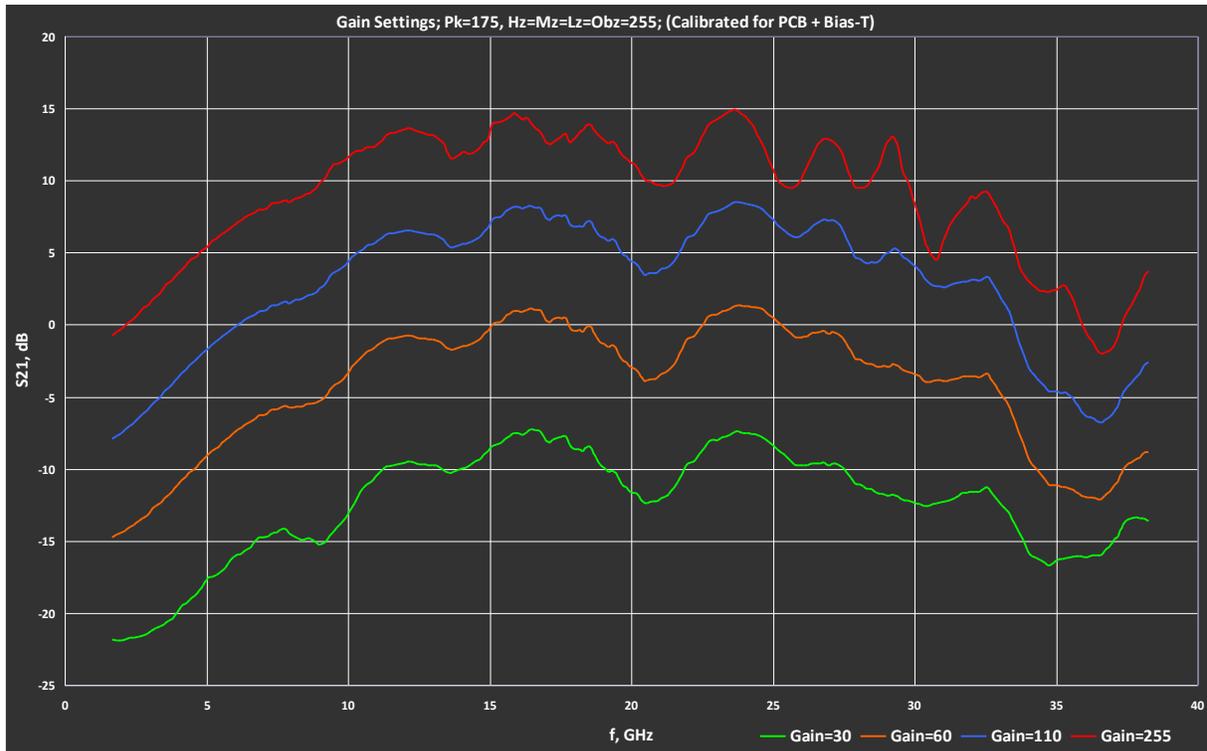


Fig. 13. CTLE Frequency Response for Various  $gn$  Values at  $pkgn=170$  and all Zeros=255



Fig. 14. CTLE Frequency Response for Various  $gn$  Values at  $pkgn=255$  and all Zeros=255

The channel's frequency response including peak's value and position can be additionally adjusted by the SPI byte *ief* as illustrated by Fig. 15.

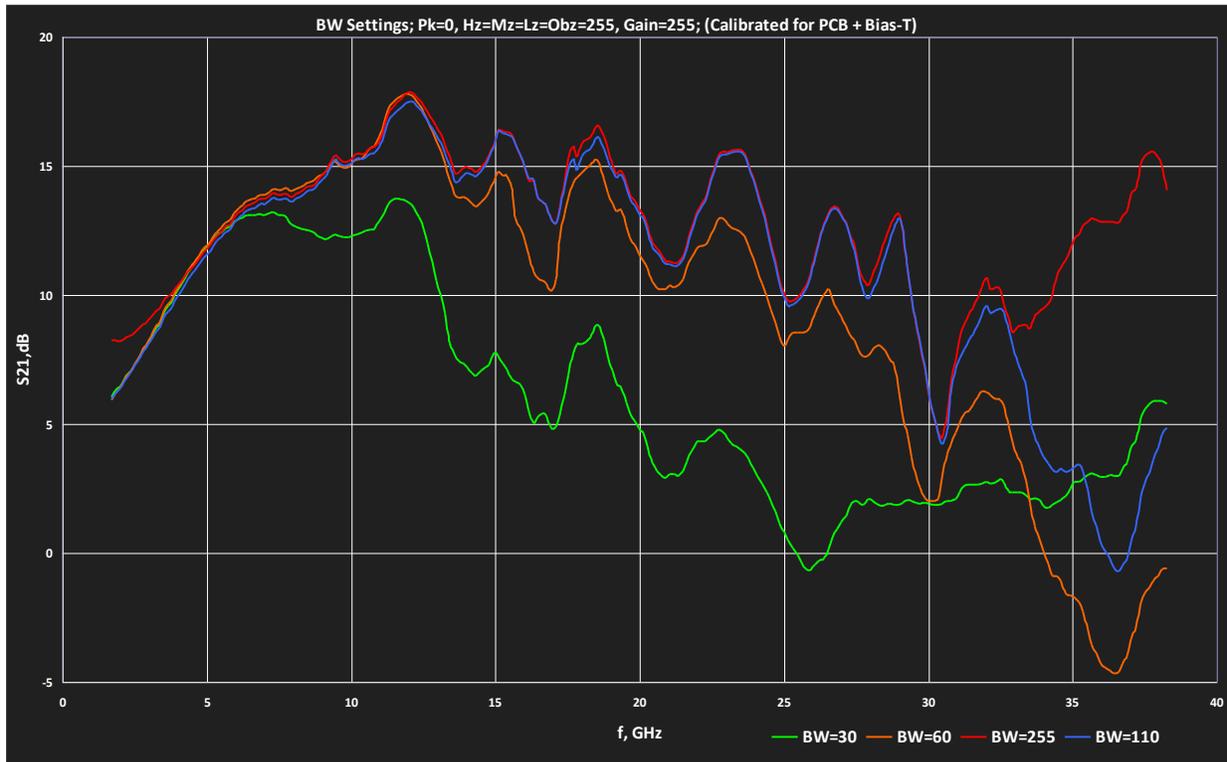


Fig. 15. CTLE Frequency Response for Various *BW (ief)* Values at *gn=255*, *pkgn=0*, and all Zeros=255

### **DC Gain Automatic Tuning**

In the automatic mode (SPI bit *on\_agc* is set to “1”) the AGC loop adjusts the DC gain of the CTLE in order to keep the low-frequency output amplitude at the user-defined level which is set by the SPI byte *ampset*. This control operates in the same way as the manual control *gn*, as shown in Fig. 11 through Fig. 14 above. Since the output control voltage of AGC affects all frequencies the same way, the entire frequency response curve is shifted up or down within the range and the shape of the frequency response curve does not change.

### **Frequency Response Automatic Adaptation**

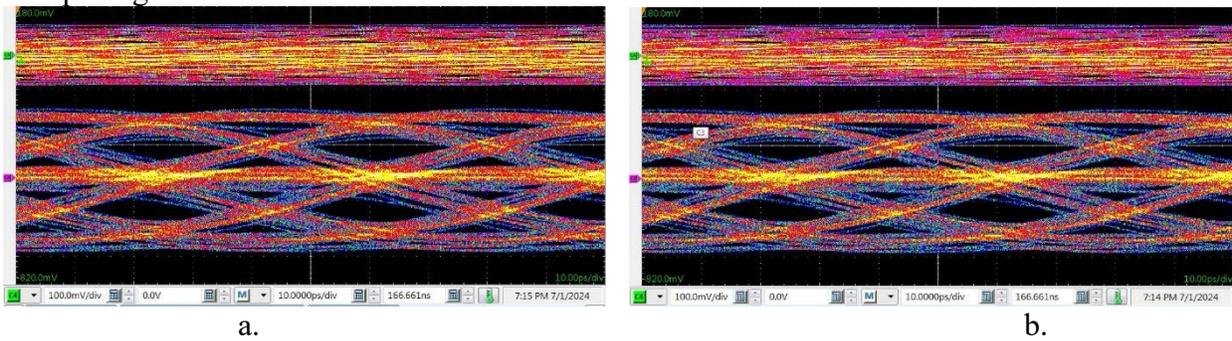
Prior to AEQ activation, manual tuning of the *zl*, *zm*, *zh*, *zob*, *pkgn*, and *ief* controls is required for the worst input signal conditions. During this tuning the SPI bit *on\_aeq* should be set to “0”.

After switching to automatic mode (SPI bit *on\_aeq* is set to “1”), the AEQ loop gradually activates the three zeros *zl*, *zm*, and *zh* one-by-one with a certain overlap that can be controlled by the SPI byte *aeqrng*. When a higher/lower peaking is required, the influence of the zeros is increased/decreased starting from *zh*. The overlap of control ranges of different zeros can be adjusted using the *aeqrng* SPI byte, where higher codes correspond to less overlap of the ranges.

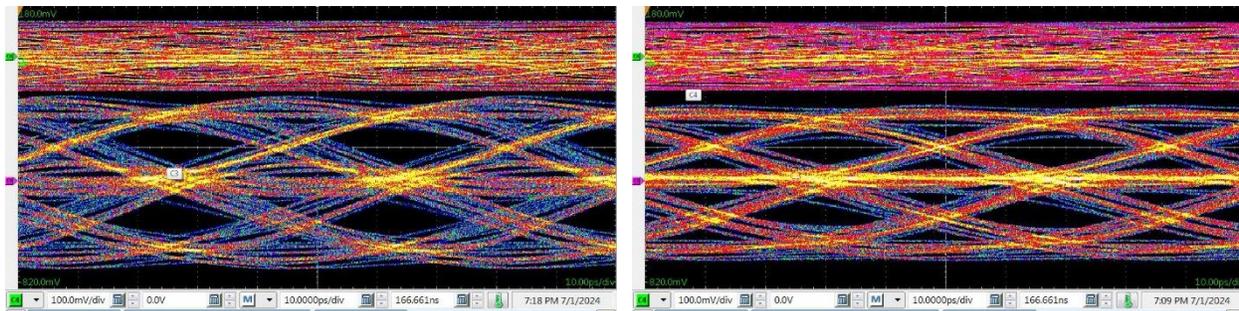
To ensure efficient automatic equalization, the SPI byte *sfshs* should be initially set to 255 and then lowered down until the desired output eye quality is achieved. This SPI byte adjusts the target peaking of the channel’s frequency response. One more SPI byte *sfshp* can be used to tune the temperature dependence of the equalization feed-back balance. It should be kept at the default value for normal operation.

For more details on the automatic adaptation mode activation refer to the TP\_ASNT6751-KHSONASNT22\_1\_2 document.

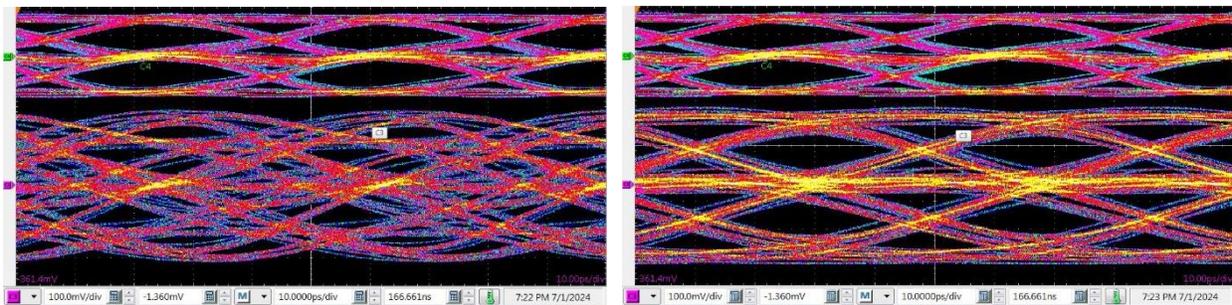
Fig. 16 through Fig. 18 demonstrate the part's handling of different PAM3 inputs signals in case of manual tuning to the worst-case conditions and in case of automatic adaptation with initial tuning to the same conditions. It should be noted that the manual tuning was kept unchanged for all input signal conditions.



*Fig. 16, Worst-Case Input (Top) and Output (Bottom) Eyes at Manual (a) and Automatic (b) Adaptation*



*Fig. 17, Medium-Case Input (Top) and Output (Bottom) Eyes at Manual (a) and Automatic (b) Adaptation*



*Fig. 18, Best-Case Input (Top) and Output (Bottom) Eyes at Manual (a) and Automatic (b) Adaptation*

It can be seen that the AEQ feedback keeps the output eyes open for all conditions, while the output eyes get closed for the medium-case and best-case input signals with unchanged manual tuning due to excessive peaking.

### 3-Wire Interface

All functions of the chip are controlled through the 3-wire SPI. The interface includes a 14-byte internal register and operates with CMOS signals from 1.2V to 3.3V. The SPI operates in Mode 0: data changes at falling edges of SCLK and is sampled at its rising edges.

In the write operational mode, the read enable signal RdOn must be set to logic “0” before SSn becomes active and must stay unchanged until SSn release. The internal data is updated at a rising edge of SSn. In the read operational mode, the read enable signal RdOn must be set to logic “1” before SSn becomes active and must stay unchanged until SSn release. The output data transmission starts at a rising edge of SSn. The SPI timing diagram is shown in Fig. 19 and its bit map is detailed in Table 3.

Table 3. 3-Wire Interface Bit Map

Byte #	Bit #	Bit order	Signal name	Signal function	Default State <sup>1)</sup>
1	From 7	MSB	zl	Manual control of the low-frequency zero	“1111111”
	to 0	LSB			
2	From 7	MSB	zm	Manual control of the medium-frequency zero	“1111111”
	to 0	LSB			
3	From 7	MSB	zh	Manual control of the high-frequency zero	“1000000”
	to 0	LSB			
4	From 7	MSB	zob	Manual control of the output buffer zero	“0000000”
	to 0	LSB			
5	From 7	MSB	pkgn	Manual control of the pkgn signal (FB off)	“1000000”
	to 0	LSB			
6	From 7	MSB	ief	Bandwidth manual adjustment (FB off)	“1000000”
	to 0	LSB			
7	From 7	MSB	gn	Manual gain control (FB off)	“1111111”
	to 0	LSB			
8	From 7	MSB	ampset	Output amplitude setting (AGC FB on)	“1000000”
	to 0	LSB			
9	From 7	MSB	incm	Input 1 DC common mode voltage adjustment	“01011010”
	to 0	LSB			
10	From 7	MSB	sfshs	Initial adaptive FB balance at nominal temperature	“1000000”
	to 0	LSB			
11	From 7	MSB	sfshp	Temperature variation control of adaptive FB balance	“1000000”
	to 0	LSB			
12	From 7	MSB	aeqrng	Overlap of zeros control Ranges adjustment	“1000000”
	to 0	LSB			
13	From 7	MSB	loscrl	Loss of signal detection threshold control	“1000000”
	to 0	LSB			
14	7		on_d2	Input 2 activation	“0”
	6		-	Not Used	“0”
	5		on_agc	AGC FB activation	“0”
	4		on_aeq1	zl adaptation activation	“0”
	3		on_aeq2	zm adaptation activation	“0”
	2		on_aeq3	zh adaptation activation	“0”
	1		-	Not Used	“0”
	0		-	Constant “0”	“0”

1).The SPI internal registers are preset to the default states at the power supply activation time.

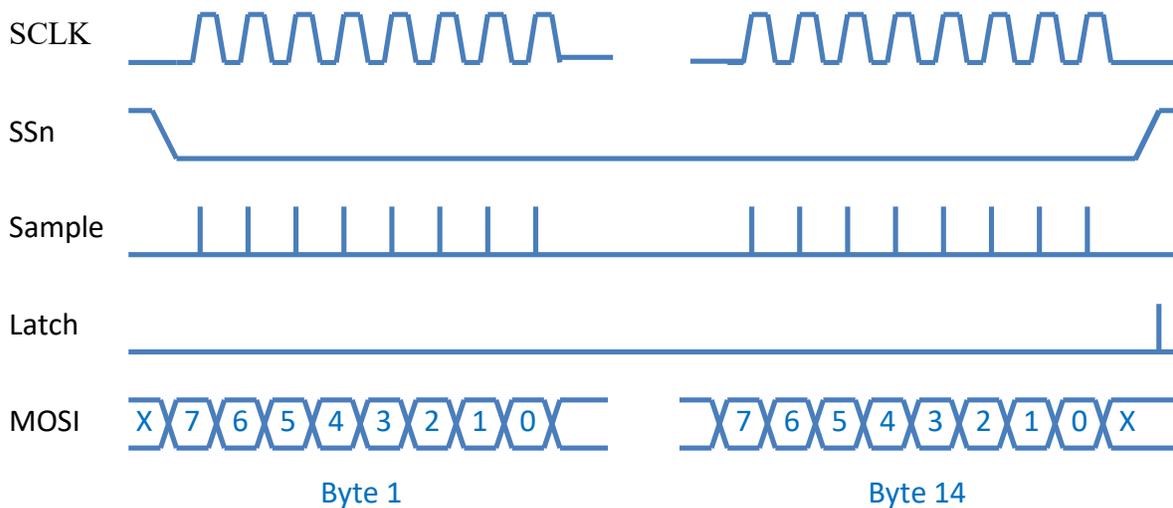


Fig. 19. SPI Timing Diagram

## TERMINAL FUNCTIONS

TERMINAL			Description
Name	No.	Type	
<b>High-Speed I/Os</b>			
d1p	36	CML-type	Differential high-speed channel 1 data inputs with internal SE 50 $\Omega$ termination to VCC
d1n	38		
d2p	40	Analog Inputs	Differential high-speed channel 2 data inputs with internal SE 50 $\Omega$ termination to VCC
d2n	42		
qp	18	CML-type	Differential high-speed data outputs with internal SE 50 $\Omega$ termination to VCC
qn	16		
<b>Low-Speed I/Os</b>			
SSn	31	1.2V to 3.3V	3-wire interface enable input with internal 536K $\Omega$ pull-up to VCC
SCLK	33		3-wire interface clock input with internal 536K $\Omega$ pull-down to VEE
MOSI	1	CMOS I/Os	3-wire interface data input with internal 536K $\Omega$ pull-down to VEE
MISO	3		3-wire interface data output
rdon	5		3-wire read/write enable input with internal 536K $\Omega$ pull-down to VEE
los	9		Loss of signal indicator output
<b>Tuning Ports and Control Points</b>			
fwrlcr1	20	Analog ports	AEQ FB low-speed error signal control
fwrhcr1	25		AEQ FB high-speed error signal control
ampcr1	27		AGC amplitude setting control
agccr1	29		AGC FB error signal control



Supply And Termination Voltages		
Name	Description	Pin Number
vee	Ground	12, 22, 34, 44
v4p3	+4.3V positive power supply Negative pin to vee	11, 23
v3p7	+3.7V positive power supply Negative pin to vee	14
v1p2	+1.2V positive supply / control point Negative pin to vee	7
vcc	+3.3V positive power supply Negative pin to vee	2, 4, 6, 8, 10, 13, 15, 17, 19, 21, 24, 26, 28, 30, 32, 35, 37, 39, 41, 43

## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee		0.0		V	External ground
vcc		3.3		V	vcc in relation to vee
v3p7		3.7		V	v3p7 in relation to vee
v4p3		4.3		V	v4p3 in relation to vee
I <sub>vcc</sub>	95		230	mA	Depending on the state of SPI control bytes
I <sub>v3p7</sub>		4		mA	
I <sub>v4p3</sub>	2		20	mA	
Power Consumption		600		mW	
Junction temperature	0	50	125	°C	
<b>Data input (d1p/d1n, d2p/d2n)</b>					
Data Rate	DC		26	Gb/s	
SE Swing		270	600	mV	For MAX output swing
DC CM voltage		vcc-0.6			Adjustable through SPI
Input termination		35	50	Ohms	
<b>Data output (qp/qn)</b>					
Max peaking frequency		28		GHz	
DC gain from Input	-28		+6	dB	Depending on SPI settings
Max voltage swing		600		mV	SE pk-pk
CM Level		vcc-0.44		V	for DC output termination
<b>Linearity (Flat Frequency Response)</b>					
THD		1.5		%	Input 400mV p-p@1GHz
THD		3.0		%	Input 600mV p-p@1GHz
THD		2.4		%	Input 400mV p-p@10GHz
THD		4.9		%	Input 600mV p-p@10GHz
<b>3-Wire Interface</b>					
Clock frequency		0.1	50	MHz	
In/out low logic levels	vee	vee+0.1		V	
In/out high logic levels	vee+1.1	vee+1.3		V	
Input current			9	uA	For each input

## PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFN package shown in Fig. 20. The package provides a center heat slug located on the back side of the package to be used for heat dissipation. ADSANTEC recommends using extreme caution when soldering this section to the board to avoid overheating. It should be connected to the VCC plain that is ground for the negative supply, or power for the positive supply.

The part's identification label is ASNT6751-KHS. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

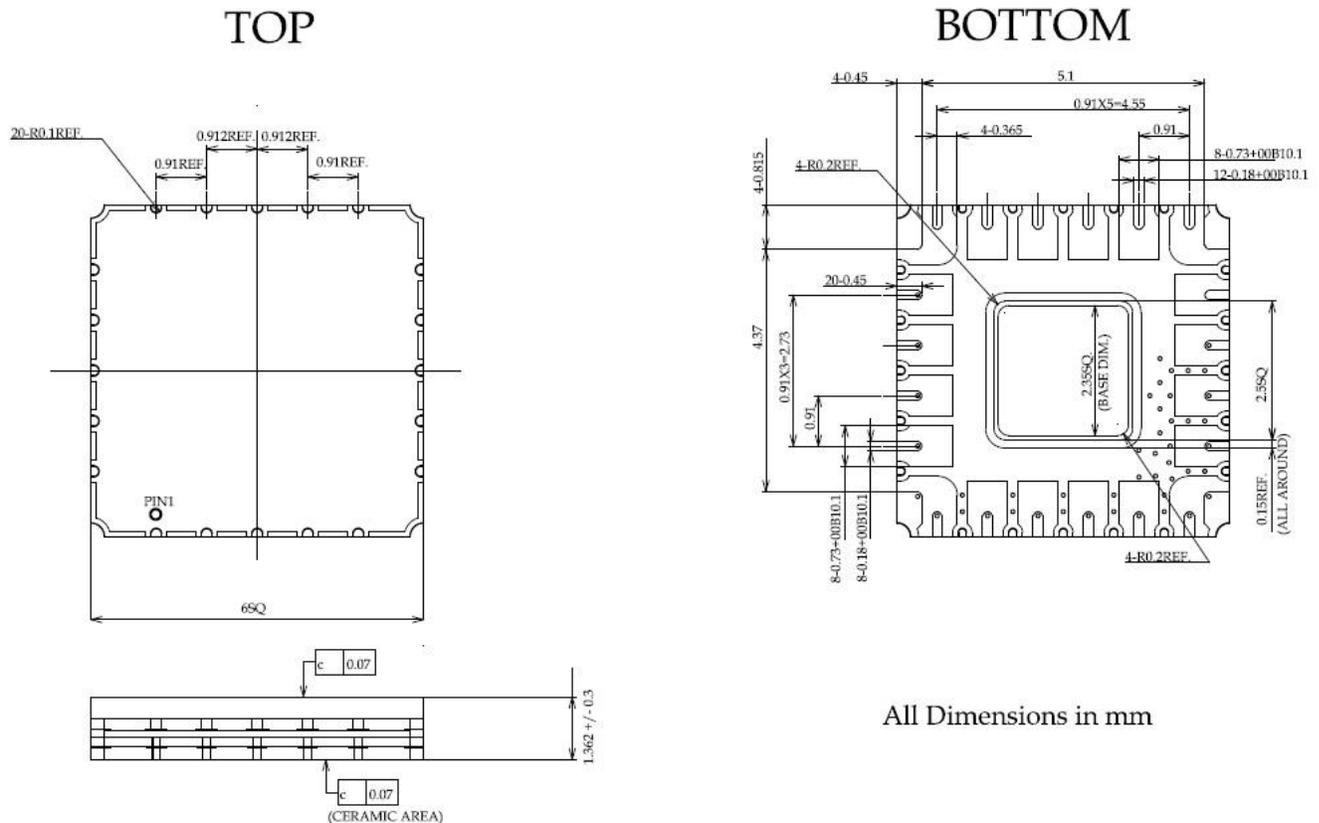


Fig. 20. CQFN44 Package Drawing (All Dimensions in mm)

## REVISION HISTORY

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.1.2	12-2025	Corrected description of Automatic adaptation mode activation
1.0.2	09-2024	First release based on test data
0.0.2	01-2024	Initial draft