ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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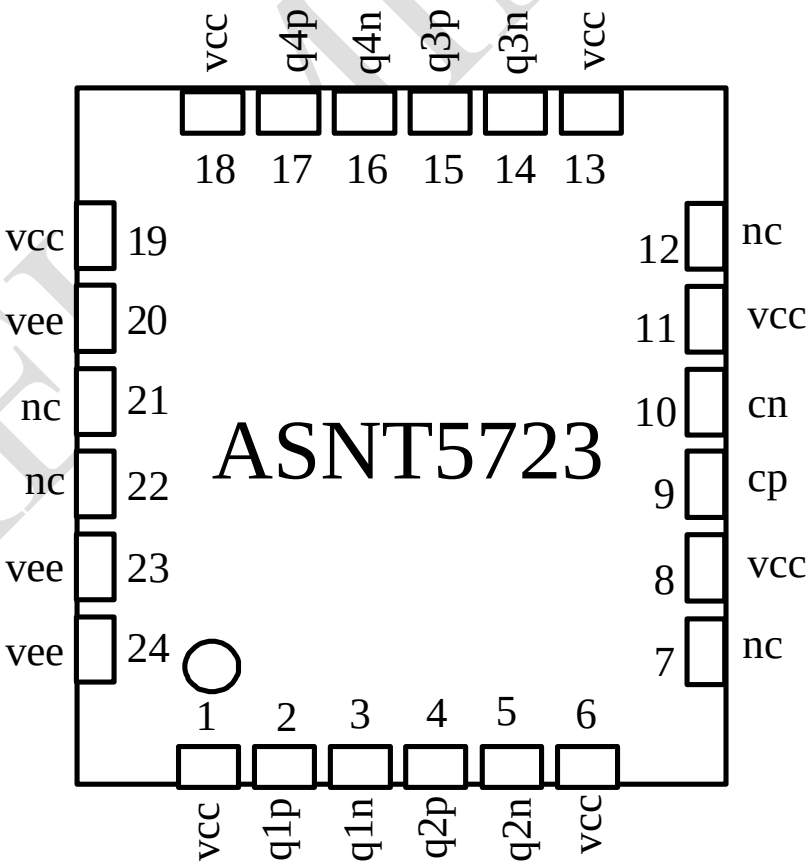
ASNT5723-PQC
DC-32*Gbps*/24*GHz* Signal Distributor 1-to-4

- High-speed broadband Digital Data/Clock Distributor
- One differential input signal port and four differential amplified output signal ports
- Fully differential CML input interface
- Fully differential CML output interfaces with 600*mV* single-ended swing
- Matched phase delays for all outputs
- Linearized output buffers for minimized undershoot/overshoot
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 850*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Standard QFN 24-pin package



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DESCRIPTION

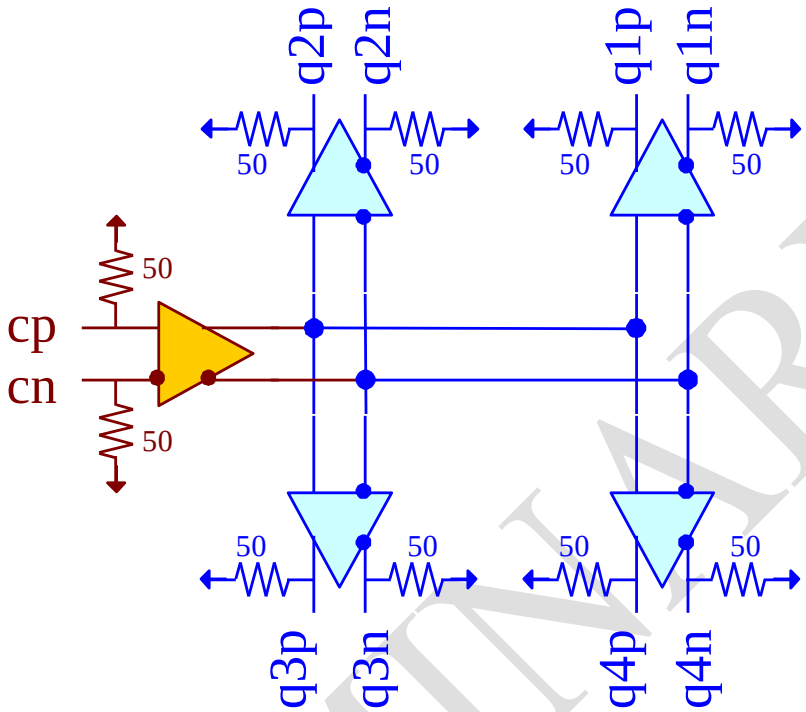

Fig. 1. Functional Block Diagram

This SiGe IC provides active broadband data/clock signal splitting and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can deliver four phase-matched copies of the broadband data/clock input signal cp/cn to four high-speed differential outputs q1p/q1n, q2p/q2n, q3p/q3n, q4p/q4n.

The part's I/O's support CML logic interface with on chip 50*Ohms* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.35	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cp	9	CML input	Differential high speed data/clock inputs with internal SE 50*Ohms* termination to vcc
cn	10		
q1p	2	CML output	Differential high speed data/clock outputs with internal SE 50*Ohms* termination to vcc. Require external SE 50*Ohms* termination to vcc
q1n	3		
q2p	4	CML output	Differential high speed data/clock outputs with internal SE 50*Ohms* termination to vcc. Require external SE 50*Ohms* termination to vcc
q2n	5		
q3p	15	CML output	Differential high speed data/clock outputs with internal SE 50*Ohms* termination to vcc. Require external SE 50*Ohms* termination to vcc
q3n	14		
q4p	17	CML output	Differential high speed data/clock outputs with internal SE 50*Ohms* termination to vcc. Require external SE 50*Ohms* termination to vcc
q4n	16		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)	1, 6, 13, 18, 19, 24
vee	Negative power supply (0*V* or -3.3*V*)	20, 23
nc	Not connected pins	7, 12, 21, 22

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee	220		290	*mA*	
Power consumption		850		*mW*	
Junction temperature	-40	25	125	*°C*	
HS data/clock input (cp/cn)					
Data rate	DC		32	*Gbps*	
Frequency	DC		24	*GHz*	
Swing (dvl)	50	300	600	*mV*	Differential or SE, p-p
Common mode level		vcc-dvl/2		*mV*	Must match for both inputs
Duty cycle	40	50	60	*%*	For clock signal
HS data/clock output (q1p/q1n, q2p/q2n, q3p/q3n, q4p/q4n)					
Data rate	DC		32	*Gbps*	
Frequency	DC		24	*GHz*	
Latency	25		40	*ps*	From the input to any output
Phase mismatch			2	*ps*	Between any two SE outputs
Logic “1” level		vcc-0.1		*V*	
Logic “0” level		vcc-0.7		*V*	With external 50*Ohm* DC termination
Rise/Fall Times	8		10	*ps*	20%-80%
Additive Jitter			2	*ps*	Peak-to-peak

PACKAGE INFORMATION

The chip die is housed in a custom q4-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply or power for the negative supply.

The part’s identification label is ASNT5723-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package’s manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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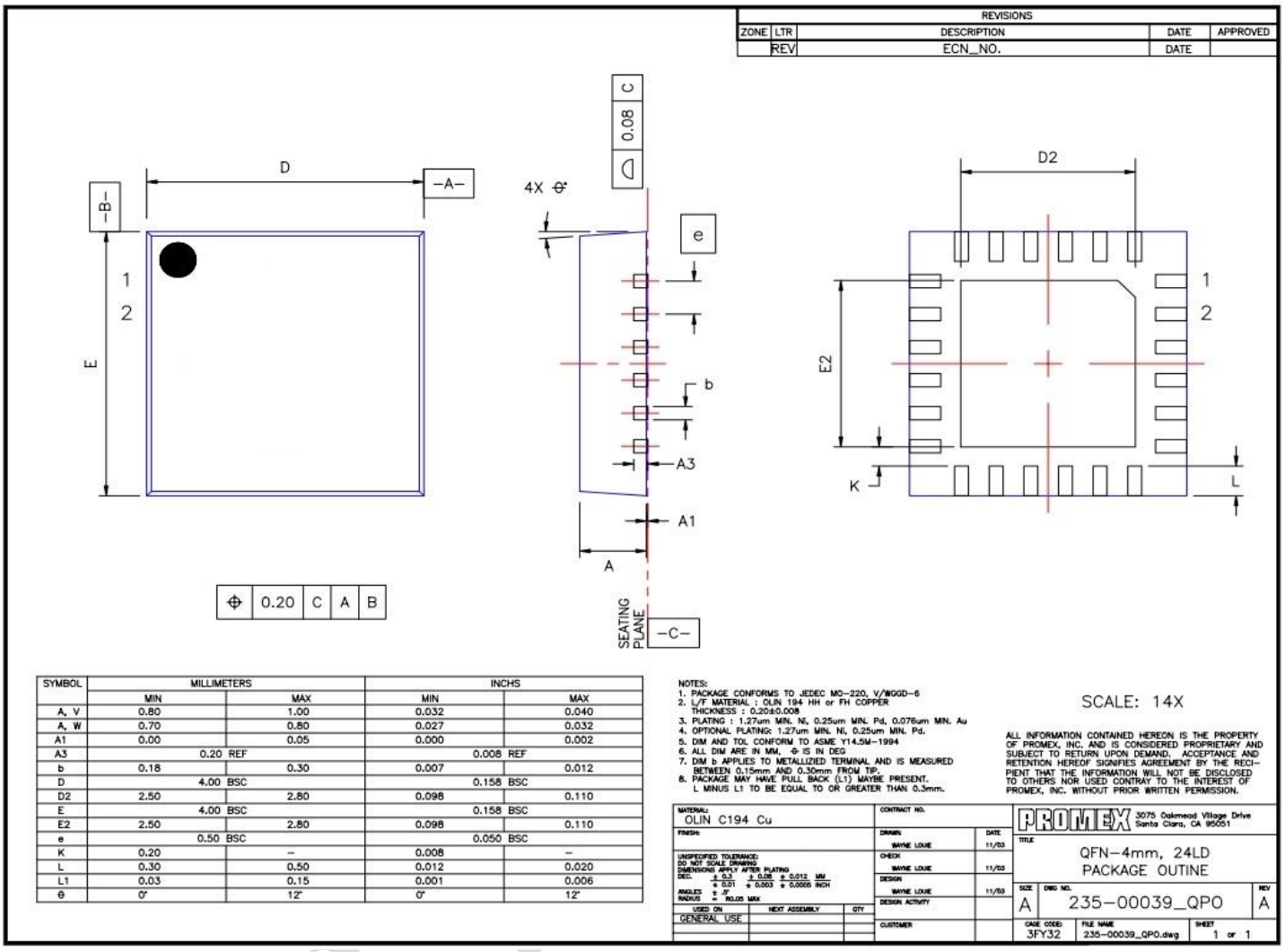

SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A, V	0.80	1.00	0.032	0.040
A, W	0.70	0.80	0.027	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.00 BSC		0.158 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.158 BSC	
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.050 BSC	
K	0.20	–	0.008	–
L	0.30	0.50	0.012	0.020
L1	0.03	0.15	0.001	0.006
θ	0°	12°	0°	12°

Fig. 2. QFN 24-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
0.0.2	04-2024	Preliminary release