ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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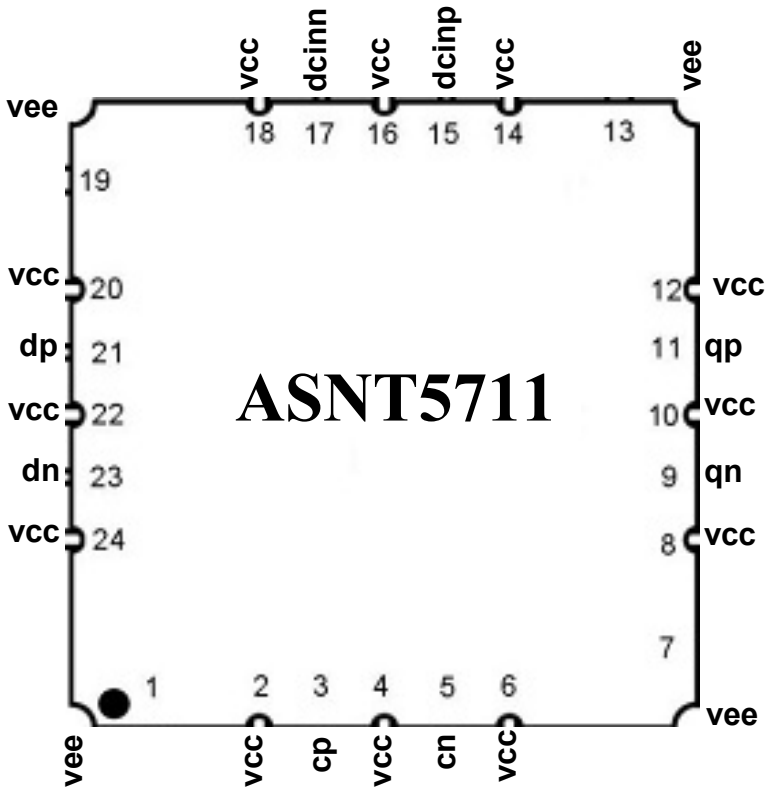
ASNT5711-KHC
DC-64*Gbps* D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock
- Input data common mode control
- 2*ps* set-up/hold time capability
- 88% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 530*mW*
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFN 24-pin package



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DESCRIPTION

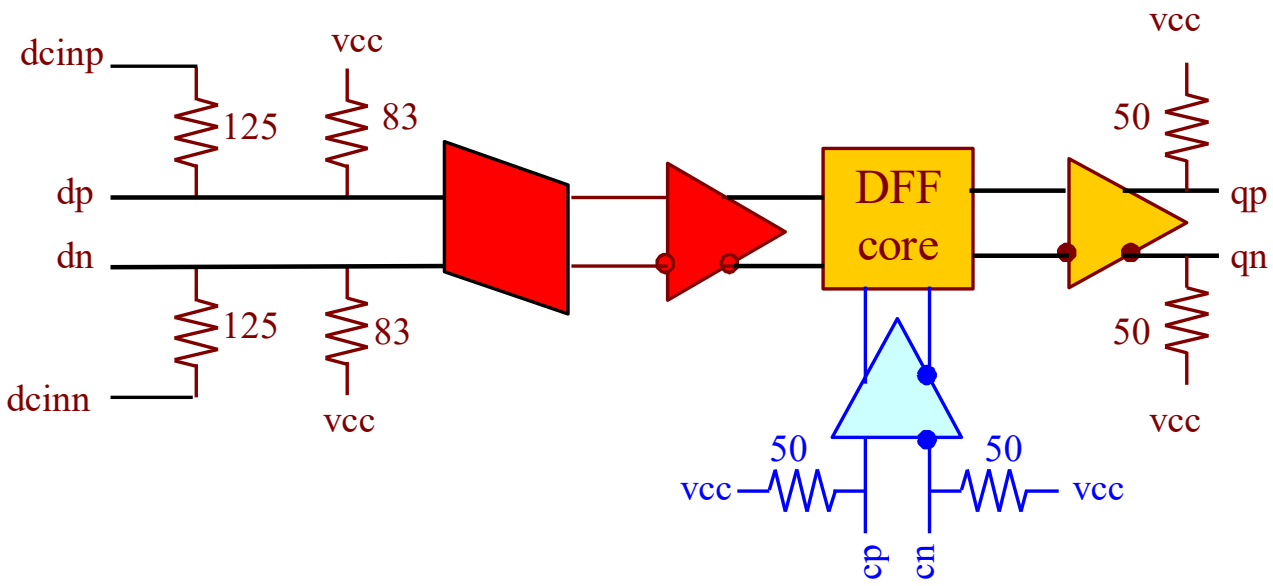

Fig. 1. Functional Block Diagram

The temperature stable ASNT5711-KHC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample a high-speed data signal dp/dn with a full-rate external clock cp/cn to create a full-rate retimed NRZ data output qp/qn. The internal DC common mode voltage levels on data inputs dp/dn can be adjusted by applying analog voltages to the control ports dcinp/dcinn.

The part's I/O's support the CML logic interface with an on chip equivalent 50*Ohm* termination and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION).

HS Clock Input Buffer

The buffer can accept high-speed signals at its differential CML input port cp/cn. It can also accept a single-ended signal with a threshold voltage applied to the unused pin. It can handle a wide range of input signal amplitudes. The buffer utilizes an on-chip single-ended 50*Ohm* termination to vcc for each input line.

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The buffer allows for adjustment of DC common-mode voltage levels of input ports dp/dn by manipulating voltages applied to the control ports dcinp/dcinn, respectively. For correct input internal

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termination, the ports dcinp/dcinn should be always connected to a power supply source, e.g. vcc if no shifts are required.

HS Data Output Buffer

The buffer receives high-speed serial data from the DFF core and converts it into a differential CML output signal qp/qn. Each buffer utilizes internal single-ended 50*Ohm* loads to vcc and requires single-ended 50*Ohm* external termination. The termination resistors can be connected from each output directly to vcc or through DC blocks to vee.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*) or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with a 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.60	*W*
Input Data Voltage Swing (SE)		1.0	*V*
Input Clk Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*°C*
Storage Temperature	-40	+100	*°C*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			Pin function	Default state	Termination
Name	No.	Type			
High-Speed I/Os					
dp	21	CML Input	Input data		SE 83*Ohms* to vcc and 125*Ohms* to dcinp/n respect.
dn	23				

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TERMINAL			Pin function	Default state	Termination
Name	No.	Type			
cp	3	CML Input	Input clock		SE 50*Ohms* to vcc
cn	5				
qp	11	CML Output	Output data.		SE 50*Ohms* to vcc. Require external SE 50*Ohms* to vcc
qn	9				
DC Controls					
dcinp	15	Analog voltage	Input data common mode voltage control	Connect to vcc!	125*Ohms* to corresponding inputs
dcinn	17				
Supply and Termination Voltages					
Name	**Description**		**Pin Number**		
vcc	Positive power supply (+3.3*V* or 0*V*)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24		
vee	Negative power supply (0*V* or -3.3*V*)		1, 7, 13, 19		

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc		0.0		*V*	External ground
vee	-3.1	-3.3	-3.5	*V*	±6%
*I*vcc		160	182	*mA*	
Power consumption		530	600	*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (dp/dn)					
Data rate	DC		64	*Gbps*	
Swing	0.05		0.80	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.7+sw/2		vcc+0.6-sw/2	*V*	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		64	*GHz*	
Swing	0.05		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.7		vcc+0.6-sw/2	*V*	Must match for both inputs
Duty Cycle	40	50	60	*%*	
Clock phase margin	86	88	90	*%*	For reliable data latching
HS Output Data (qp/qn)					
Data rate	DC		64	*Gbps*	
Jitter	0.8		1.2	*ps*	Peak-to-peak at 40*Gbps*
DC Input Controls (cdinp, cdinn)					
Max level		vcc		*V*	
Min level		vcc - 1.3		*V*	

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PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFN package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

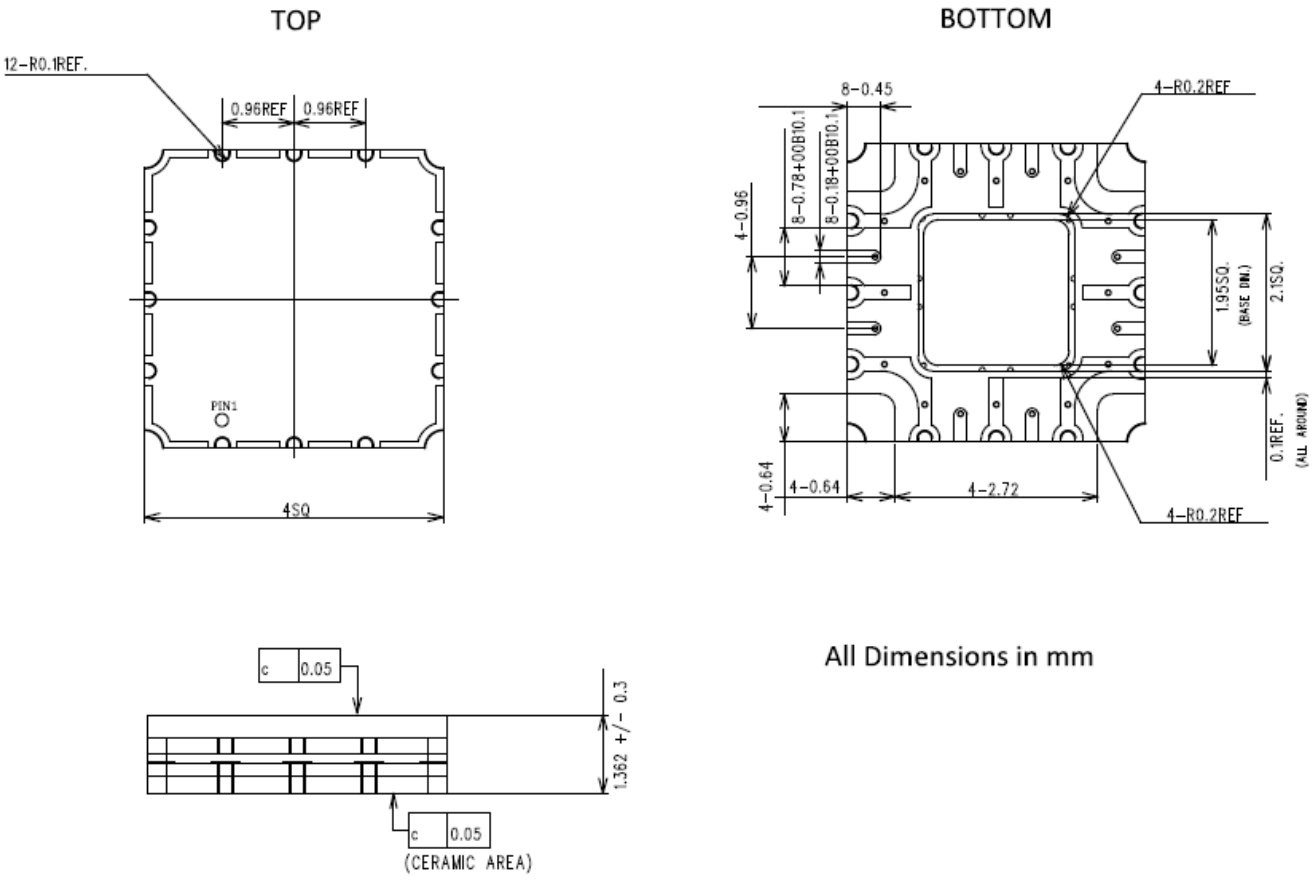

Fig. 2. CQFN 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT5711-KHC. The first 8 characters of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
1.2.2	01-2026	Added tested jitter values
1.1.1	12-2025	Corrected title (no amplitude adjustment)
1.0.2	11-2023	First release
0.0.1	04-2023	Preliminary release