ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
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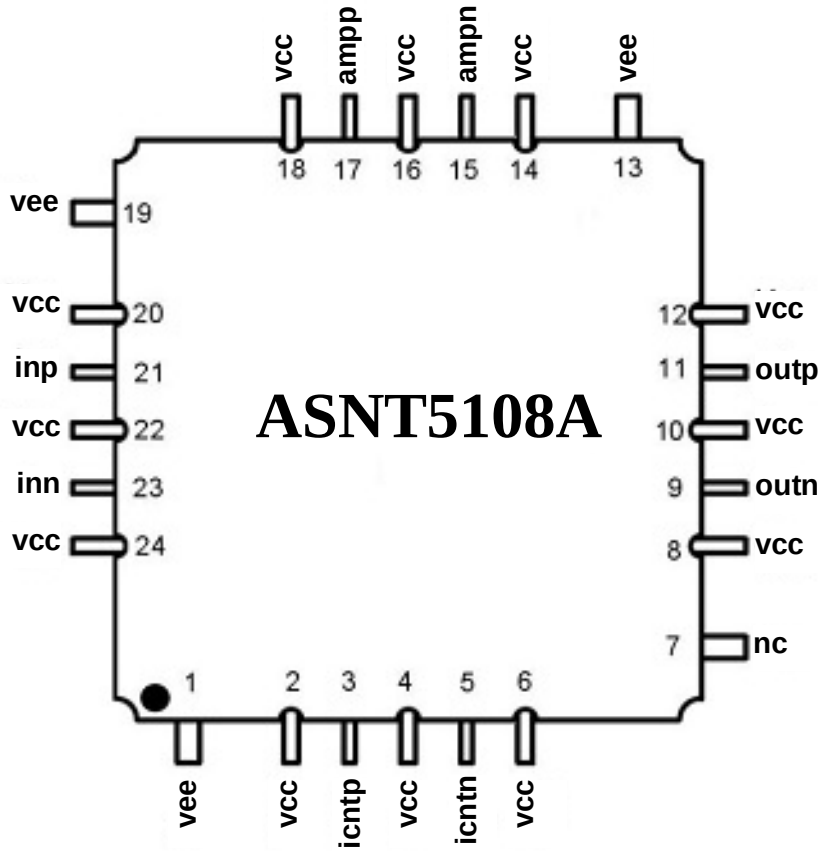
ASNT5108A-KMC
DC-30*Gbps*/24*GHz* Signal Phase Shifter with Amplitude Control

- Broadband (DC-30*Gbps*/DC-24*GHz*) tunable data/clock phase shifter
- Delay adjustment range over 160*ps*
- Fully differential CML input interfaces
- Fully differential CML output interface with adjustable SE amplitude from 0.0 to 1.0*V*
- 1*GHz* of bandwidth for the phase adjustment tuning ports
- 10*MHz* of bandwidth for the amplitude adjustment tuning ports
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 1.25*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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DESCRIPTION

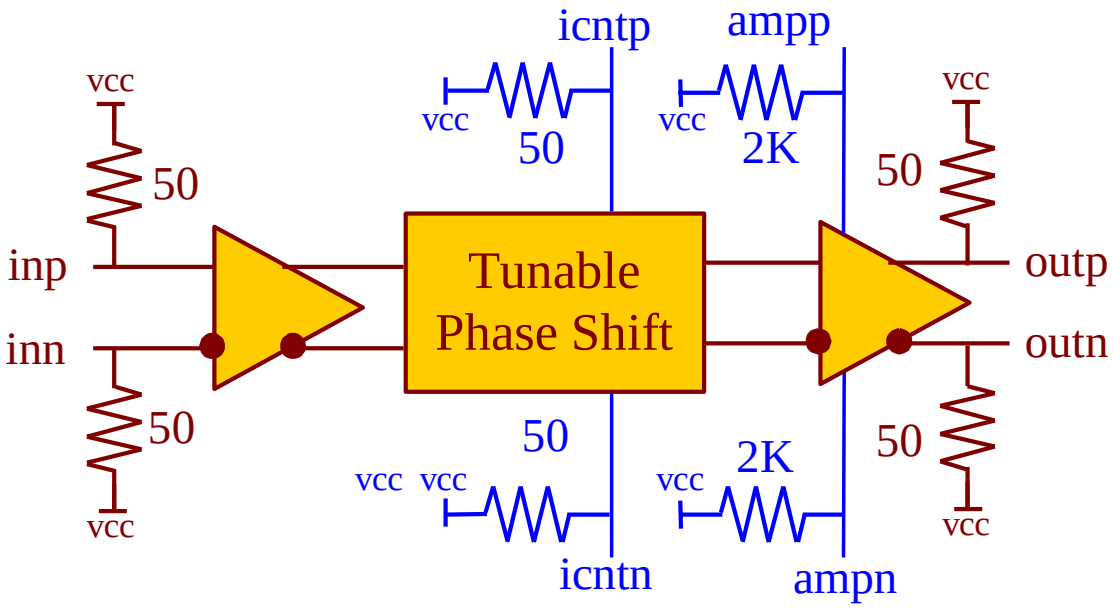

Fig. 1. Functional Block Diagram

The IC shown in Fig. 1 is a variable delay line that provides an adjustable delay of its differential output signal outp/outn in relation to its broadband input signal inp/inn. The delay adjustment range is temperature-stabilized. The delay is controlled through a wide-band differential tuning port icntp/icntn.

The part's output amplitude is controlled through a wide-band differential tuning port ampp/ampn.

The part's I/O's support the CML logic interface with on chip 50*Ohms* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

Delay Control Port

The delay is controlled through a wide-band differential tuning port icntp/icntn. There are three possible delay control options: (1) apply a differential signal with a certain voltage swing, (2) apply SE signals with the same swing to one or another control input while applying the required DC common voltage to the other input, (3) apply a SE signal with half the swing in turn to one and another control input and keep the other input at its default value of vcc. The delay control diagram is shown in Fig. 2.

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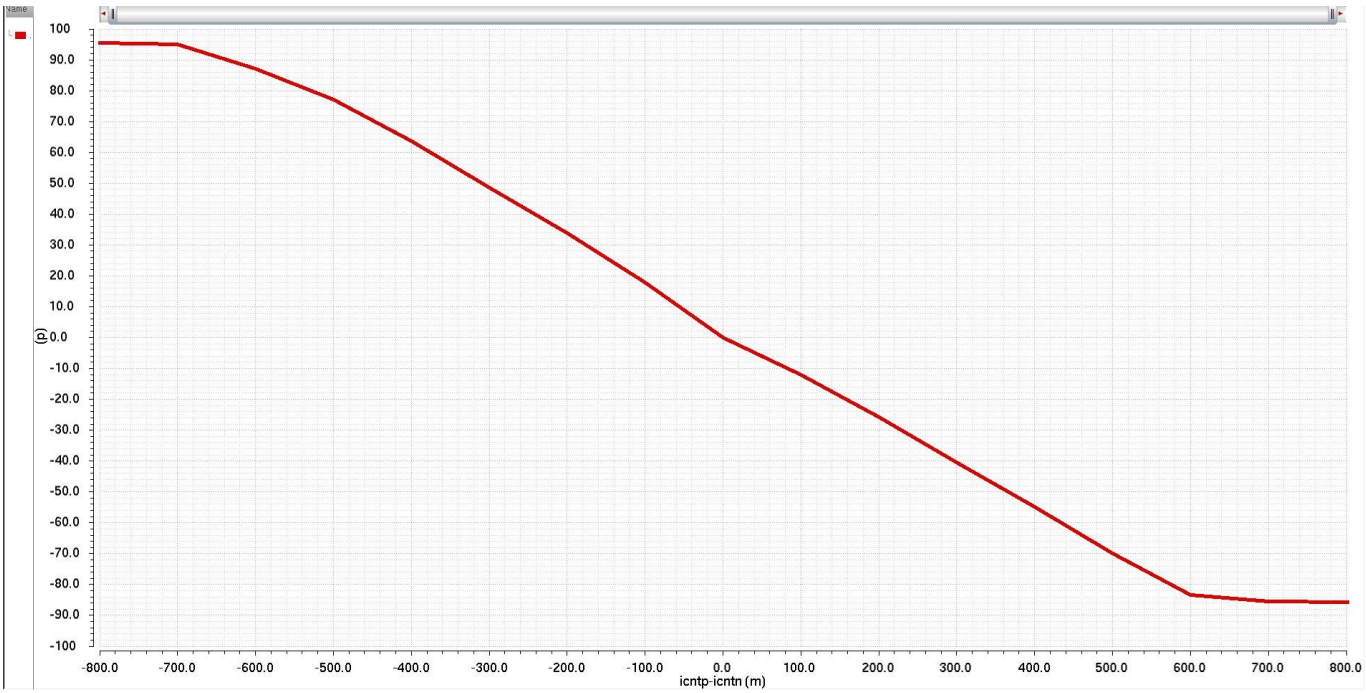

Fig. 2. Delay Control Diagram

Amplitude Control Port

The output amplitude is controlled through a wide-band differential tuning port ampp/ampn. The amplitude control diagram is shown in Fig. 3.

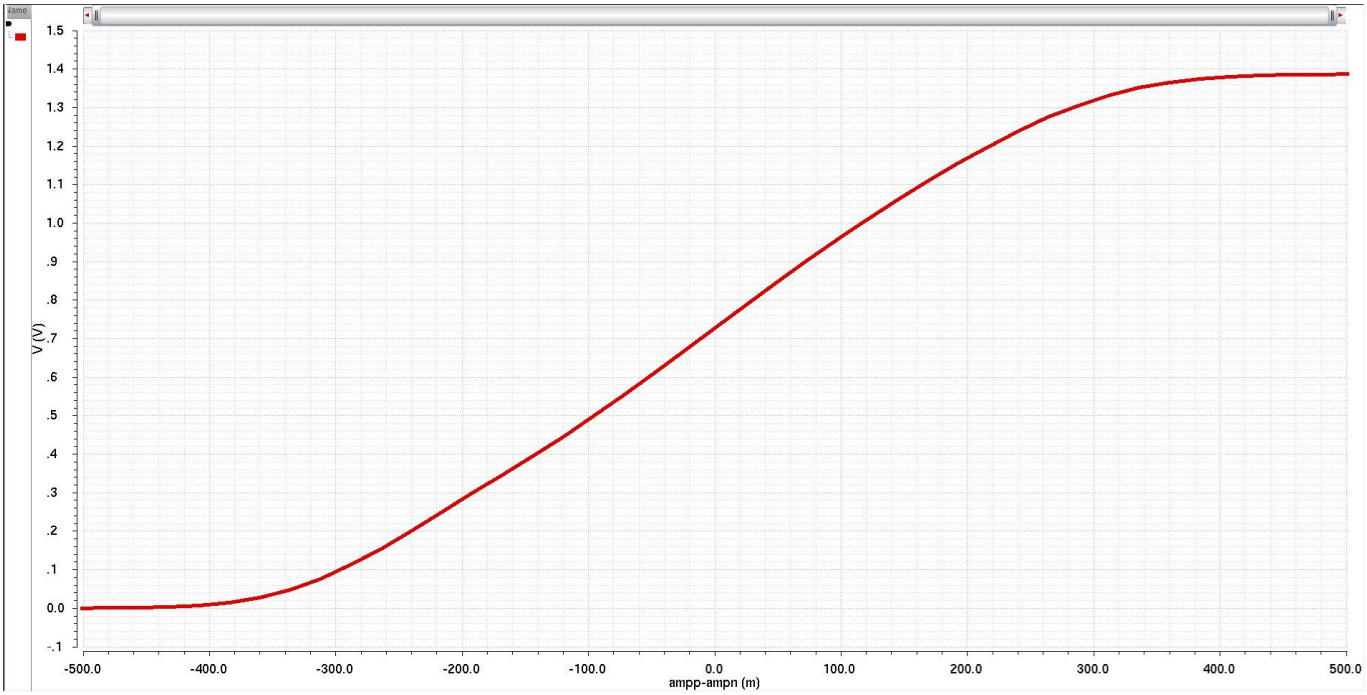

Fig. 3. Amplitude Control Diagram

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POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.5	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
ip	21	CML input	Differential high-speed signal inputs with internal SE 50*Ohms* termination to vcc.
in	23		
icntp	3	CML input	Differential high-speed control inputs with internal SE 50*Ohms* termination to vcc.
icntn	5		
ampp	17	Input	Differential low-speed control inputs with internal SE 2*KOhms* terminations to vcc.
ampn	15		
outp	11	CML output	Differential high-speed signal outputs with internal SE 50*Ohms* termination to vcc. Require external SE 50*Ohm* termination to vcc.
outn	9		
n/c	7	-	Not connected in the package

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply. (+3.3*V* or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply. (0*V* or -3.3*V*)	1, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee	340		400	*mA*	
Power consumption		1250		*mW*	
Junction temperature	-40	25	125	*°C*	

Data Rate	DC		30	*Gbps*	
Frequency	DC		24	*GHz*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Data/Clock (outp/outn)					
Data Rate	DC		30	*Gbps*	
Frequency	DC		24	*GHz*	
Logic "1" level		vcc		*V*	
Highest logic "0" level		vcc		*V*	With external 50*Ohms* DC termination and full range of ampp/ampn control.
Lowest logic "0" level	vcc-1.4		vcc-1.0	*V*	
Rise/Fall times	6		10	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak
Duty cycle	45	50	55	*%*	For clock signal
Output-to-Input Delay					
Adjustment range		180		*ps*	At 1*GHz*
		160		*ps*	At 24*GHz*
					For the full range of icntp/icntn control signals
Phase shift stability	-2		2	*ps*	0-125°C
Phase Shift Control port (icntp/icntn)					
Bandwidth	DC		1000	*MHz*	
SE voltage level	vcc-600		vcc	*mV*	Half control range when the opposite pin is at vcc.
SE voltage level	vcc-1200		vcc	*mV*	Full control range when the opposite pin is at vcc-0.6*V*.
Differential swing	0		1200	*mV*	Peak-peak. Full control range.
CM Level		vcc-(Diff. swing)/4		*V*	In differential mode
Output Amplitude Control port (ampp/ampn)					
Bandwidth	DC		10	*MHz*	
SE voltage level	vcc-400		vcc	*mV*	Half control range when the opposite pin is at vcc.
SE voltage level	vcc-800		vcc	*mV*	Full control range when the opposite pin is at vcc-0.4*V*.
Differential swing	0		800	*mV*	Peak-peak. Full control range.
CM Level		vcc-(Diff. swing)/4		*V*	In differential mode

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PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 4. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

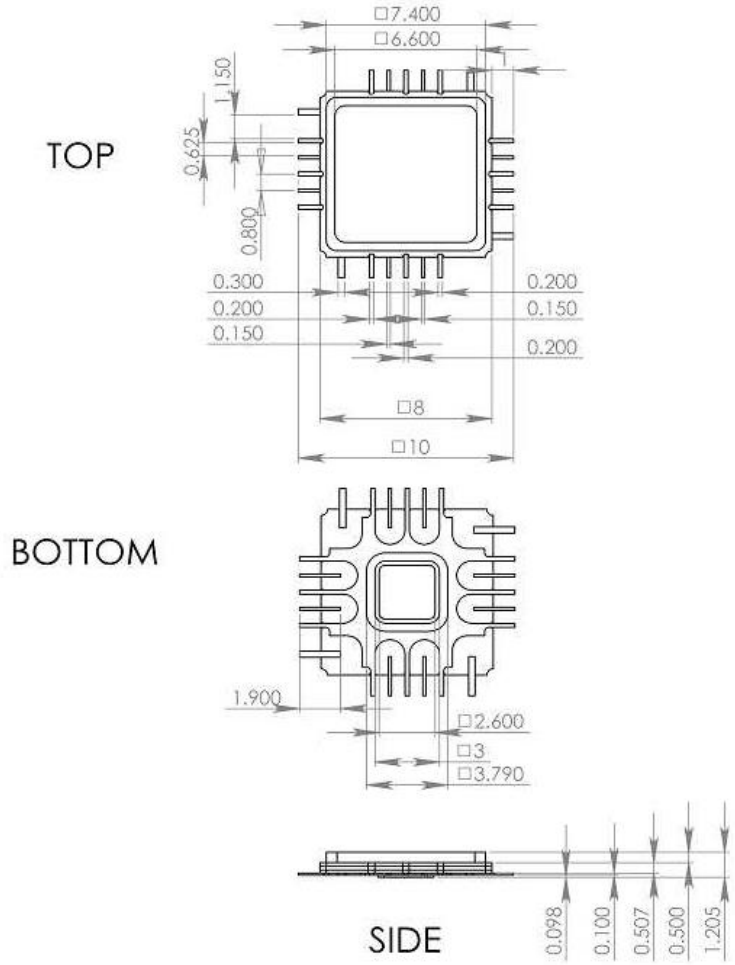

Fig. 4. CQFP 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT5108A-KMC. The first 9 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
1.0.2	10-2023	First release
0.0.1	03-2022	Preliminary release