ADSANTEC
Ultra High-Speed Mixed Signal ASICs

*Advanced Science And Novel Technology Company, Inc.*
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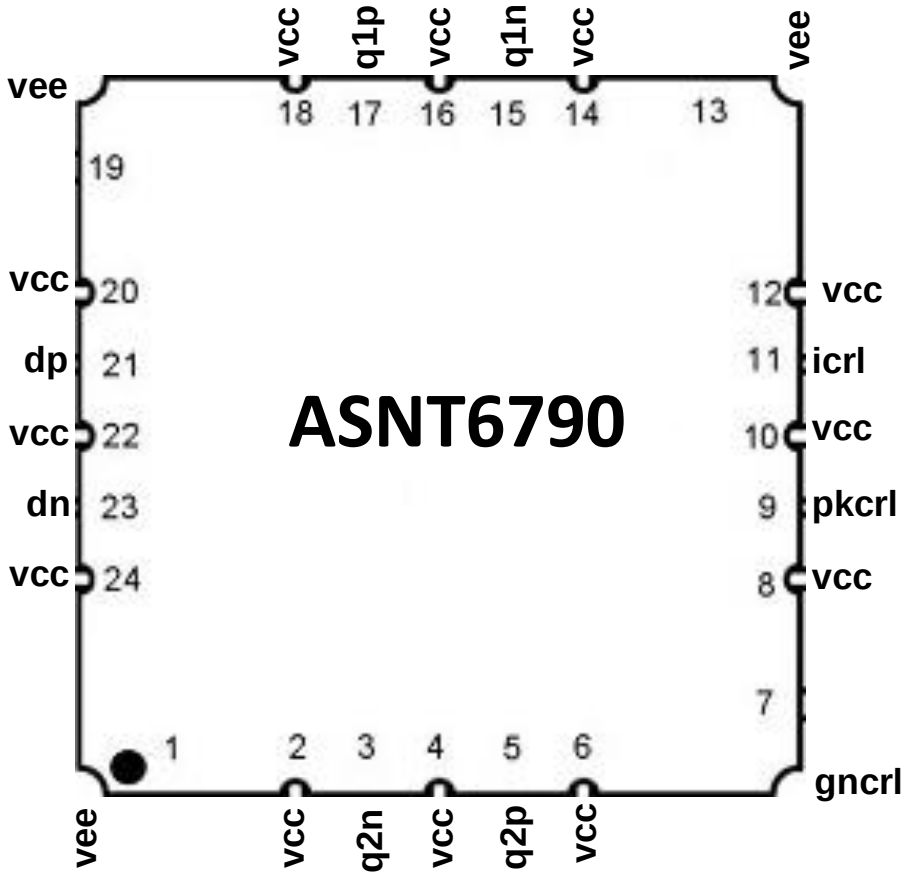
# ASNT6790-KHC
# DC-35*GHz* 1-to-2 Analog Signal Splitter

- DC to 35*GHz* broadband linear signal splitter
- Exhibits an extra-flat frequency response ideal for PAM3 and PAM4 applications
- One differential CML-type input port and two phase-matched differential CML-type output ports
- Single ended input linearity range up to $0.6V_{pk\text{-}pk}$ and differential input linearity up to $1.2V_{pk\text{-}pk}$
- Adjustable gain around from -4*dB* to +3*dB*
- Adjustable high-frequency peaking
- Adjustable internal currents for power consumption and bandwidth control
- Low jitter and limited temperature variation over industrial temperature range
- Single +3.6*V* or -3.6*V* power supply
- Power consumption: 760*mW* typical
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFN 24-pin package



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# DESCRIPTION

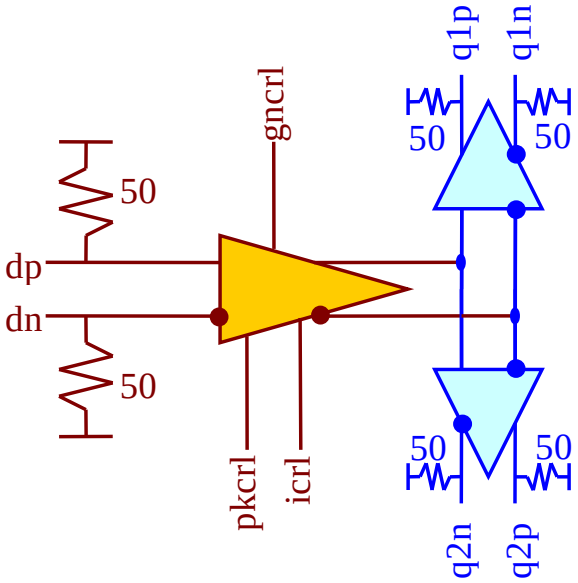


*Fig. 1. Functional Block Diagram*

The temperature stable ASNT6790-KHC 1-to-2 analog signal splitter is intended for use in high-speed interleaved ADCs or similar systems. Its extra-flat frequency response is ideal for PAM3 and PAM4 signals. The IC shown in Fig. 1 can receive a broad-band analog signal at its differential input dp/dn and effectively distribute it to two separate phase matched differential outputs q1p/q1n, q2p/q2n with a nominal gain of 0*dB*. A low-speed analog current control icrl is available for power consumption and bandwidth adjustments. A low-speed analog control pkcrl is available for peaking adjustments at higher frequencies (above 25*GHz*). A relatively flat frequency response with variation of no more than ±0.5*dB* within DC-to-30*GHz* can be achieved with these two control voltages. Another low-speed analog control gncrl is available for gain adjustment. A nominal gain of 0*dB* can be achieved for all corner, voltage, and temperature variations.

The part's I/O's support the CML logic interface with on chip 50*Ohms* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically.

# POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.6*V*), or positive supply (vcc = +3.6*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.6*V*.**

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# TYPICAL PERFORMANCE CHARACTERISTICS

At default values and with lower current/power consumption, the frequency responses of ASNT6790-KHC are shown in Fig. 2.

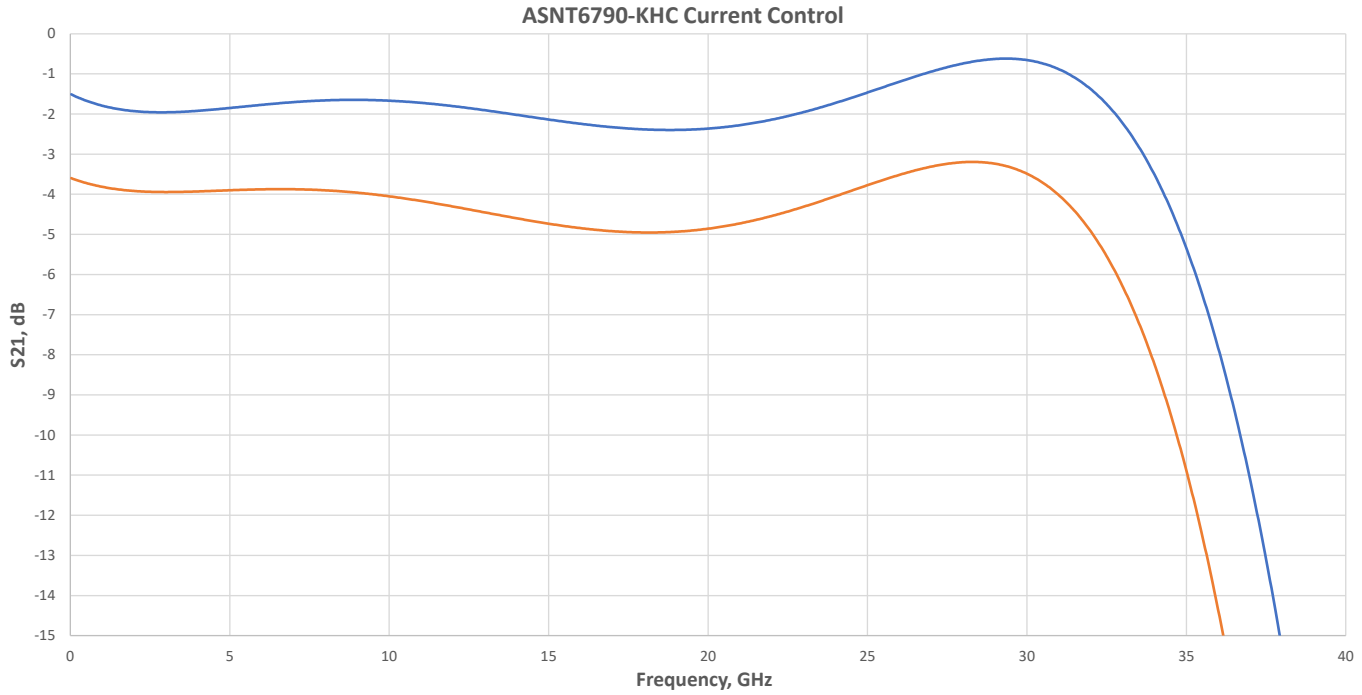


*Fig. 2. Frequency Response at **Lower Current/Power**, **Default Controls***

The frequency responses at different gain controls are shown in Fig. 3.

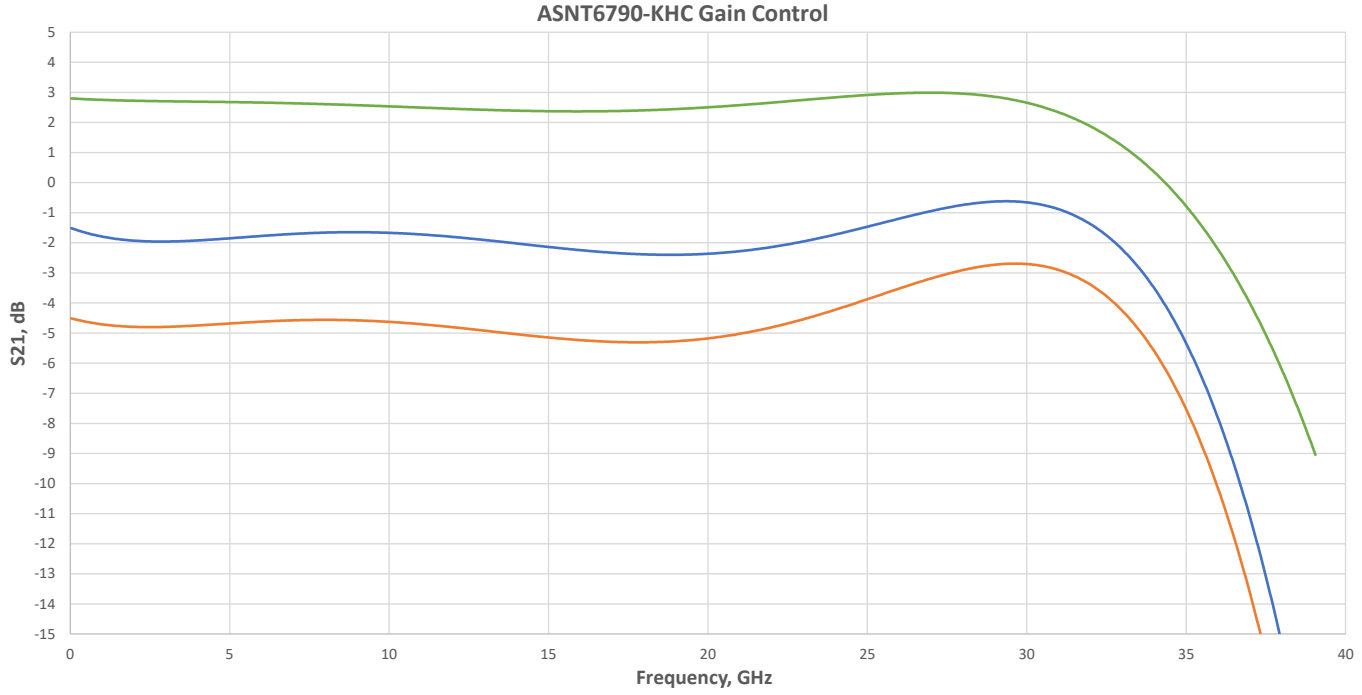


*Fig. 3. Frequency Response at **Minimum Gain**, **Default**, and **Maximum Gain***

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The frequency responses at different peaking controls are shown in Fig. 4.

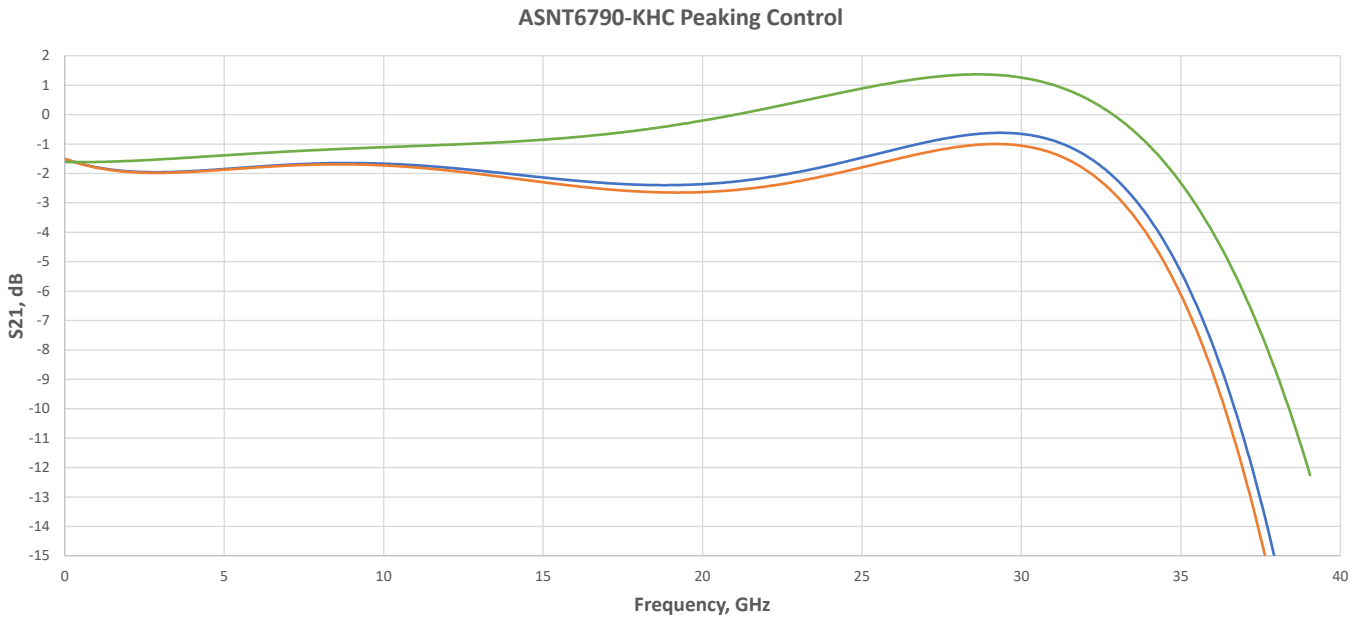


*Fig. 4. Frequency Response at **Minimum Peaking**, **Default**, and **Maximum Peaking***

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# PAM4 SIGNAL EYE PROPAGATION

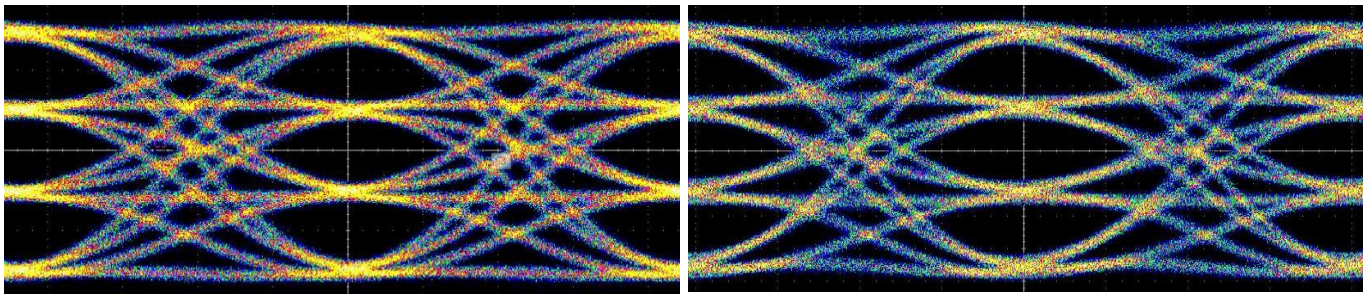

*Fig.5. PAM4 at 25Gbaud, 800mV Differential Peak-Peak, Left: Input, Right: Output*

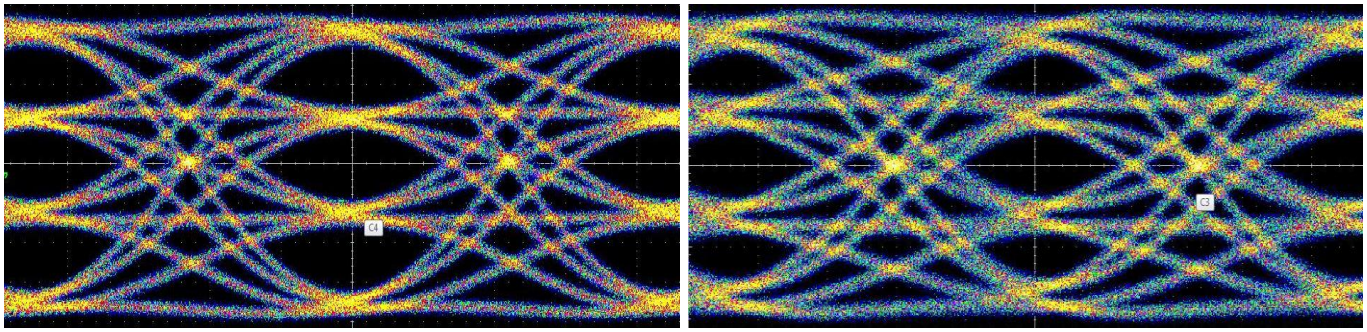

*Fig.6. PAM4 at 32Gbaud, 800mV Differential Peak-Peak, Left: Input, Right: Output*

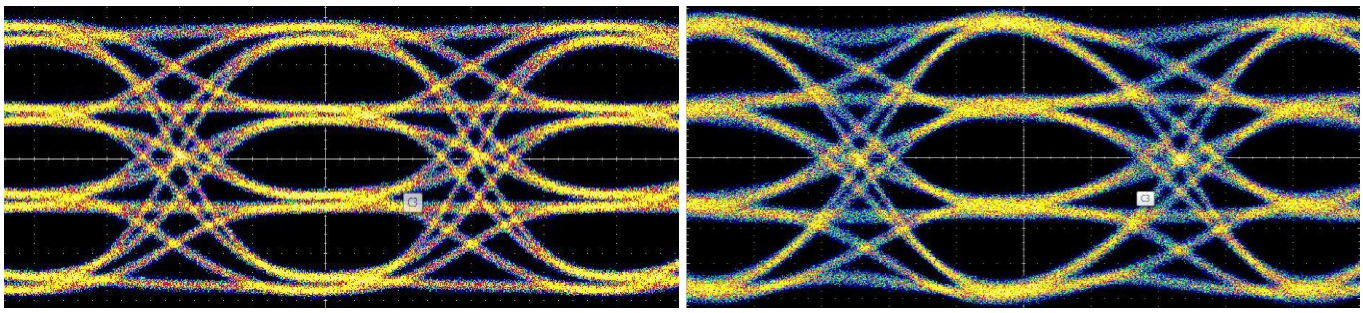

*Fig.7. PAM4 at 25Gbaud, 1200mV Differential Peak-Peak, Left: Input, Right: Output*

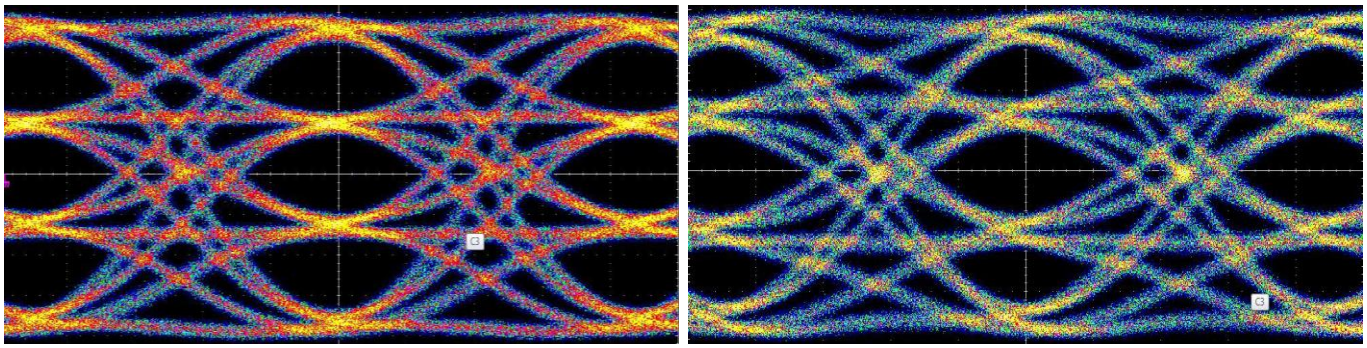

*Fig.8. PAM4 at 32Gbaud, 1200mV Differential Peak-Peak, Left: Input, Right: Output*

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# ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

*Table 1. Absolute Maximum Ratings*

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply Voltage (vee) | | -3.9 | *V* |
| Power supply current | | 300 | *mA* |
| Input Voltage | vcc-1.0 | vcc+0.4 | *V* |
| RF Input Voltage Swing (SE) | | 0.8 | *V* |
| Analog control voltages | vee | vcc | *V* |
| Case Temperature | | +90 | *ºC* |
| Storage Temperature | -40 | +100 | *ºC* |
| Operational Humidity | 10 | 98 | *%* |
| Storage Humidity | 10 | 98 | *%* |

# TERMINAL FUNCTION

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| **Name** | **No.** | **Type** | |
| dp | 21 | CML input | Differential high-speed data inputs with internal SE 50*Ohms* termination to vcc |
| dn | 23 | | |
| q1p | 17 | CML output | Differential high-speed data outputs with internal SE 50*Ohms* termination to vcc. Require external SE 50*Ohms* termination to vcc |
| q1n | 15 | | |
| q2p | 5 | CML output | |
| q2n | 3 | | |
| gncrl | 7 | Analog Control | Analog gain control with internal 15*KOhms* termination to vcc and 35*KOhms* termination to vee. |
| pkcrl | 9 | | Analog peaking control with internal 48*KOhms* termination to vcc and 55*KOhms* termination to vee. |
| icrl | 11 | | Analog current control with internal 24*KOhms* termination to vcc and 84.5*KOhms* termination to vee. |

| Supply and Termination Voltages | | |
|---|---|---|
| **Name** | **Description** | **Pin Number** |
| vcc | Positive power supply (+3.6*V* or 0) | 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24 |
| vee | Negative power supply (0*V* or -3.6*V*) | 1, 13, 19 |

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# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| vee | -3.2 | -3.6 | -3.8 | *V* | -12%, +6% |
| vcc | | 0.0 | | *V* | External ground |
| *I*vee | 100 | 210 | 250 | *mA* | At max. control range |
| Power consumption | 320 | 755 | 950 | *mW* | At max. control range |
| Junction temperature | -25 | 50 | 125 | *°C* | |
| **Input Analog (dp/dn)** | | | | | |
| Bandwidth | DC | | 35 | *GHz* | -3*dB* |
| Common mode voltage level | | vcc | | *V* | Internally generated |
| Single-ended voltage swing, pk-pk; unused input not connected or AC terminated | | | 600 | *mV* | THD < 0.8% at 2*GHz* |
| | | | 600 | *mV* | THD < 0.4% at 5*GHz* |
| | | | 600 | *mV* | THD < 1.1% at 10*GHz* |
| Single-ended voltage swing, pk-pk; unused input not connected or AC terminated | | | 1.2 | *V* | THD < 4% at 2*GHz* |
| | | | 1.2 | *V* | THD < 2.3% at 5*GHz* |
| | | | 1.2 | *V* | THD < 3.6% at 10*GHz* |
| Input Noise Density | | TBD | | *nV*/sqrt(*Hz*) | |
| S11 | | TBD | | *dB* | at 3*GHz* |
| | | TBD | | *dB* | at 10*GHz* |
| | | TBD | | *dB* | at 20*GHz* |
| | | TBD | | *dB* | at 25*GHz* |
| **Gain Control Signal (gncrl)** | | | | | |
| Control range | vee+2 | | vee+3.6 | *V* | |
| Default voltage level | | vee+2.5 | | *V* | at ±3.6*V* supply |
| Gain adjustment | -4 | 0 | 3 | *dB* | |
| **Peak Control Signal (pkcrl)** | | | | | |
| Control range | vee+1.5 | | vee+2.6 | *V* | |
| Default voltage level | | vee+1.9 | | *V* | at ±3.6*V* supply |
| Peaking adjustment | 0 | | 3 | *dB* | at 28GHz |
| **Current Control Signal (icrl)** | | | | | |
| Control range | vee+2.3 | | vee+3.3 | *V* | |
| Default voltage level | | vee+2.8 | | *V* | at ±3.6*V* supply |
| Current adjustment | 100 | 210 | 250 | *mA* | |
| **Output Analog (q1p/q1n, q2p/q2n)** | | | | | |
| Common mode level | | vcc-0.6 | | *V* | With external 50*Ohms* DC termination |
| Small signal differential gain | | 0 | | *dB* | up to 30*GHz* |
| Gain variation with optimal peaking control settings | | ±0.5 | | *dB* | Up to 30*GHz* |
| Output referred 1*dB* Compression Point | | >6 | | *dBm* | Single-Ended, 20*Gbps* |

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# PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFN package shown in Fig. 9. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

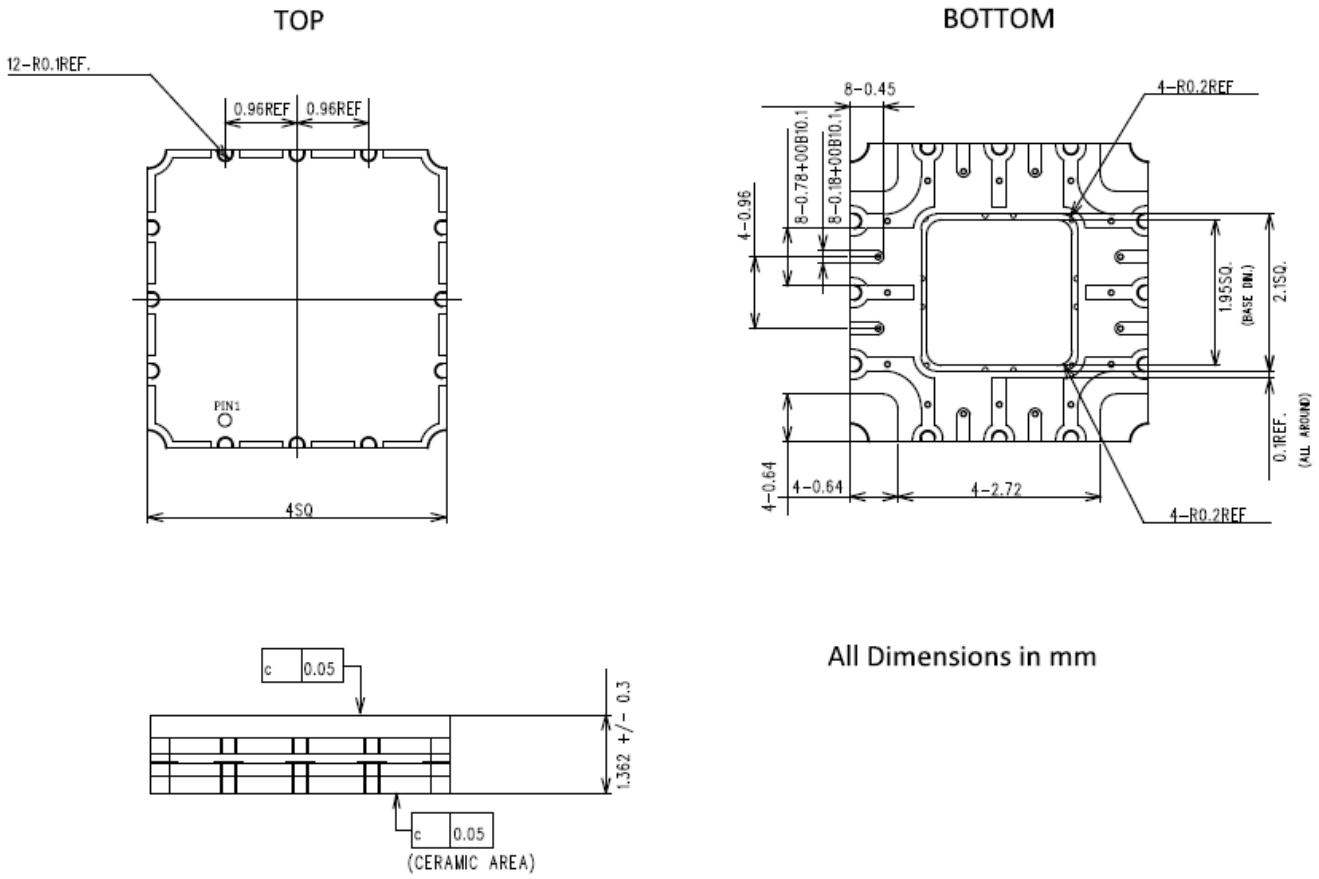


*Fig. 9. CQFN 24-Pin Package Drawing (All Dimensions in mm)*

The part's identification label is ASNT6790-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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# REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 1.1.2 | 02-2025 | Updated part description |
| 1.0.2 | 09-2023 | First release |