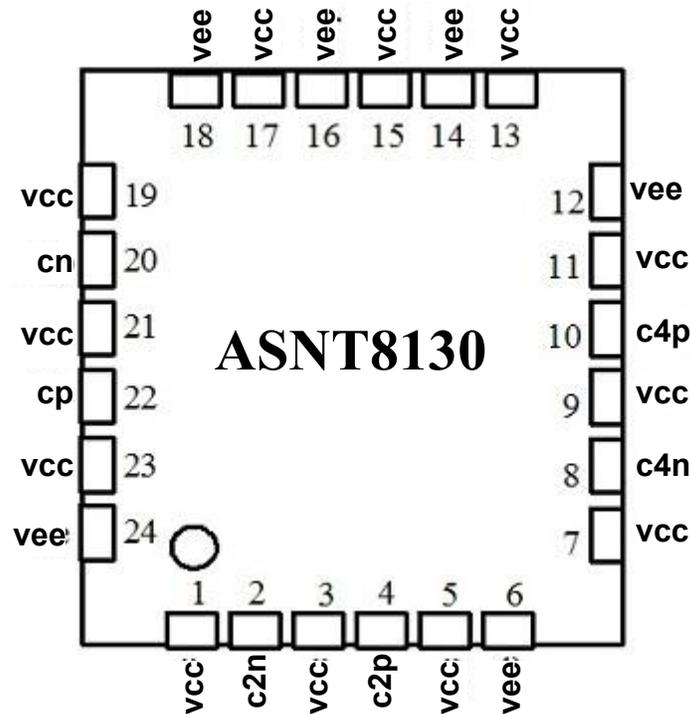




ASNT8130-PQC

32GHz High-Sensitivity Divider by 2 and by 4

- Wide frequency range from DC to 32GHz
- Divided-by-2 and divided-by-4 outputs
- 50% duty cycle of the divided clock signals
- Fully differential CML input interface
- Fully differential CML output interfaces
- Single +3.3V or -3.3V power supply
- Industrial temperature range
- Power consumption of 265mW at full operational speed
- Standard MLF/QFN 24-pin package





DESCRIPTION

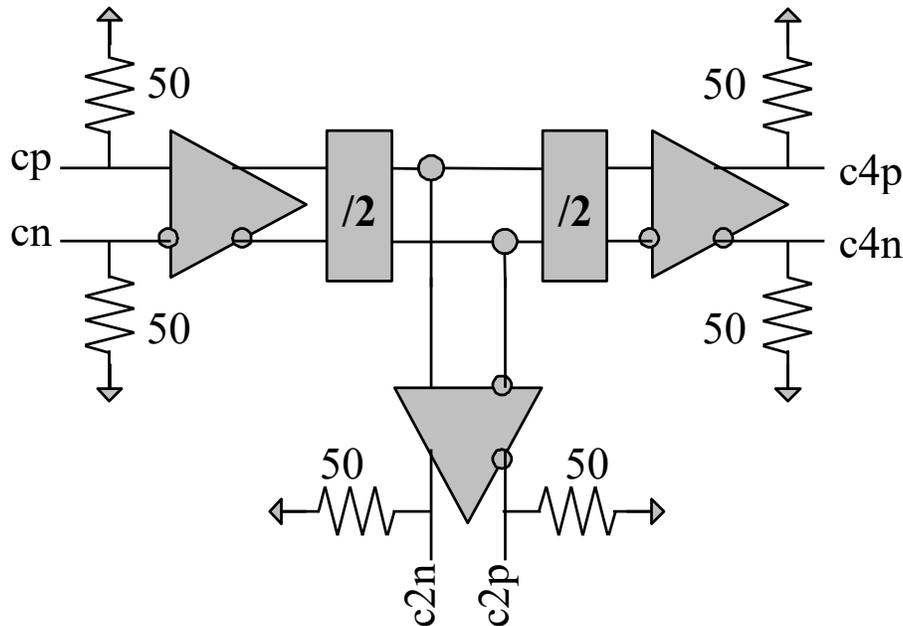


Fig. 1. Functional Block Diagram

ASNT8130-PQC is a high-speed, low-power divider by-2 and by-4 with increased sensitivity. The part shown in *Fig. 1* accepts a CML input clock signal (cp/cn) with the speed from DC to maximum operational frequency and provides clean 50% duty cycle output signals with divided-by-2 (c2p/c2n) and divided-by-4 (c4p/c4n) frequency. The part's I/Os support the CML logic interface with on chip 50 Ohms termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also **POWER SUPPLY CONFIGURATION**).

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0V = ground and vee = -3.3V), or a positive supply (vcc = +3.3V and vee = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50 Ohms termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0V and vee = -3.3V.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in *Table 1* may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).



Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.35	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
cp	22	CML input	Differential clock input with internal SE 50Ohms termination to VCC.
cn	20		
c2p	4	CML output	Differential divided clock outputs. Require external SE 50Ohms termination to VCC.
c2n	2		
c4p	10		
c4n	8		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply. (+3.3V or 0V)		1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23
vee	Negative power supply. (0V or -3.3V)		6, 12, 14, 16, 18, 24



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I _{vee}		80		mA	
Power consumption		265		mW	
Junction temperature	-25	50	125	°C	
HS Input Clock (cp/cn)					
Frequency	0		32	GHz	
Swing	60		800	mV	Differential or SE, p-p
CM Voltage Level	vcc-0.8	vcc-0.2	vcc	mV	Must match for both inputs
Output Divided Clock (c2p/c2n, c4p/c4n)					
Frequency <i>f</i> ₂	0		16	GHz	For c2 out signal
Frequency <i>f</i> ₄	0		8	GHz	For c4 out signal
Logic “1” level		vcc		V	
Logic “0” level		vcc-0.35		V	With external 50Ohms DC termination
Duty cycle	45	50	55	%	
Additive Jitter		TBD		ps	Peak-to-peak

PACKAGE INFORMATION

The die is housed in a standard 24-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to ground to help dissipate heat generated by the chip during operation.

The part’s identification label is ASNT8130-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package’s manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

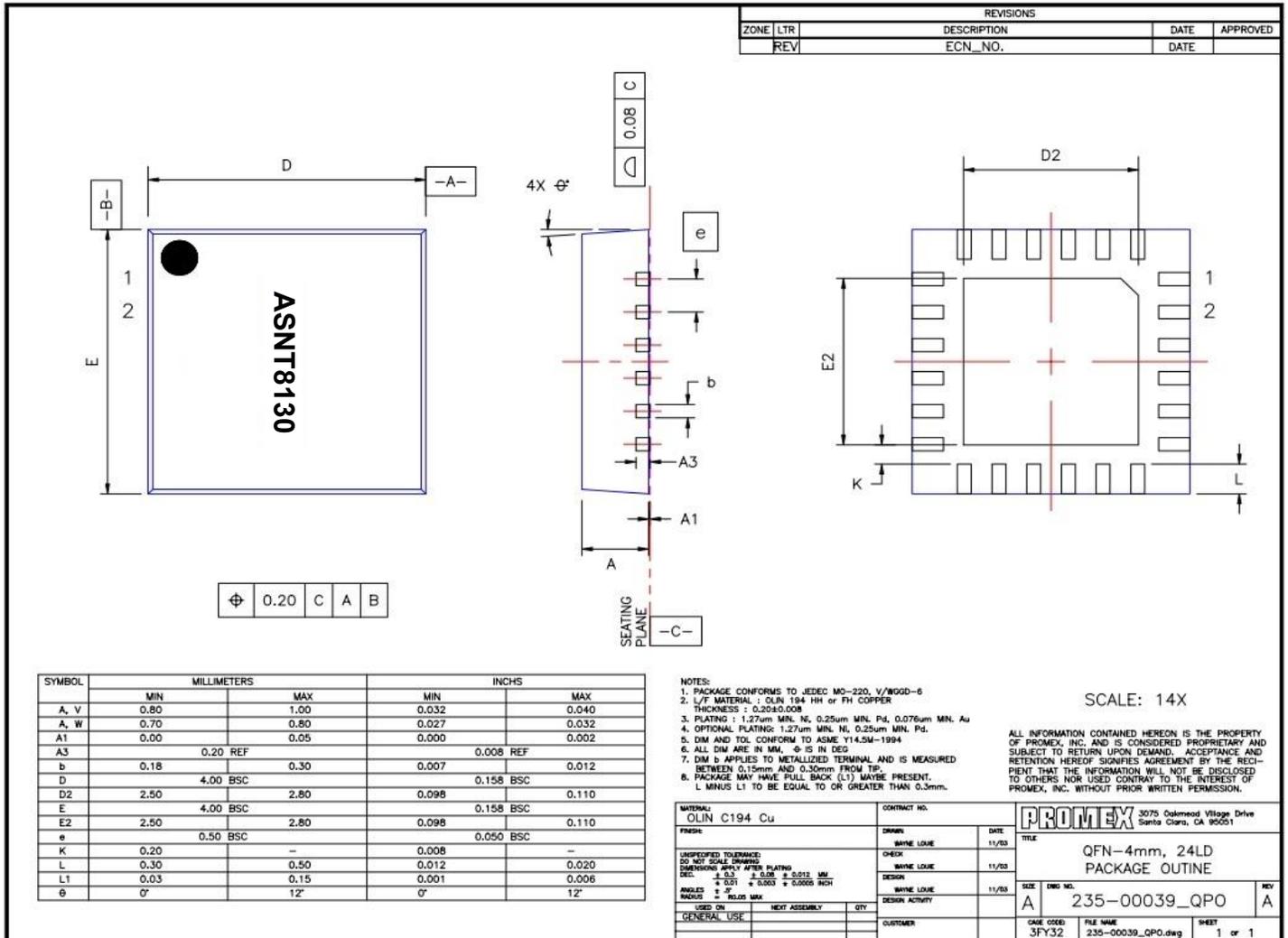


Fig. 2. QFN 24-Pin Package Drawing (All Dimensions in mm)



REVISION HISTORY

Revision	Date	Changes
2.6.2	02-2026	Updated block diagram
2.5.2	09-2017	Corrected Electrical Characteristics Updated Letterhead Updated Formatting
2.4.1	07-2015	Updated RoHS Information
2.3.1	03-2013	Corrected title Corrected description Corrected specification of the output swing
2.2.1	01-2013	Correction: output Diff Swing instead of SE.
2.1.1	01-2013	Corrected Absolute Maximum Ratings. Corrected current and power consumption. Corrected format.
2.0.1	06-2012	Added pin out drawing Added Power Supply Configuration text Added Absolute Maximum Ratings table Revised Electrical Characteristics section Added Package Information section Added Revision History
1.0	09-2011	First release