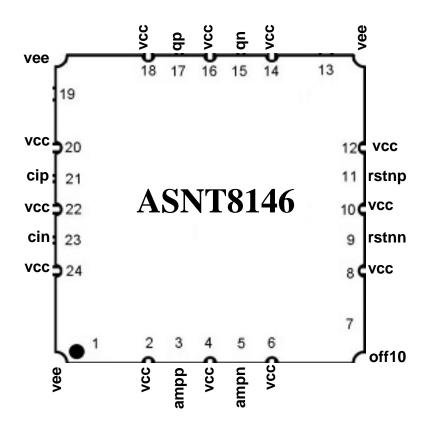


Ultra High-Speed Mixed Signal ASICs

Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940 www.adsantec.com

ASNT8146-KHC Generator of DC-to-32*Gb/s* PRBS with Selectable Polynomials and Output Amplitude Control

- Full-length (2⁹-1) or (2¹⁰-1) pseudo-random binary sequence (PRBS) generator
- Selectable power of the Polynomial
- DC to 32*Gb/s* output data rate
- External output amplitude control
- Asynchronous reset signal for elimination of the "all zeros" initial state
- Fully differential CML input interface
- Fully differential CML output interface
- Single +3.3V or -3.3V power supply
- Power consumption: 1220mW
- Custom CQFN 24-pin package





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DESCRIPTION

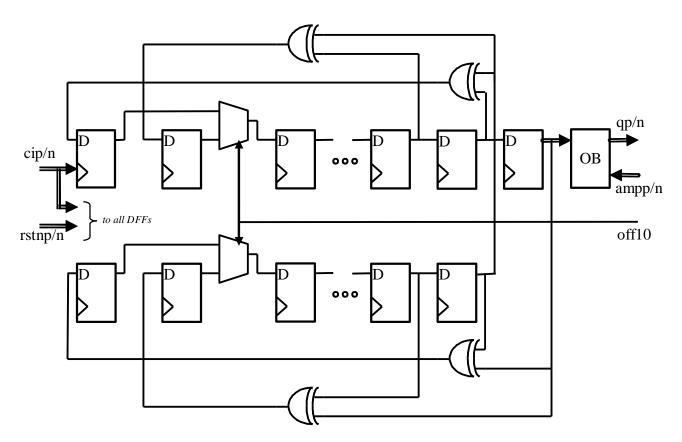


Fig. 1. Functional Block Diagram

The SiGe IC shown in Fig. 1 provides a selectable full 511-bit or 1023-bit long pseudo-random binary sequence (PRBS) signal according to either a $(x^9 + x^4 + 1)$, or a $(x^{10} + x^7 + 1)$ polynomial respectively, where x^D represents a delay of D clock cycles. This is implemented as a linear feedback shift register (LSFR) in which the outputs of either the ninth and fourth, or tenth and seventh flip-flops are combined together by an XOR function, and provided as an input to the first flip-flop of the register.

The PRBS register can be preset to All-"1" state with an asynchronous external active-low preset signal rstnp/rstnn.

The generated PRBS signals are delivered to a differential output port qp/qn through a CML output buffer (OB).

The Output Buffer provides the possibility for an output amplitude adjustment through an external low-speed differential analog port ampp/ampn. The simulated control diagram is shown in Fig 2.



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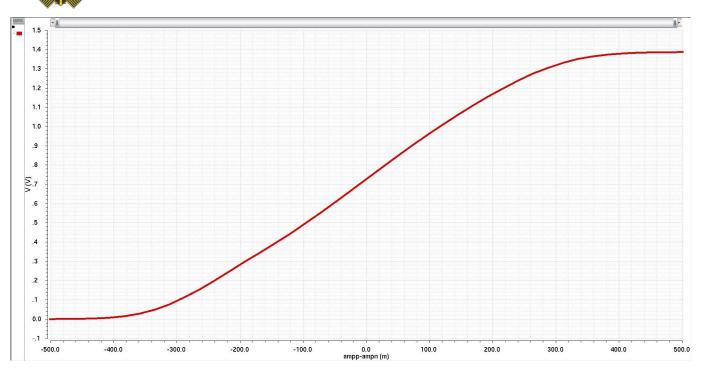


Fig. 2. Simulated Output Amplitude Control Diagram

All I/O stages are back terminated to **vcc** with on-chip 50*Ohms* resistors and may be used in either DC or AC coupling modes (see also POWER SUPPLY CONFIGURATION). In the first mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the second mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0V = ground and vee = -3.3V), or a positive supply (vcc = +3.3V and vee = 0.0V = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0V and vee = -3.3V.



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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power supply current		500	mA
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°С
Storage Temperature	-40	+100	°С
Operational Humidity	10	98	%
Storage Humidity	10	98	%

Table 1. Absolute Maximum Ratings

TERMINAL FUNCTIONS

TERMINAL		AL	DESCRIPTION		
Name	No.	Туре			
	High-Speed I/Os				
rstnp	11	CML	Differential high-speed asynchronous reset (active low) inputs		
rstnn	9	input	with internal SE 500hms termination to VCC		
cip	21	CML	Differential clock input signals with internal 500hms		
cin	23	input	termination to VCC		
qp	17	CML	Differential data outputs. Require external SE 500hms		
qn	15	output	termination to VCC		
ampp	3	CML	Differential low-speed control inputs with internal SE 2KOhms		
ampn	5	input	terminations to vcc.		
Control Signal					
off10	7	CMOS	3.3V CMOS input with internal 1 <i>MOhms</i> pull-up to vcc		
		input			

TERMINAL			DESCRIPTION		
Name	No.	Туре			
Supply and Termination Voltages					
Name	Description		Description Pin Number		
vcc	Positive power supply $(+3.3V \text{ or } 0)$			2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24	
vee	Negative power supply (0V or -3.3V)			1, 13, 19	



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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN '	TYP	MAX	UNIT	COMMENTS	
General Parameters						
vee	-3.1	-3.3	-3.5	V	±6%	
VCC		0.0		V	External ground	
Ivee	340	370	400	mА	Depending on amplitude control	
Power consumption		1220		mW		
Junction temperature	-40	25	125	°C		
		H	IS Input	Clock (cip/cin)	
Frequency	DC		32	GHz		
Swing	0.15		0.8	V	Differential or SE, p-p	
CM Voltage Level	VCC-0.8 VCC V Must match for both inputs		Must match for both inputs			
		H	IS Outpu	ıt Data (qp/qn)	
Swing (SE) pk-pk	0 1.4 V		V	Depending on amplitude control		
CM Voltage Level	vcc-Swing/2		V			
Output Jitter	2.5		ps	Peak-to-peak		
		R	eset Sign	al (rstnr	o/rstnn)	
Frequency	DC		15	GHz		
Rise time			20	%	of the clock period	
Recovery time	36		ps			
Swing	0.05 0.8		V	Differential p-p		
CM Voltage Level						
	Outpu	t Am	olitude C	ontrol p	ort (ampp/ampn)	
Bandwidth	DC		10	MHz.		
SE voltage level	vcc-400)	VCC	mV	Half control range when the opposite pin is	
					at VCC.	
SE voltage level	vcc-800)	VCC	mV	Full control range when the opposite pin is	
					at vcc-0.4V.	
Differential swing	0		800	mV	Peak-peak; full control range.	
CM Level	CM Levelvcc-(Diff. swing)/4VIn differential mode					
		PF	RBS Sele	ct Signal	l (off10)	
High voltage level	vcc-0.4		VCC	V		
Low voltage level	vee	v	ee+0.4	V	Do not apply voltages below vee!	

PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFN package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section be soldered to the **vcc** plain, which is ground for a negative supply, or power for a positive supply.



TOP

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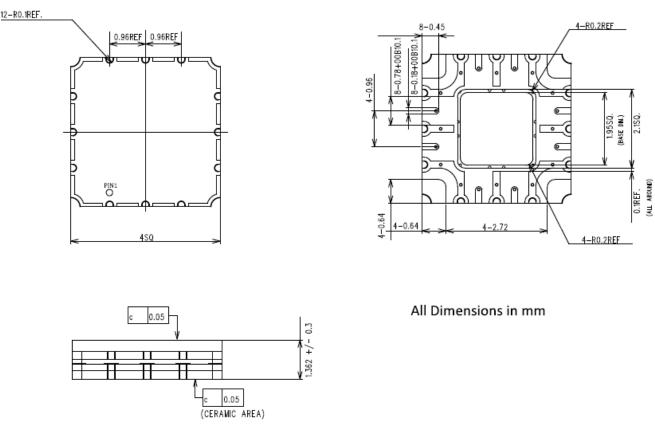


Fig. 3. CQFN 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT8146-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.0.2	10-2024	First release
0.0.3	04-2023	Preliminary release
0.0.2	03-2023	Preliminary release