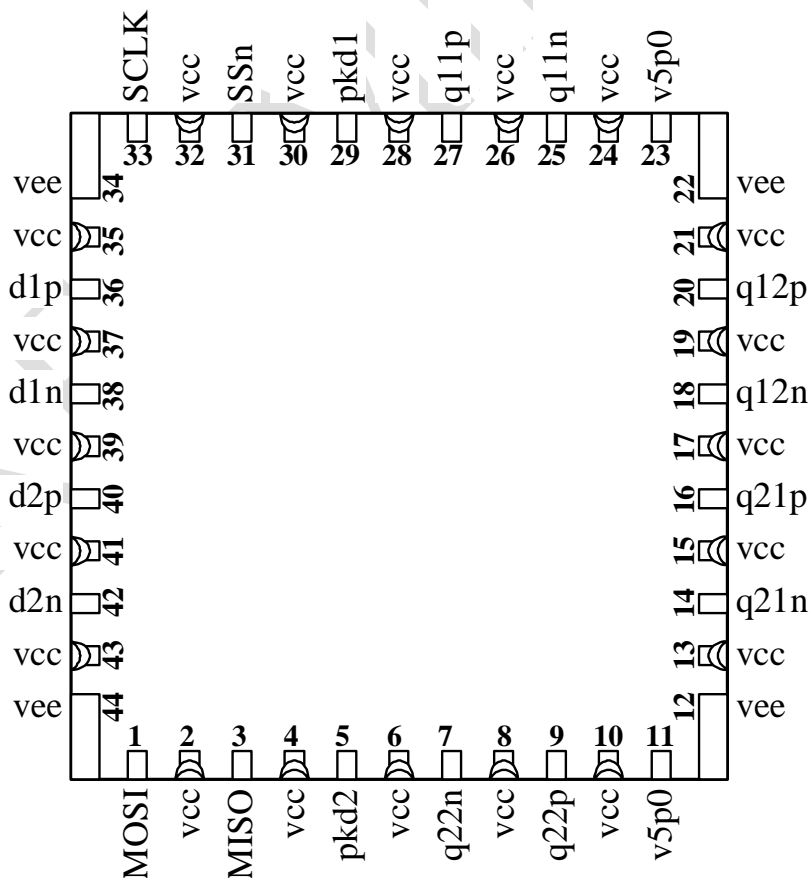


## ASNT6155-KHS

### Dual 2-Channel CTLE with Peak Detectors

- High-speed adjustable linear equalizer
- Two independent data channels with two independent equalization paths per channel
- Independently adjustable 3 zeros and 2 poles in each path AC response
- Independent gain adjustment in each equalization path
- High-speed CMOS 3-wire interface for chip control
- Input peak detectors in both channels
- Fully differential CML-type analog input and output interfaces
- Two power supplies for the data paths and AC control circuitry
- Average power consumption: 1.5W
- Fabricated in SiGe for high performance, yield, and reliability
- Limited temperature variation over industrial temperature range
- Die size 1.5x1.5mm<sup>2</sup>
- Custom QFN 44-pin package



## DESCRIPTION

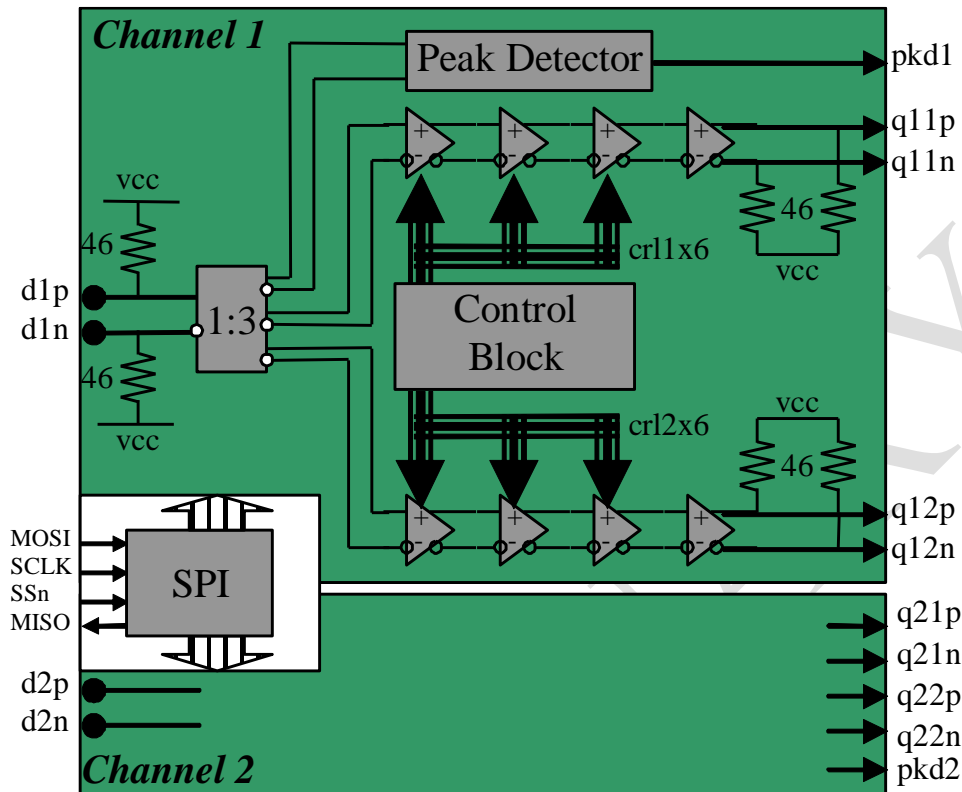


Fig. 1. Functional Block Diagram

The IC shown in Fig. 1 is a four-path adjustable continuous-time linear equalizer (CTLE) with two independently controlled analog data equalization channels combined in two groups. Each equalization channel has its own output. The AC response of each path has 8 controls: adjustable DC gain, adjustable linearity, 3 independently adjustable zeros, 2 independently adjustable poles, and additional high-frequency bandwidth control.

Input Peak Detectors that represent the input signal amplitude are added to each channel.

The part's I/Os support CML-type differential interface with on-chip 46 Ohms termination to VCC. Matching external terminations are also required.

All operational modes of the chip are controlled by a Control Block that communicates with an external computer through a high-speed 3-wire serial interface. The channel groups are named Group A and Group B in the corresponding graphical user interface (GUI).

The part operates with a positive supply  $V_{CC} = +3.3V$  for the main data paths, and an additional positive supply  $V_{5p0} = +5.0V$  for the AC control circuitry. The negative supply rail  $V_{EE}$  should be connected to external ground as shown in Fig. 2a.

The part can also operate with a negative supply  $V_{EE} = -3.3V$  for the main data paths, and an additional positive supply  $V_{5p0} = +1.7V$  for the AC control circuitry. In this case the positive

supply rail VCC should be connected to external ground as shown in Fig. 2b. Also, the SPI input and output signals should be connected through DC blocks, or optocouplers.

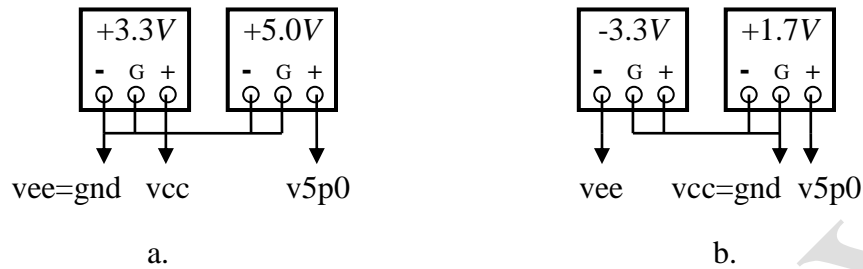


Fig. 2. Power Supply Configurations: Positive (a) and Negative (b)

### Equalization Path

Typical AC responses of an Equalization Path are shown in Fig. 3.

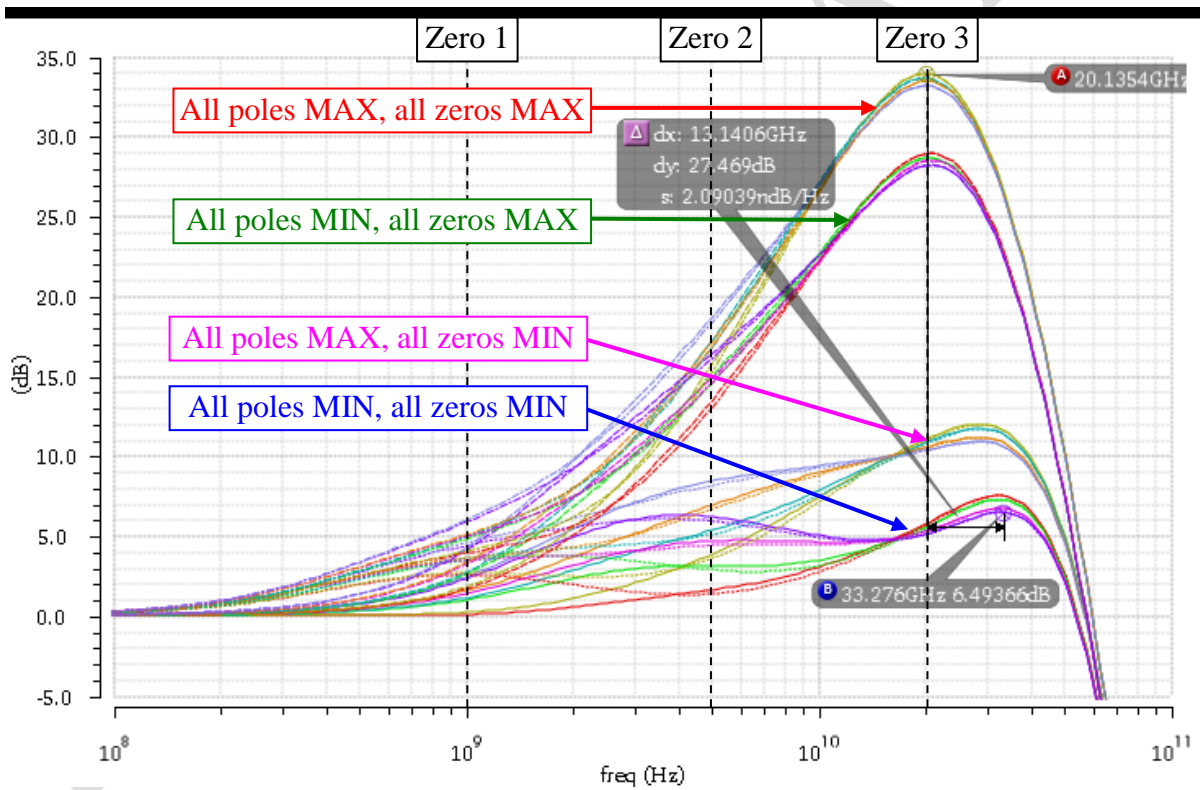


Fig. 3. Typical AC responses of an Equalization Path

Each path has 3 independent adjustable Zeros, and two independent adjustable Poles. For each setting, the DC gain can be adjusted between -3dB and +5dB.

Additionally, the path's bandwidth (BW) can be also adjusted using EF controls as shown by the red and magenta curves in Fig. 4 that are plotted for the Min Pole, and Min Zero setting.

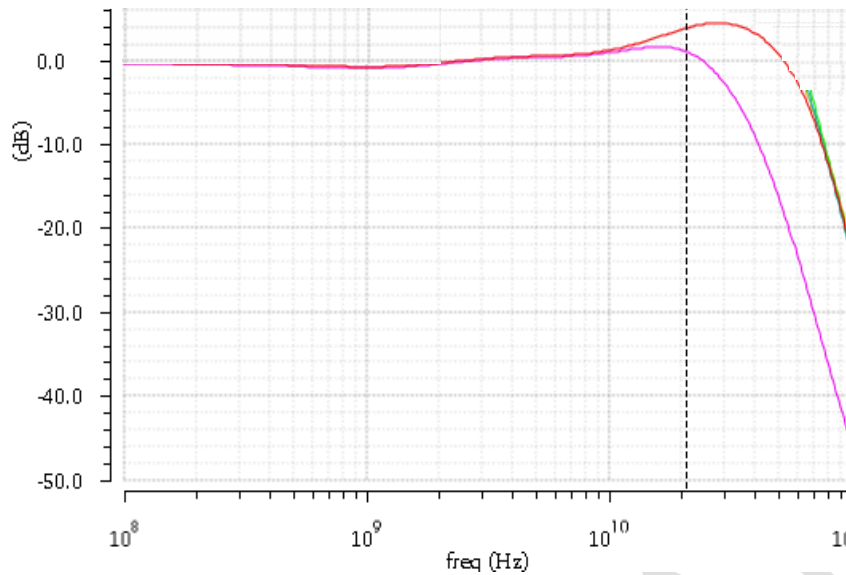


Fig. 4. BW Control Characteristics

If required, a channel’s linearity can be adjusted using lbuf controls. The higher values of the code correspond to higher linearity and higher power consumption of the chip. They also increase the channel’s gain for any gain settings other than maximum.

Corresponding controls are detailed in Table 1. Increase of any control results in gain increase within a certain frequency range around the specified frequency as shown in the corresponding drawings.

Table 1. Data Channel Controls

Control function	Frequency, GHz	SPI name	GUI Slider name	Corresponding drawing
Low-frequency zero	1	zcl_X	Zero at f / Lo	Fig. 3
Mid-frequency zero	5	zcm_X	Zero at f / M	Fig. 3
High-frequency zero	16	zch_X	Zero at f / Hi	Fig. 3
First pole	2	pc1_X	Pole / 1	Fig. 3
Second pole	16	pc2_X	Pole / 2	Fig. 3
Gain	DC	gc_X	Gain	
Output EF	>20	efcX	Out BW	Fig. 4
Input EF	>20	efc12	Input BW	Fig. 4
Ibuf	DC	bufc_Y	Linearity	

Here X is the channel (or output) number that equals to 1 or 2 and Y is the Group number that equals A or B. In the GUI, X=1 corresponds to Channel1 in Group A, or Channel 3 in Group B, and X=2 corresponds to Channel2 in Group A, or Channel 4 in Group B.

### Peak Detector

The Peak Detector block represents the single-ended swing of its input signal as an output voltage between 1.65V to 2.85V. The typical characteristics for a 1GHz sinusoidal input signal at different PT operational conditions are shown in Fig. 5.

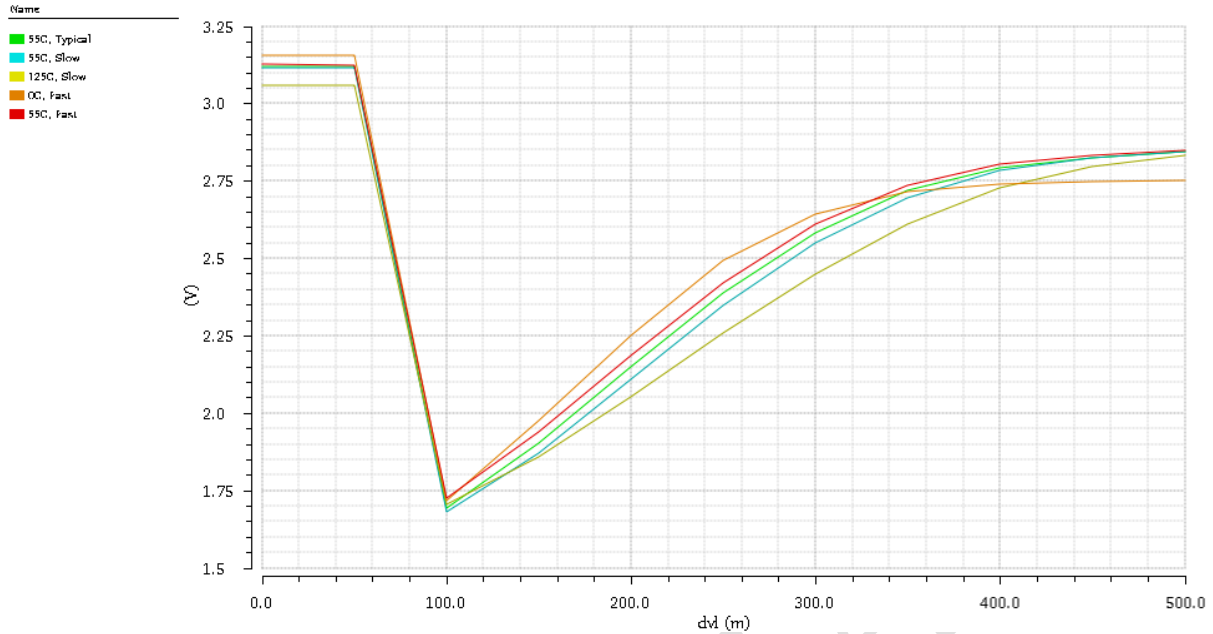


Fig. 5. Peak Detector Typical Simulated Characteristics for Different  $T^\circ$  and Process Corners

As can be seen in the plot, the signal swings below a certain value are represented by the high voltage above 3.0V. This function can be used as an indication of NO Input Signal (Loss-of-signal, or LOS). The LOS threshold can be adjusted through SPI as shown in Fig. 6.

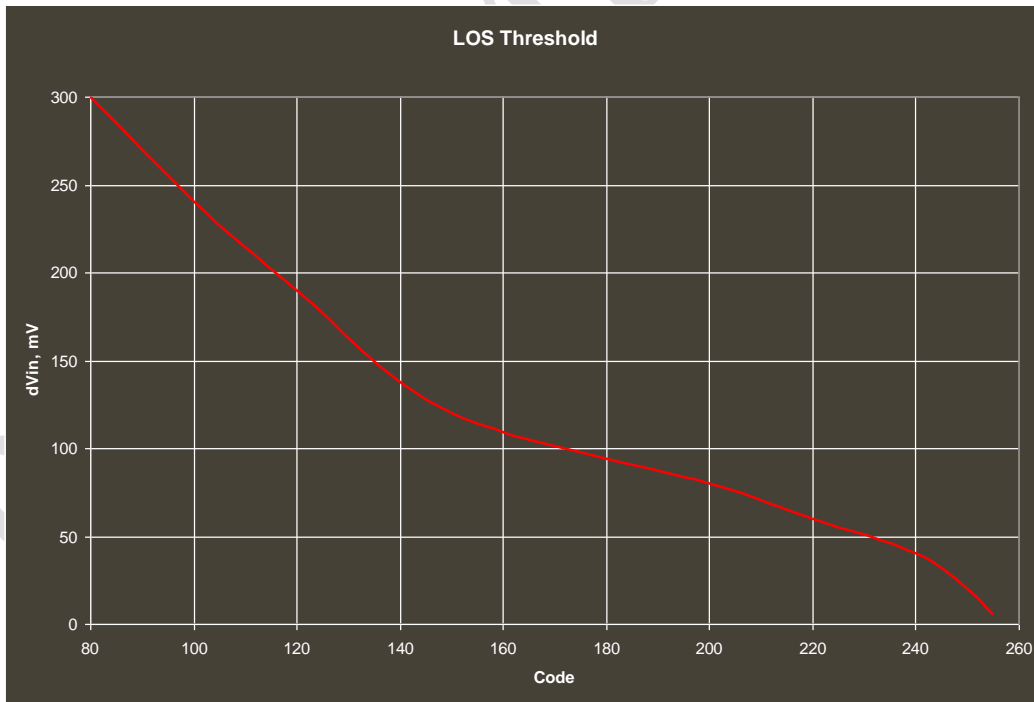


Fig. 6. LOS Threshold Adjustment

The Peak Detector features a short settling time as shown in Fig. 7 that shows the sinusoidal input signal, and the Peak Detector output at different operational conditions.

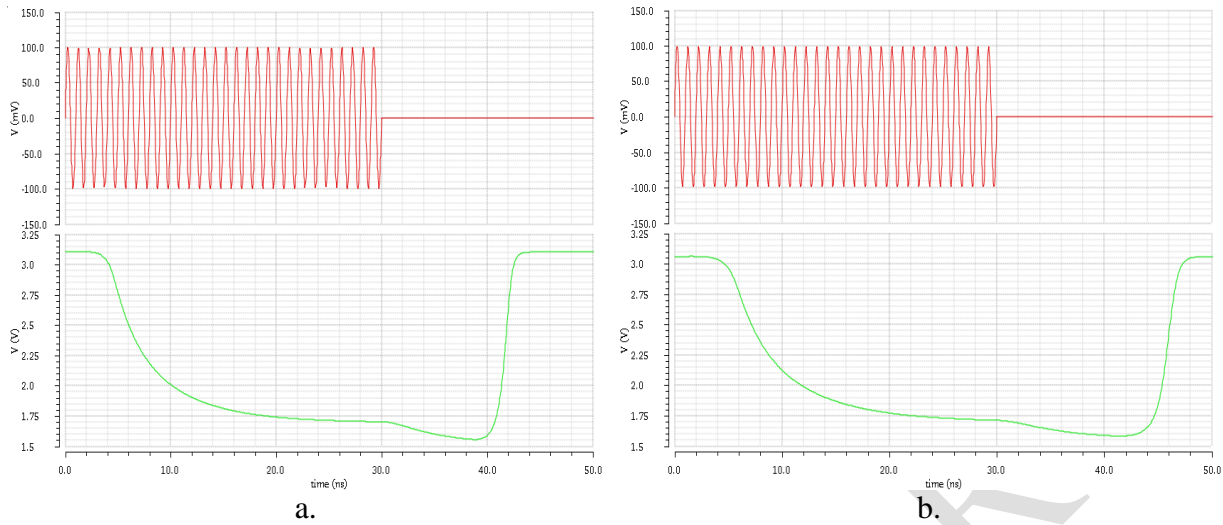


Fig. 7. Peak Detector settling Time (a – Nominal, b – Worst Case Slow)

### 3-Wire Interface

All functions of the chip are controlled through a 3-wire SPI. The interface includes a 17-byte internal register and operates with 3.3V CMOS signals. It provides control signals for any of 2 groups of channels: Group A (Channels 1 and 2), and Group B (Channels 3 and 4). Each group data can be loaded independently, and the active group is selected by bit1 of byte17 in each data packet. The bit map of the interface is shown in Table 2, and its timing diagram in Fig. 8.

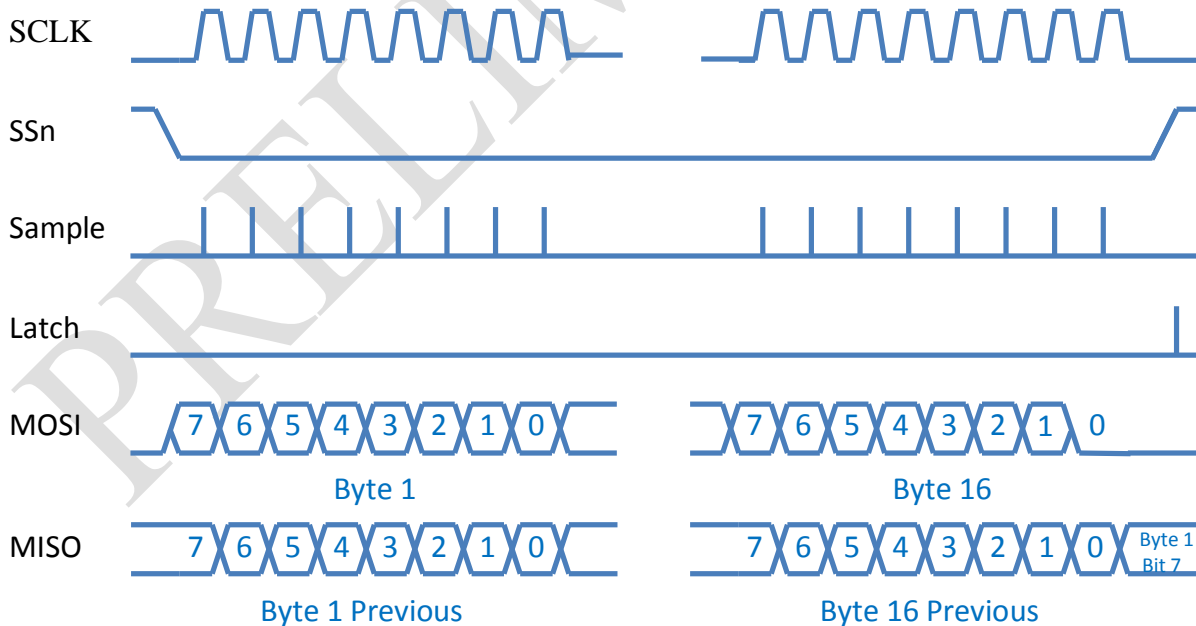


Fig. 8. SPI Timing Diagram





Table 2. 3-Wire Interface Bit Map

Byte #	Bit #	Bit order	Signal name	Default Value	Signal function
1	From 7	MSB	zcl_1	10000000	Low-frequency zero control for the first output of the selected Group
	to 0	LSB			
2	From 7	MSB	zcm_1	10000000	Middle-frequency zero control for the first output of the selected Group
	to 0	LSB			
3	From 7	MSB	zch_1	01000000	High-frequency zero control for the first output of the selected Group
	to 0	LSB			
4	From 7	MSB	gc_1	10000000	Gain control for the first output of the selected Group
	to 0	LSB			
5	From 7	MSB	pc1_1	10000000	First pole control for the first output of the selected Group
	to 0	LSB			
6	From 7	MSB	pc2_1	10000000	Second pole control for the first output of the selected Group
	to 0	LSB			
7	From 7	MSB	efc1	10000000	BW control for the first output of the selected Group
	to 0	LSB			
8	From 7	MSB	zcl_2	10000000	Low-frequency zero control for the second output of the selected Group
	to 0	LSB			
9	From 7	MSB	bufc	10010010	Linearity control for both channels of a Group through stages current adjustment
	to 0	LSB			
10	From 7	MSB	zcm_2	10000000	Middle-frequency zero control for the second output of the selected Group
	to 0	LSB			
11	From 7	MSB	zch_2	01000000	High-frequency zero control for the second output of the selected Group
	to 0	LSB			
12	From 7	MSB	gc_2	10000000	Gain control for the second output of the selected Group
	to 0	LSB			
13	From 7	MSB	pc1_2	10000000	First pole control for the second output of the selected Group
	to 0	LSB			
14	From 7	MSB	pc2_2	10000000	Second pole control for the second output of the selected Group
	to 0	LSB			
15	From 7	MSB	efc2	10000000	BW control for the second output of the selected Group
	to 0	LSB			
16	From 7	MSB	losth1	10000000	LOL threshold control for the selected Group
	to 0	LSB			
17	From 7	MSB	efc12	100000	Additional BW control for both outputs of the selected Group
	to 2	LSB			
	1		wraddr	0	“0”– write to Group A, “1”– write to Group B
0		-	0	Constant “0”	

The initial registers of the SPI are preset to the above default states at the time of the chip power supply activation.

## TERMINAL FUNCTIONS

TERMINAL			Description
Name	No.	Type	
<b>High-Speed I/Os</b>			
d1p	36	CML-type Analog Inputs	Differential high-speed channel 1 data inputs with internal SE 46Ohm termination to VCC
d1n	38		
d2p	40		
d2n	42		
q11p	27	CML-type Analog Outputs	Differential high-speed channel 1 path 1 data outputs with internal SE 46Ohm termination to VCC
q11n	25		
q12p	20		
q12n	18		
q21p	16		
q21n	14		
q22p	9		
q22n	7		
<b>Low-Speed I/Os</b>			
SSn	31	3.3V CMOS I/Os	3-wire interface enable input with internal 474KOhm pull-up to VCC
SCLK	33		3-wire interface clock input with internal 474KOhm pull-down to VEE
MOSI	1		3-wire interface data input with internal 474KOhm pull-down to VEE
MISO	3		3-wire interface data output
pkd1	29	CMOS Output	Error Detector output and below-threshold signal amplitude indicator, with internal 6KOhm SE termination to VCC
pkd2	5		

Supply And Termination Voltages		
Name	Description	Pin Number
v5p0	+5.0V positive power supply Negative pin to VEE	11, 23
vee	Ground	12, 22, 34, 44
vcc	+3.3V positive power supply Negative pin to VEE	2, 4, 6, 8, 10, 13, 15, 17, 19, 21, 24, 26, 28, 30, 32, 35, 37, 39, 41, 43

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed VEE).



Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Main Supply Voltage (vcc)		3.6	V
Additional Supply Voltage (v5p0)		5.5	V
RF Input Voltage Swing (SE)		750	mV
Case Temperature		+85	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee		0.0		V	External ground
vcc	3.1	3.3	3.5	V	vcc in relation to vee
v5p0	4.8	5.0	5.3	V	v5p0 in relation to vee
$I_{v5p0}$ per eq. channel	3.5		28	mA	Depending on the state of SPI control bytes
$I_{vcc}$	120		600	mA	
Power Consumption	0.45	1.5	2.6	W	
vcc ramp length			10	ms	For reliable SPI preset
Junction temperature	0	50	125	°C	
<b>Data input (d1p/d1n, d2p/d2n)</b>					
Data Rate	DC		32	Gb/s	
SE Swing (1GHz differential signal)	200		440	mV	0.3% THD, Min/Max bufc
	330		530	mV	0.9% THD, Min/Max bufc
CM Level	vcc-Swing/2				for DC input termination
<b>Data output (q11p/q11n, q12p/q12n, q21p/q21n, q22p/q22n)</b>					
Max peaking frequency	20		33	GHz	
Gain from Input	-3		+5	dB	Depending on SPI settings
CM Level	vcc-0.35			V	for DC output termination
<b>Peak Detector output (pkd1, pkd2)</b>					
Voltage range	1.6		2.8	V	For input swing control
	3.05		3.25	V	For LOS operation
Settling time	15		20	ns	
<b>3-Wire Interface</b>					
Clock frequency	0.1		50	MHz	
Input low logic level	vee		vee+0.4	V	
Input high logic level	vcc-1.3		vcc	V	
Output low logic level	vee		vee+0.2	V	
Output high logic level	vcc-0.3		vcc	V	
Input current			9	uA	For each input

## PACKAGE INFORMATION

The die is housed in a custom, 44-pin CQFN package shown in Fig. 9. The package provides a center heat slug located on the back side of the package to be used for heat dissipation. ADSANTEC recommends using extreme caution when soldering this section to the board to avoid overheating. It should be connected to the VCC plain that is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6155-KHS. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

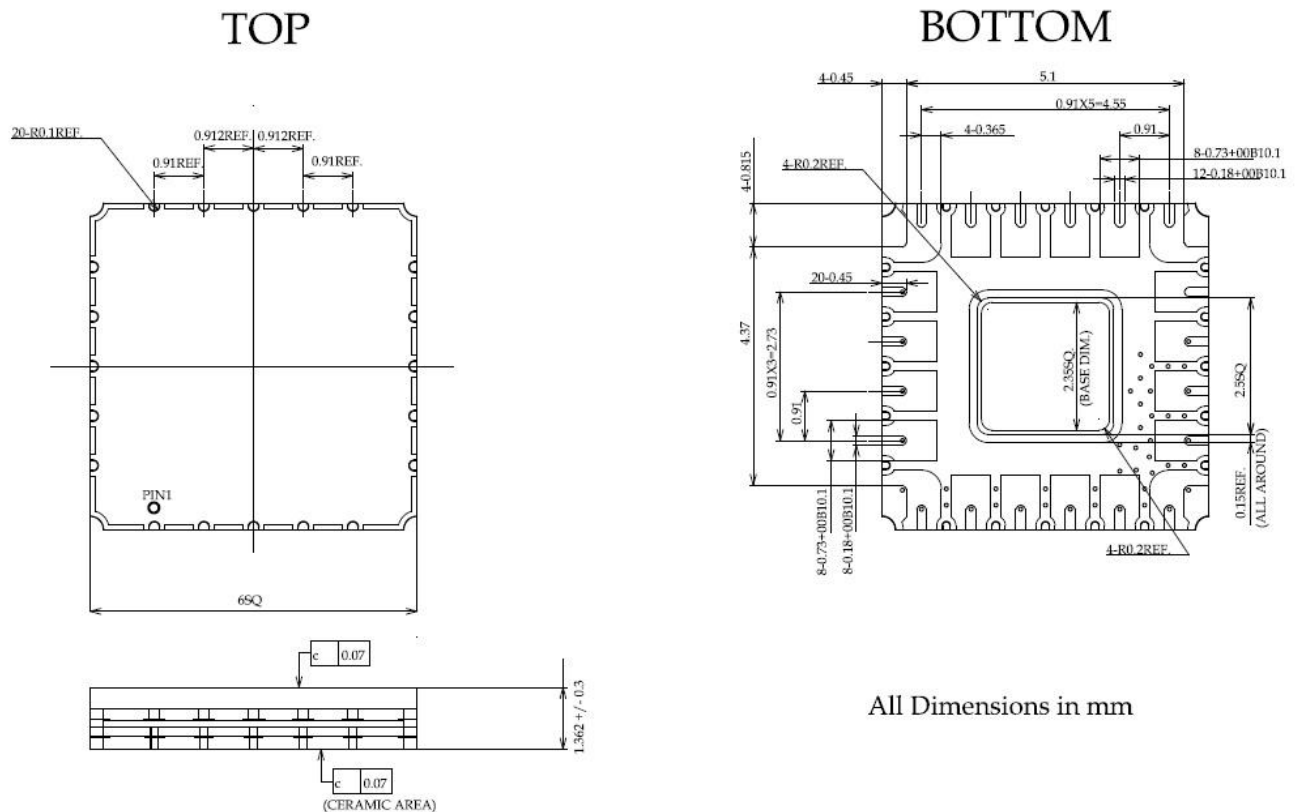


Fig. 9. CQFN44 Package Drawing (All Dimensions in mm)



## REVISION HISTORY

Revision	Date	Changes
0.4.2	04-2023	Updated Package Drawing
0.3.2	04-2023	Updated Package Drawing
0.2.2	04-2023	Corrected Pole 1 frequency Corrected v5p0 current consumption specification Corrected power consumption value
0.1.2	02-2023	Preliminary release