ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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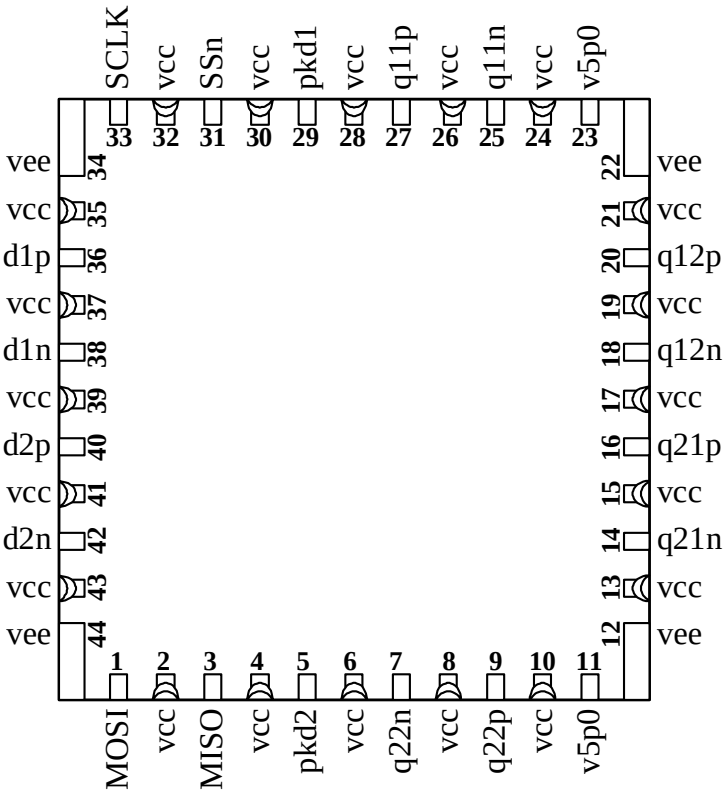
ASNT6154-KHS

Dual 2-Channel CTLE with Peak Detectors & Selectable Input Termination

- High-speed adjustable linear equalizer
- Two independent data channels with two independent equalization paths per channel
- Independently adjustable 3 zeros and 2 poles in each path AC response
- Independent gain adjustment in each equalization path
- High-speed CMOS 3-wire interface for chip control
- Input peak detectors in both channels
- Fully differential CML-type analog input and output interfaces
- Selectable Normal/High input termination in both channels
- Two power supplies for the data paths and AC control circuitry
- Average power consumption: 1.4*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Limited temperature variation over industrial temperature range
- Die size 1.5x1.5mm^2
- Custom CQFN 44-pin package



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DESCRIPTION

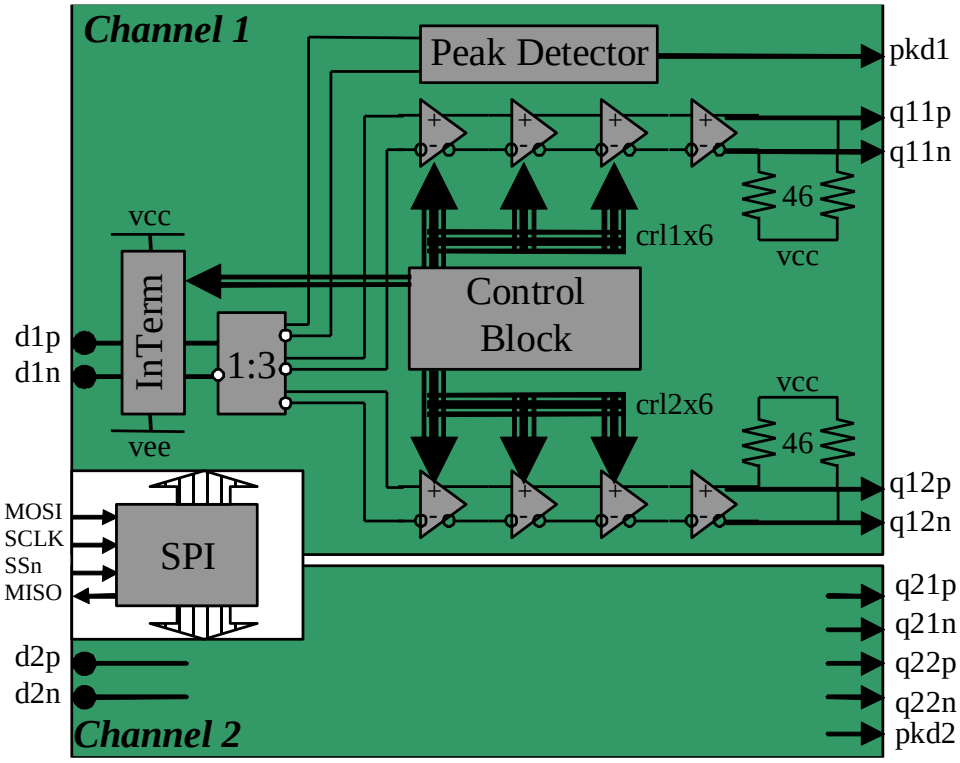

Fig. 1. Functional Block Diagram

The IC shown in Fig. 1 is a four-path adjustable continuous-time linear equalizer (CTLE) with two independently controlled analog data equalization channels combined in two groups. Each equalization channel has its own output. The AC response of each path has 8 controls: adjustable DC gain, adjustable linearity, 3 independently adjustable zeros, 2 independently adjustable poles, and additional high-frequency bandwidth control. Input Peak Detectors that represent the input signal amplitude are added to each channel.

The part's I/Os support CML-type differential interface with on-chip 46*Ohms* termination to vcc. Matching external terminations are also required. The input terminations can be switched between normal resistance of 46*Ohms* and high resistance. For the normal resistance, there are two selectable common mode voltage levels: equal to vcc and below vcc, as shown in Table 1.

Table 1. Input Termination Control

offtrmp, *code*	ontrmnn, *code*	Internal V_{CM}, *V*	Termination, *Ohms*
0	0	vcc	46
0	1	vcc-0.3	46
1	0	from vcc-1.3 to vcc-0.3	25*K*
1	1	Forbidden state	

All operational modes of the chip are controlled by a Control Block that communicates with an external computer through a high-speed 3-wire serial interface. The channel groups are named Group A and Group B in the corresponding graphical user interface (GUI).

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The part operates with a positive supply vcc = +3.3*V* for the main data paths, and an additional positive supply v5p0 = +5.0*V* for the AC control circuitry. The negative supply rail vee should be connected to external ground as shown in Fig. 2a.

The part can also operate with a negative supply vee = -3.3*V* for the main data paths, and an additional positive supply v5p0 = +1.7*V* for the AC control circuitry. In this case the positive supply rail vcc should be connected to external ground as shown in Fig. 2b. Also, the SPI input and output signals should be connected through DC blocks, or optocouplers.

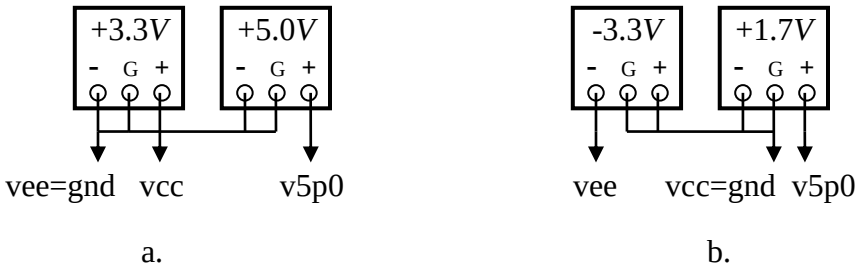

Fig. 2. Power Supply Configurations: Positive (a) and Negative (b)

Equalization Path

Typical AC responses of an Equalization Path measured on a test PCB are shown in Fig. 3.

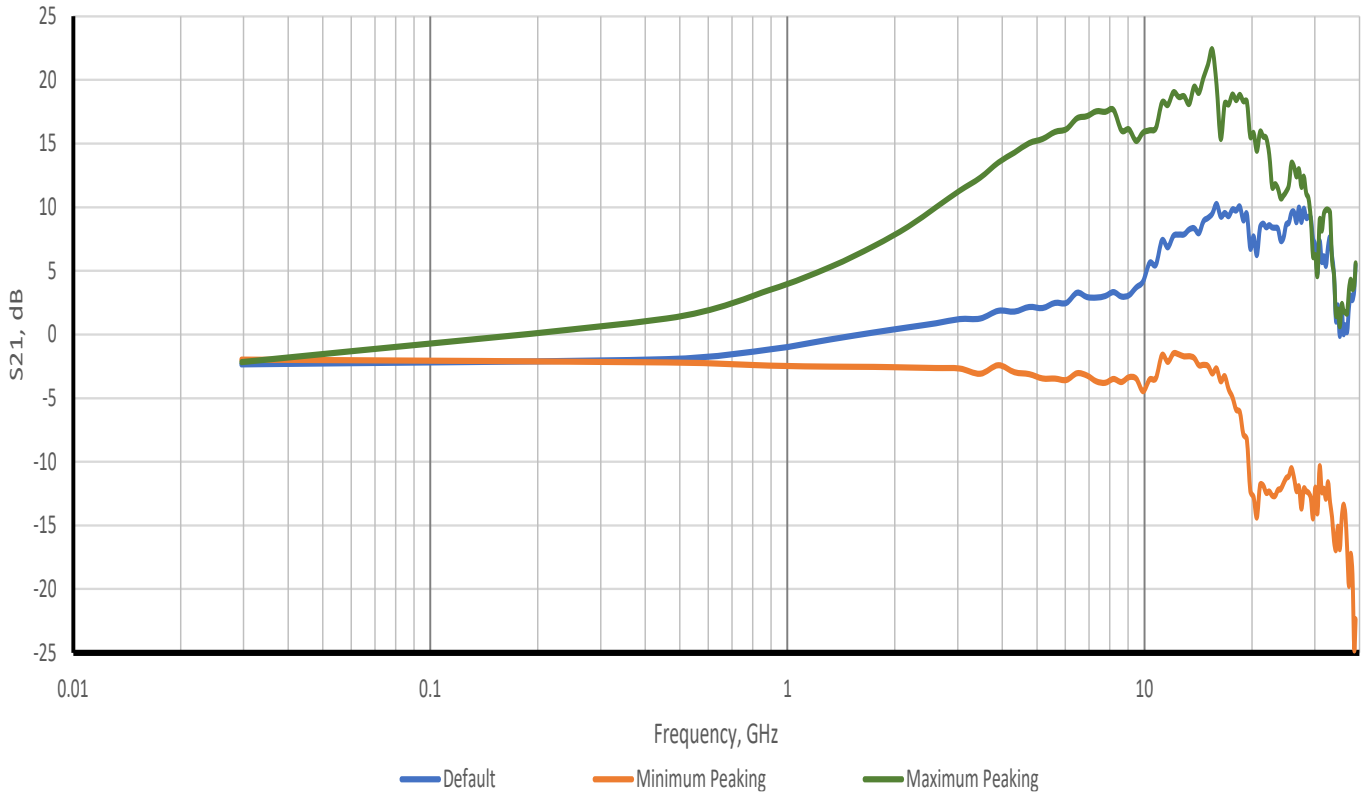

Fig. 3. Minimum, Default, and Maximum Peaking AC responses of an Equalization Path

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Each path has 3 independent adjustable Zeros, and two independent adjustable Poles. For each setting, the DC gain can be adjusted between -6dB and +14dB. Default states of the GUI section for Channel 1 (Group A) are shown in Fig. 4.

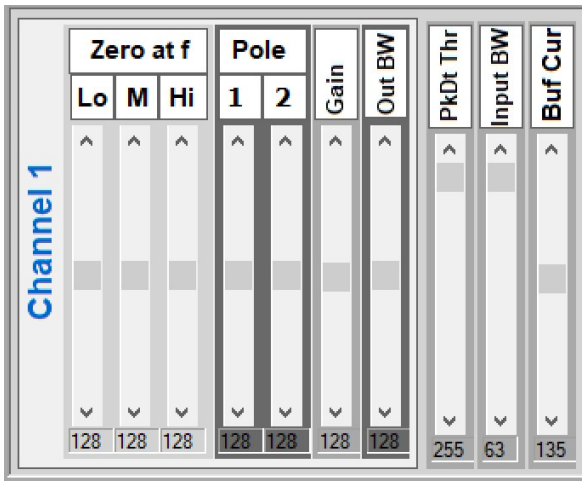

Fig. 4. Default GUI Settings for Channel 1, Group A

The following screenshots (Fig. 5 through Fig. 13) demonstrate the frequency response adjustment ranges for individual controls with all other controls at their default states.

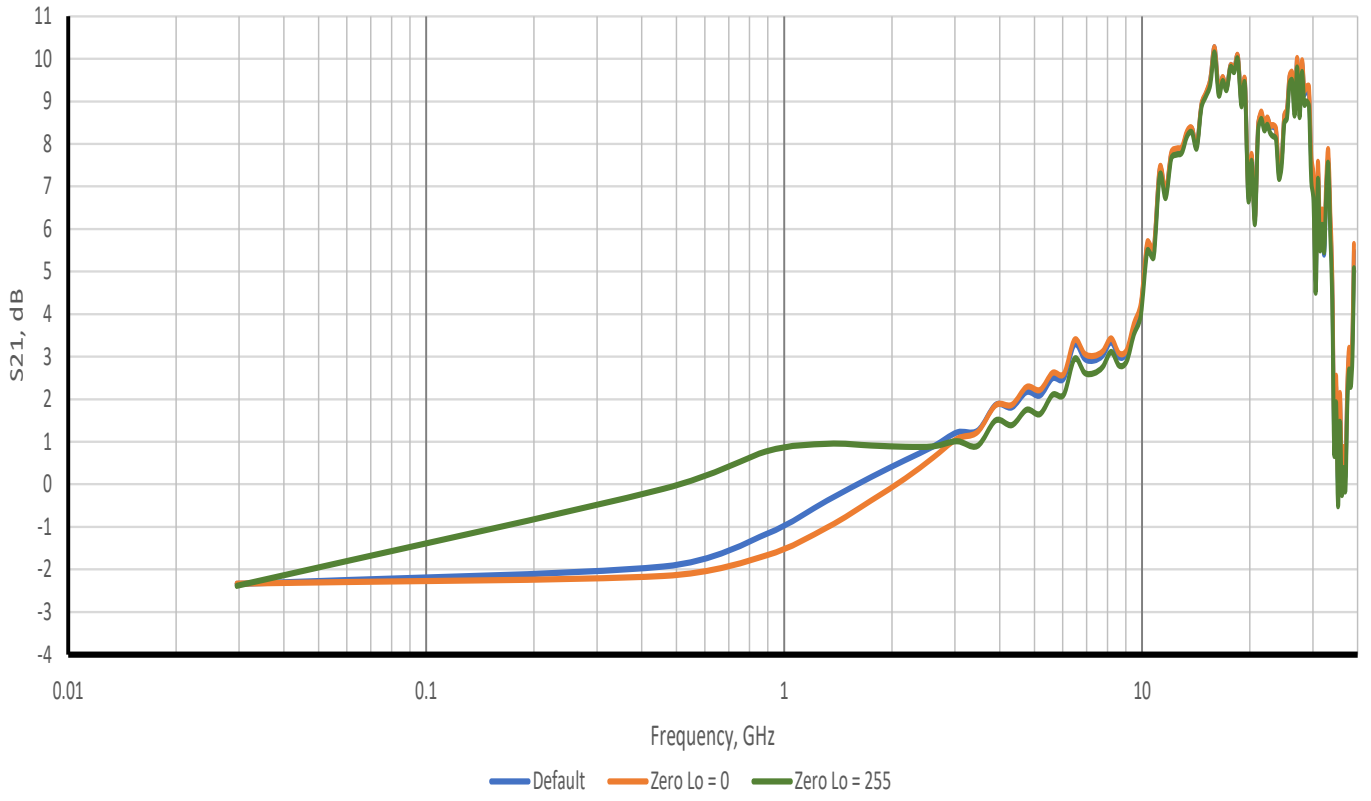

Fig. 5. Low-Frequency Zero (Zero Lo) Adjustment Effect

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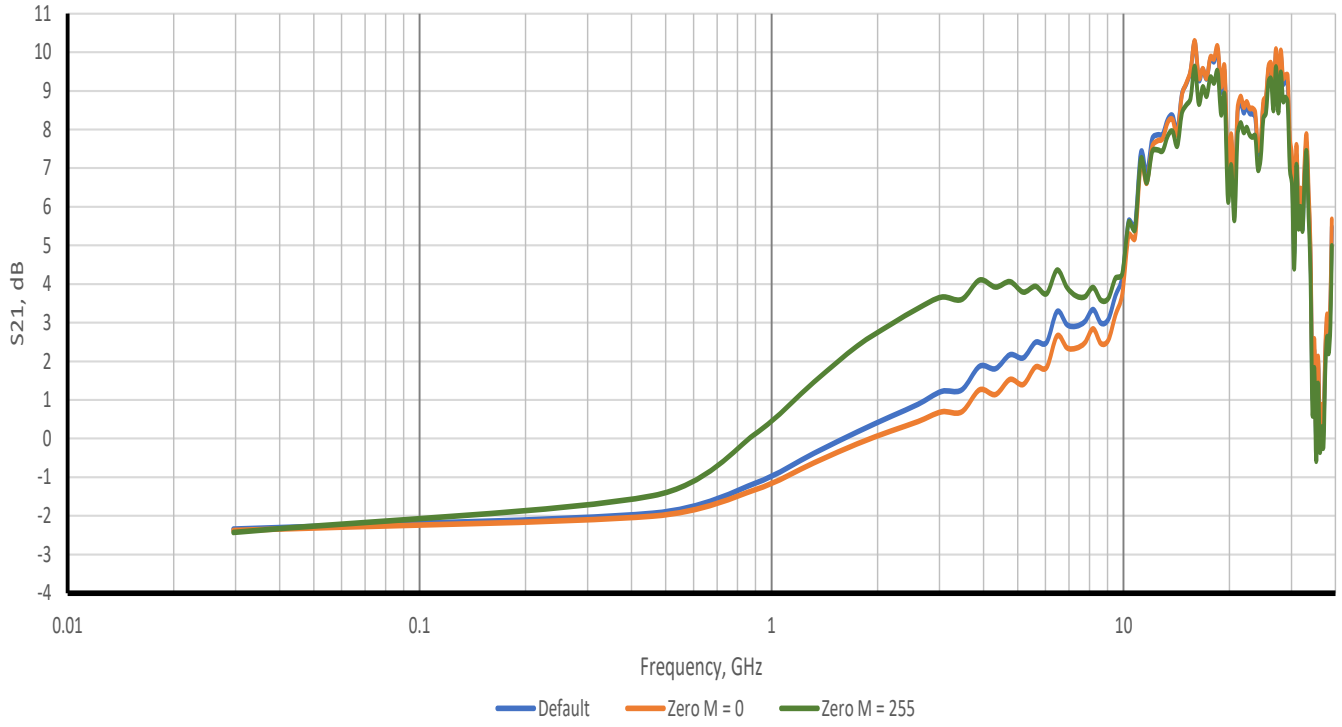

Fig. 6. Mid-Frequency Zero (Zero M) Adjustment Effect

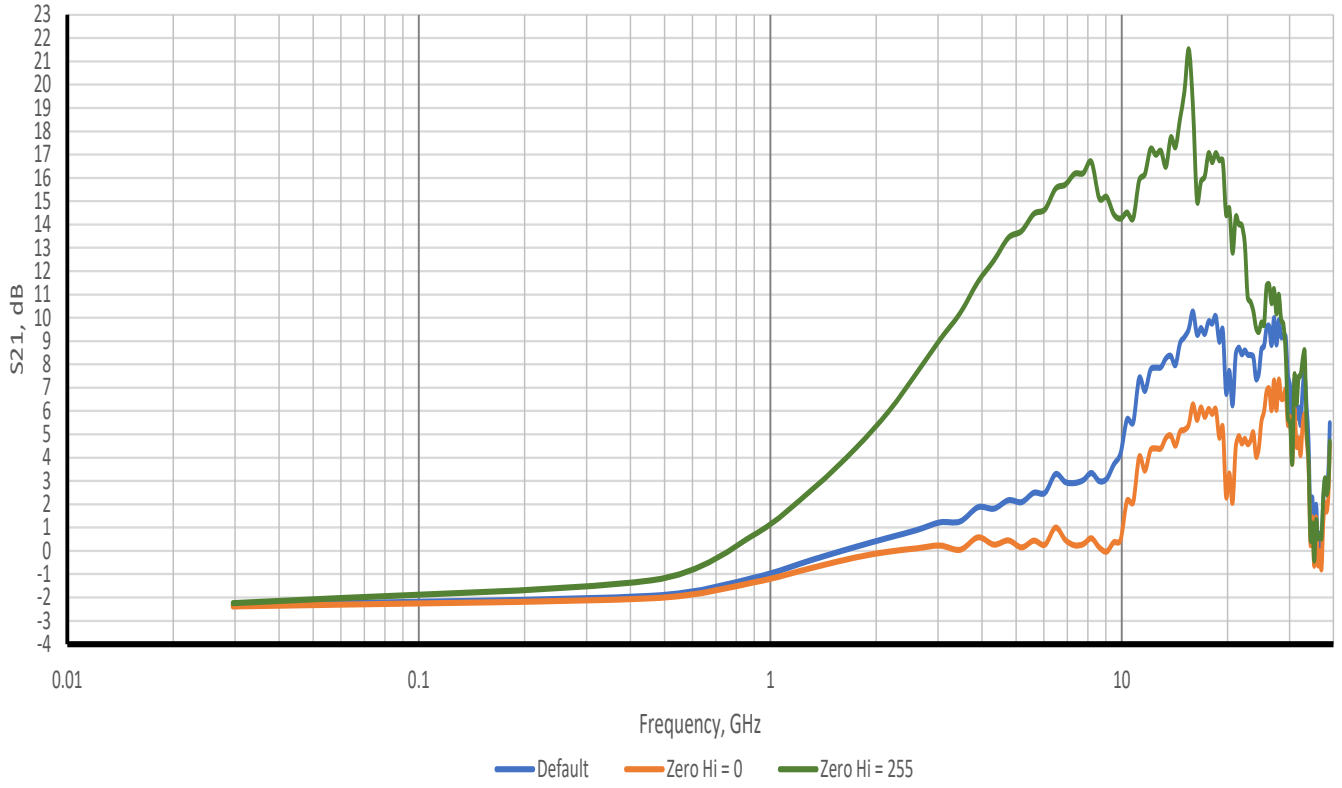

Fig. 7. High-Frequency Zero (Zero Hi) Adjustment Effect

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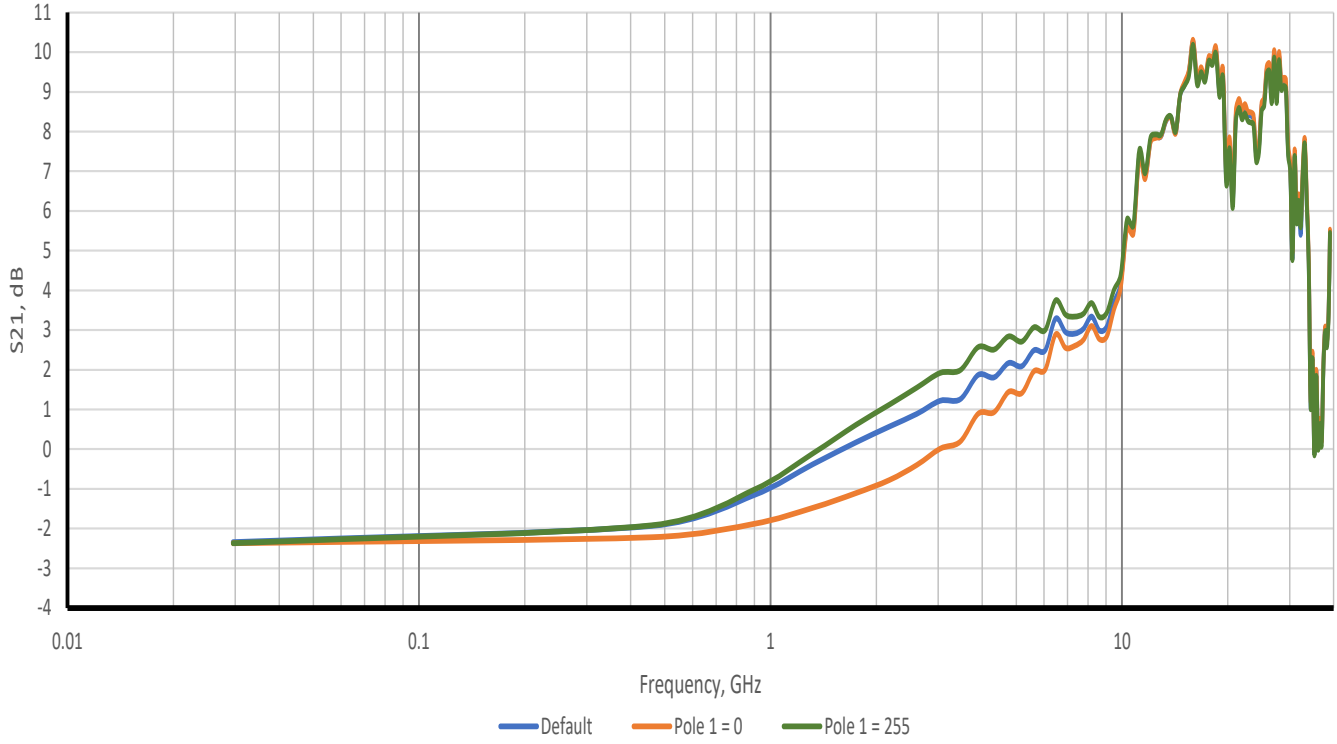

Fig. 8. Low-Frequency Pole (Pole 1) Adjustment Effect

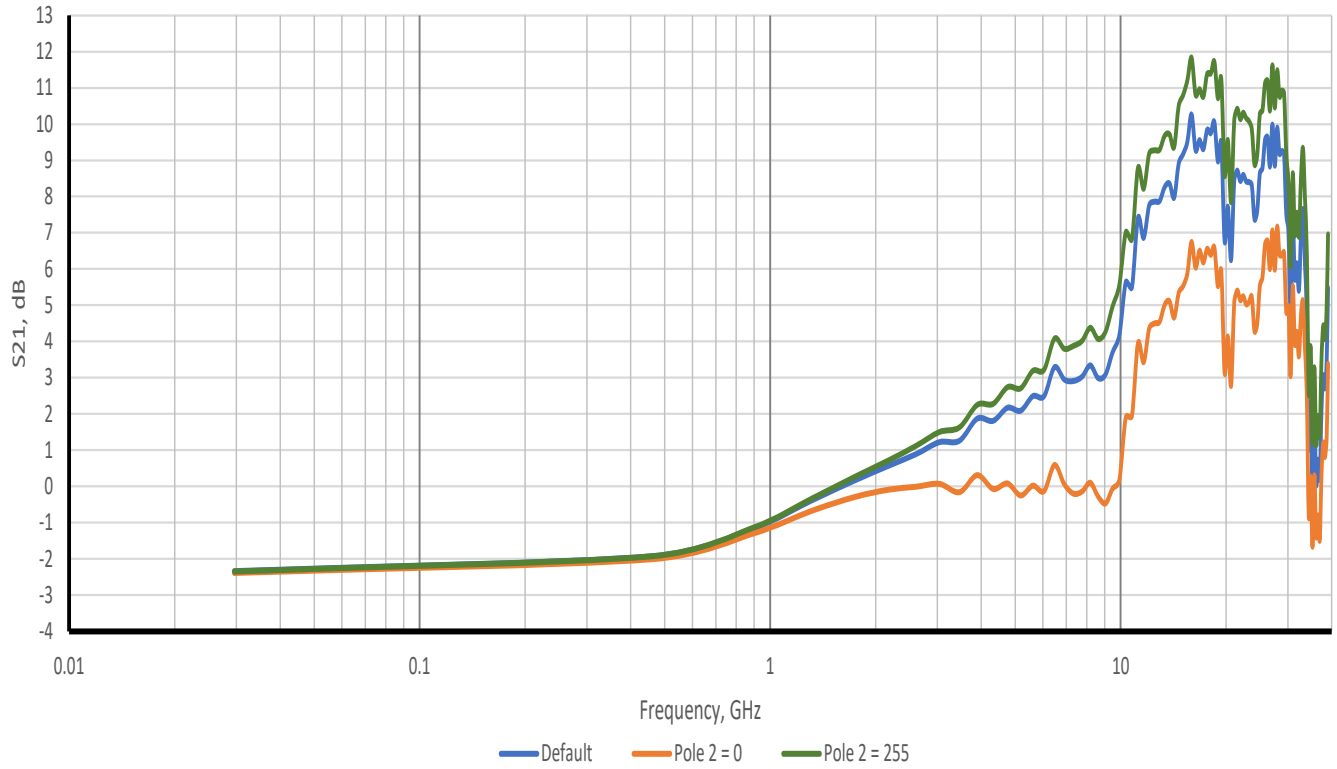

Fig. 9. High-Frequency Pole (Pole 2) Adjustment Effect

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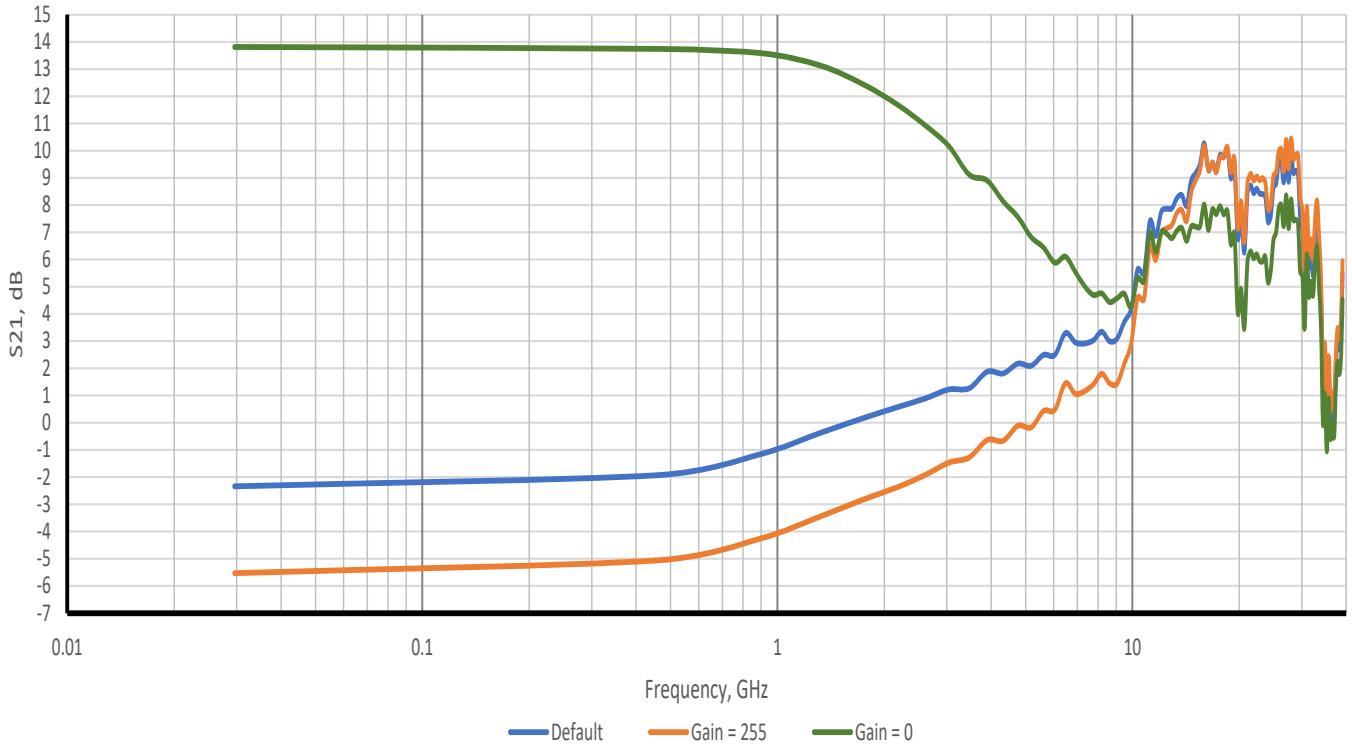

Fig. 10. Gain Adjustment Effect

Additionally, the path's bandwidth (BW) can also be adjusted using EF controls as shown below.

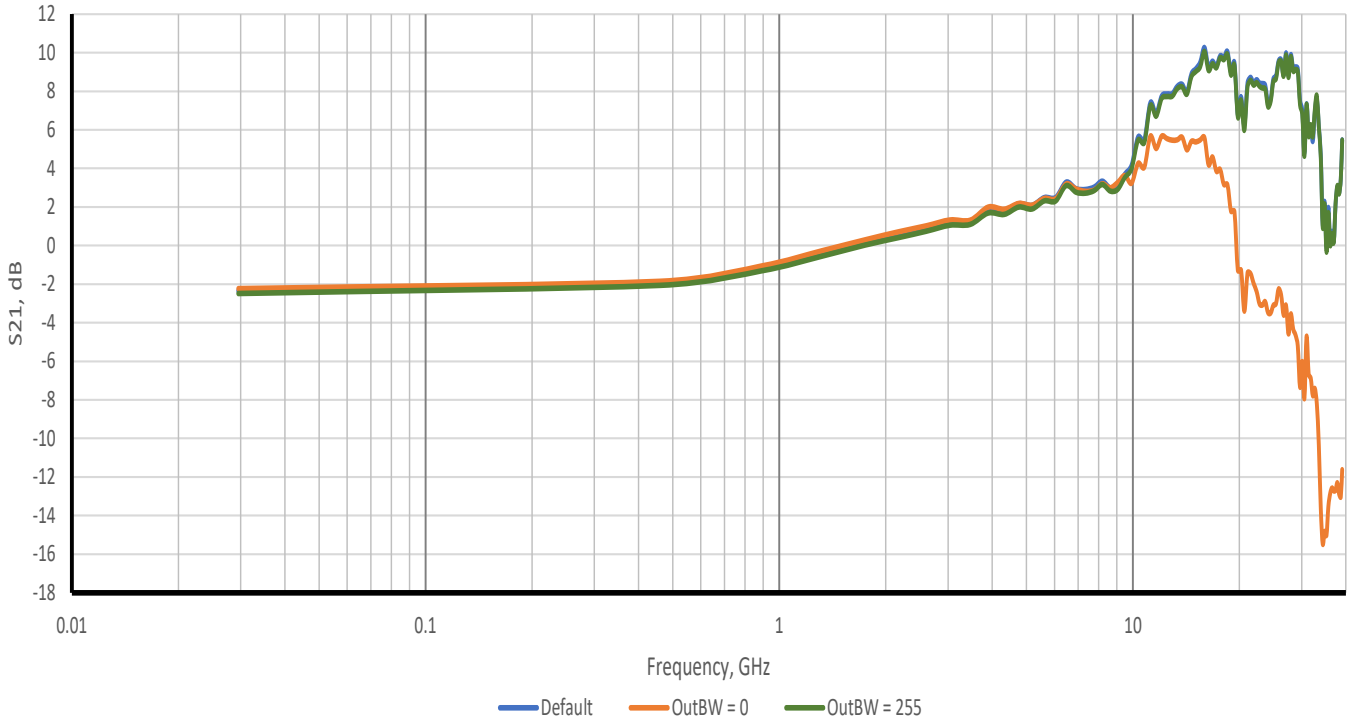

Fig. 11. Output BW Adjustment Effect

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Fig. 12. Input BW Adjustment Effect

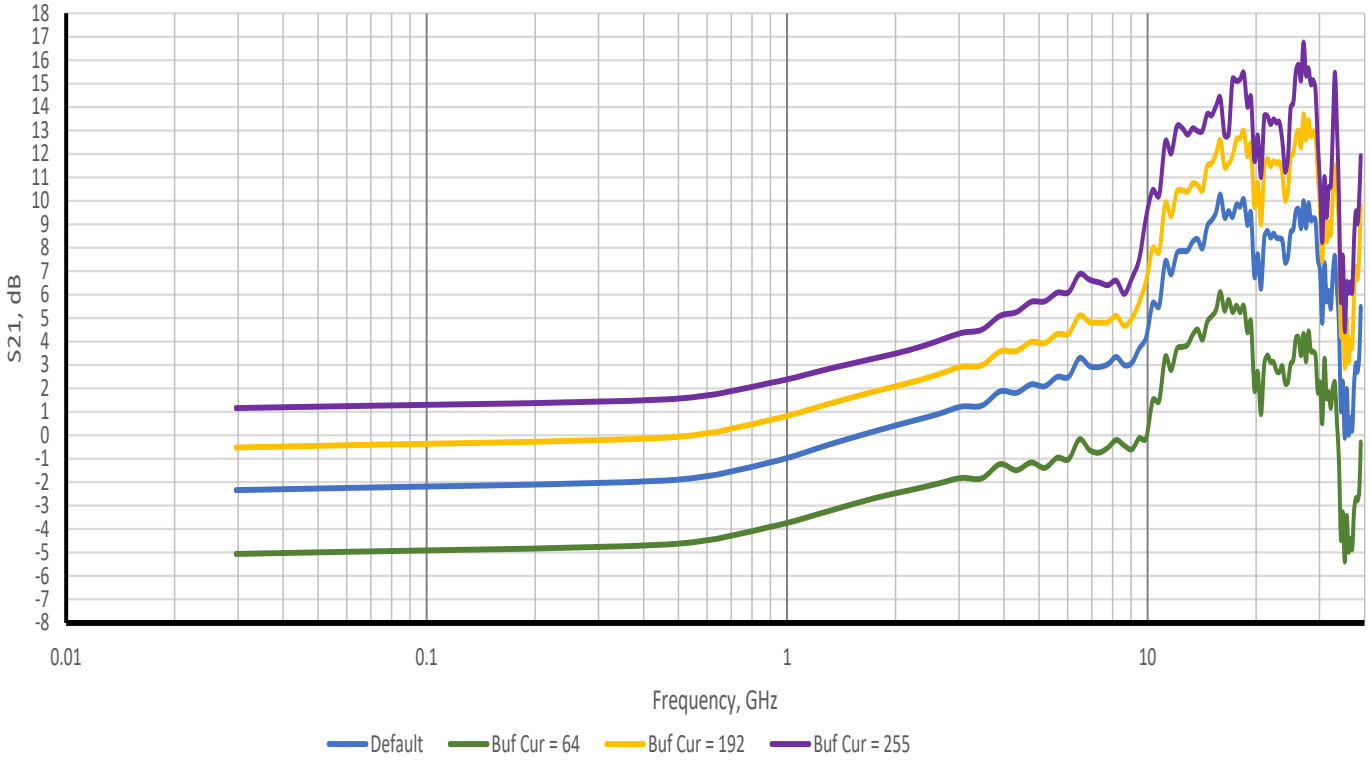

Fig. 13. Buffer Current (Buf Cur) Adjustment Effect

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As can be seen, the increase of the BufCur control code increases the channel's gain for any gain settings other than maximum. This control also adjusts the channel's linearity: the higher values of the code correspond to higher linearity and higher power consumption of the chip. To keep the chip in its operational range, it is not recommended to drop the BufCur all the way to its minimum value.

Corresponding controls are detailed in Table 2. Increase of any control results in gain increase within a certain frequency range around the specified frequency as shown in the corresponding drawings.

Table 2. Data Channel Controls

Control function	Frequency, *GHz*	SPI name	GUI Slider name	Corresponding drawing
Low-frequency zero	1	zcl_X	Zero at f / Lo	Fig. 5
Mid-frequency zero	5	zcm_X	Zero at f / M	Fig. 6
High-frequency zero	16	zch_X	Zero at f / Hi	Fig. 7
First pole	16	pc1_X	Pole / 1	Fig. 8
Second pole	16	pc2_X	Pole / 2	Fig. 9
Gain	DC	gc_X	Gain	Fig. 10
Output EF	>20	efcX	Out BW	Fig. 11
Input EF	>20	efc12	Input BW	Fig. 12
Buf current	DC	bufc_Y	Buf Cur	Fig. 13

Here X is the channel (or output) number that equals to 1 or 2 and Y is the Group number that equals A or B. In the GUI, X=1 corresponds to Channel 1 in Group A, or Channel 3 in Group B, and X=2 corresponds to Channel 2 in Group A, or Channel 4 in Group B.

Peak Detector

The Peak Detector block represents the single-ended swing of its input signal as an output voltage between 1.65*V* to 2.85*V*. The typical characteristics for a 1*GHz* sinusoidal input signal at different PT operational conditions are shown in Fig. 14.

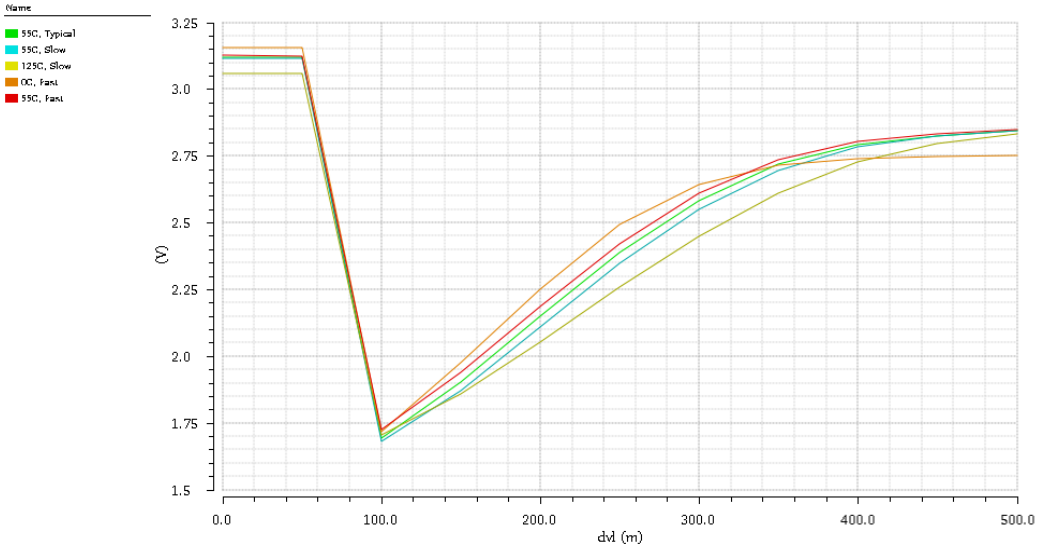

Fig. 14. Peak Detector Typical Simulated Characteristics for Different T° and Process Corners

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As can be seen in the plot, the signal swings below a certain value are represented by the high voltage above 3.0V. This function can be used as an indication of NO Input Signal (Loss-of-signal, or LOS). The LOS threshold can be adjusted through the SPI as shown in Fig. 15.

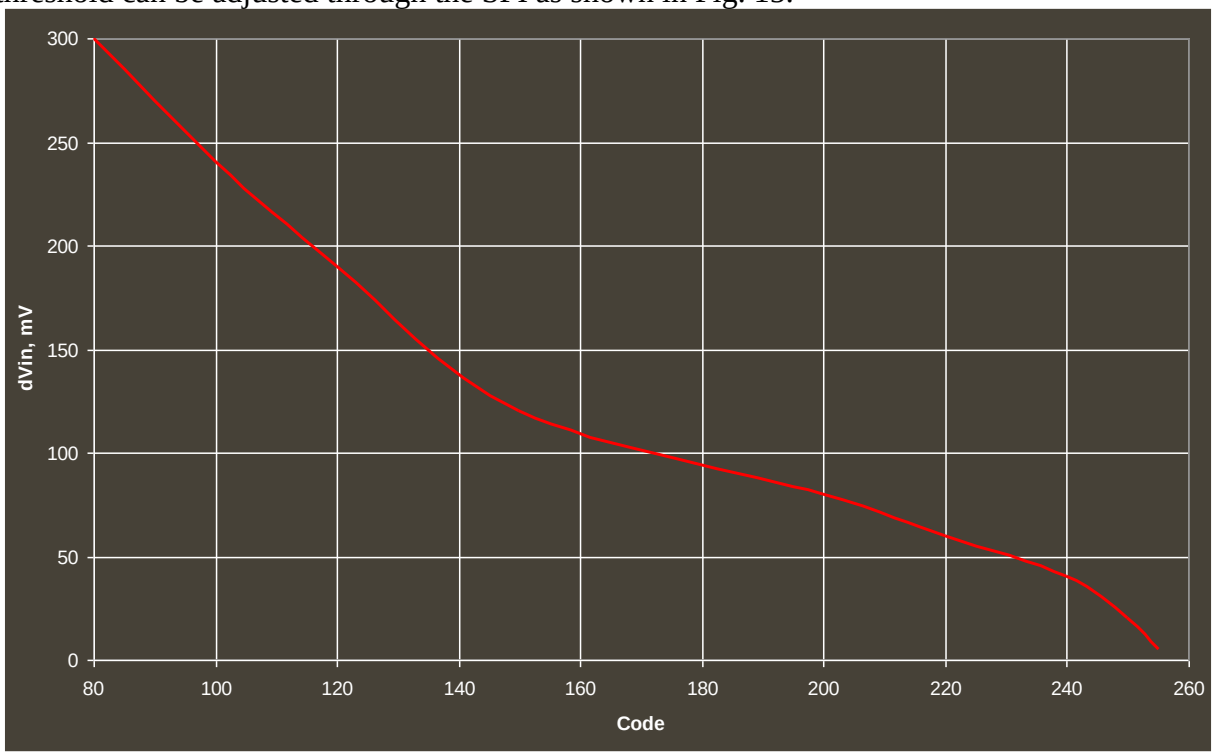
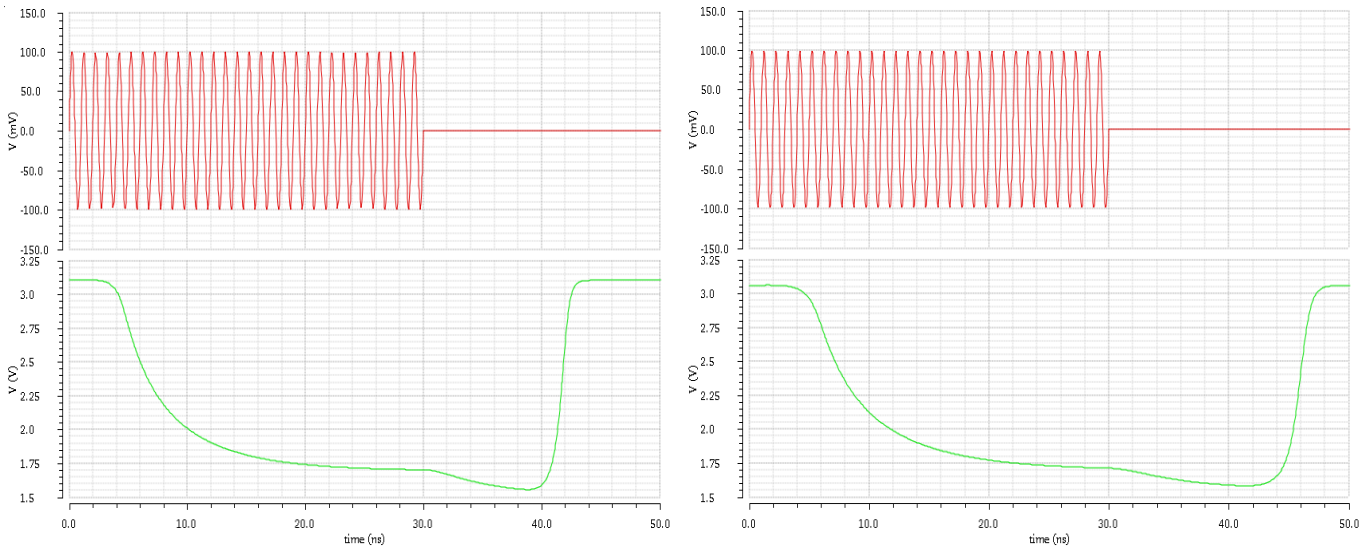


Fig. 15. LOS Threshold Adjustment Range

The Peak Detector features a short settling time as seen in Fig. 16 which shows the sinusoidal input signal, and the Peak Detector output at different operational conditions.



a. b.

Fig. 16. Peak Detector settling Time (a – Nominal, b – Worst Case Slow)

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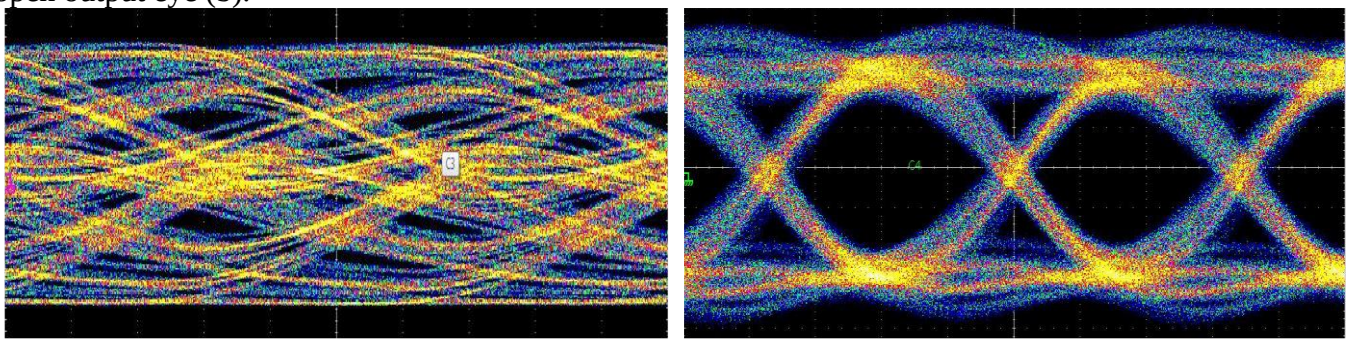
Examples of Recovered Signals

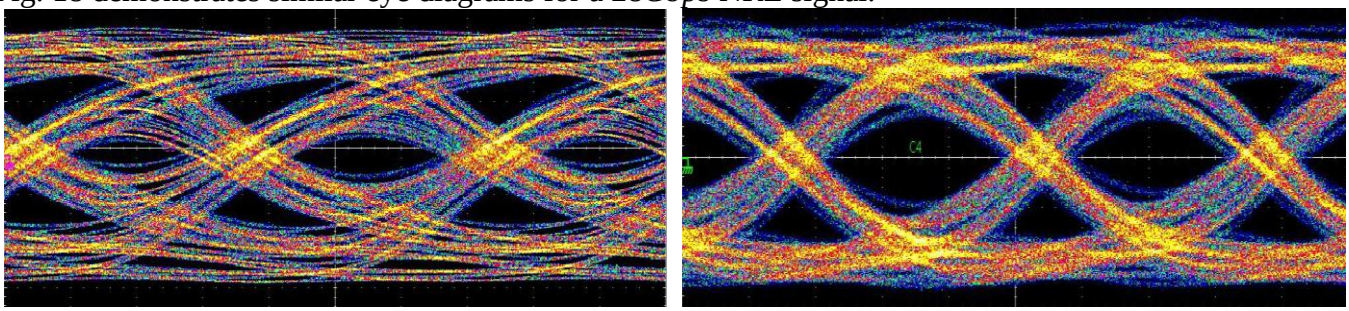
The following examples illustrate the functionality of the ASNT6154-KHS. Fig. 17 demonstrates the reconstruction of an almost completely closed eye diagram of an input 20*Gbps* NRZ signal (a) into a well open output eye (b).



a. b.

Fig. 17. 20Gbps NRZ PRBS31 Signal (a – before CTLE, b – after CTLE)

Fig. 18 demonstrates similar eye diagrams for a 28*Gbps* NRZ signal.



a. b.

Fig. 18. 28Gbps NRZ PRBS31 Signal (a – before CTLE, b – after CTLE)

The corresponding settings of the CTLE's channels are shown in Fig. 19a and Fig. 19b.

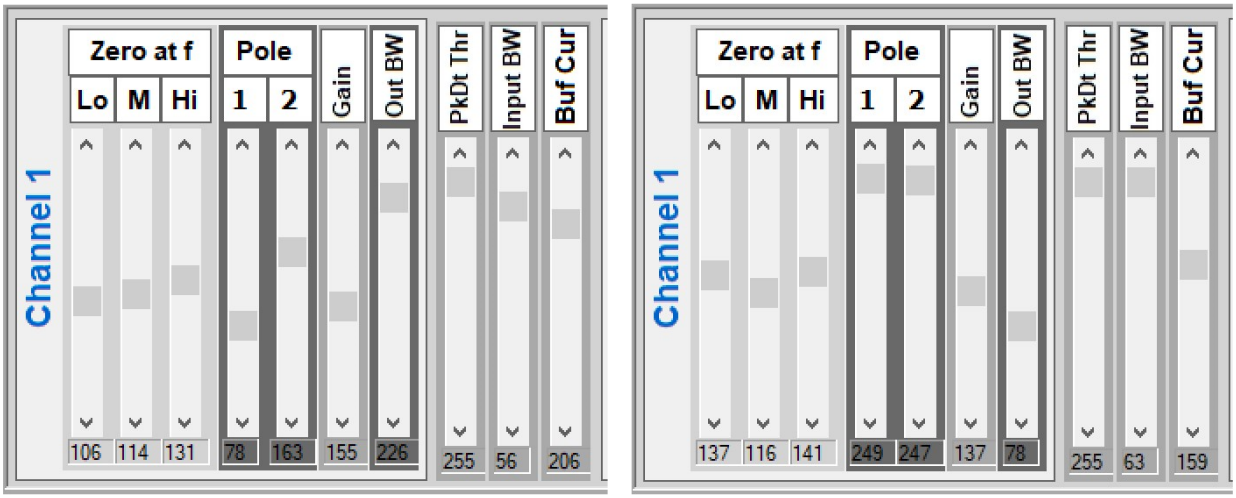


Fig. 19. Equalizer settings for Fig. 17 and Fig. 18

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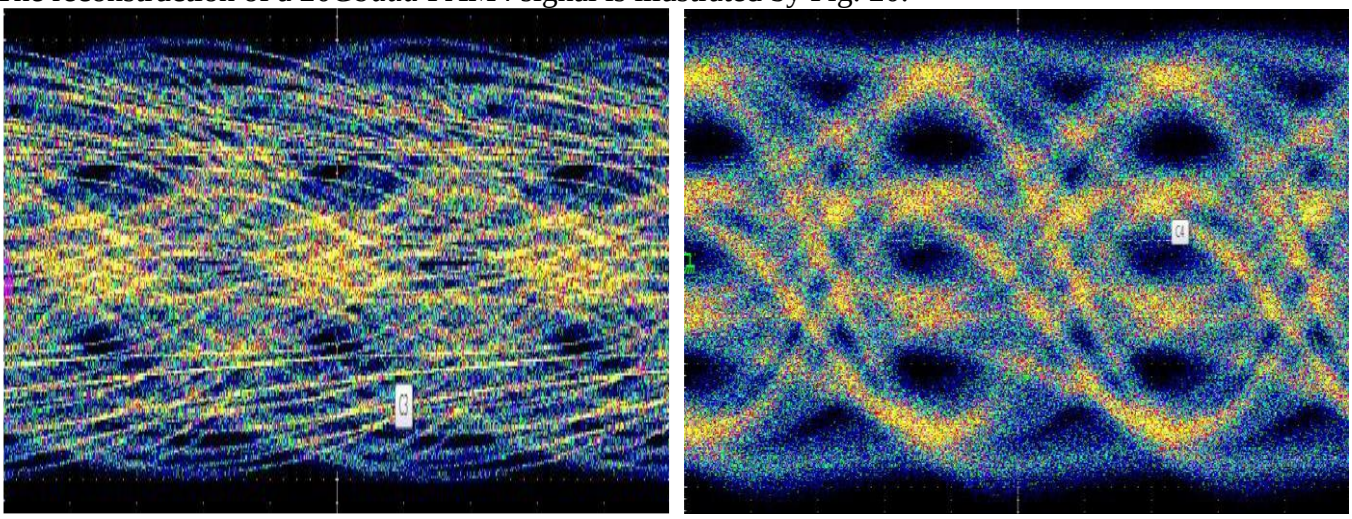
The reconstruction of a 20*Gbaud* PAM4 signal is illustrated by Fig. 20.



a. b.

Fig. 20. 20Gbps PAM4 PRBS31 Signal (a – before CTLE, b – after CTLE)

3-Wire Interface

All functions of the IC are controlled through a 3-wire SPI. The interface includes an 18-byte internal register and operates with 3.3*V* CMOS signals. It provides control signals for any of 2 groups of channels: Group A (Channels 1 and 2), and Group B (Channels 3 and 4). Each group data can be loaded independently, and the active group is selected by bit1 of byte18 in each data packet. The bit map of the interface is shown in Table 3, and its timing diagram in Fig. 21.

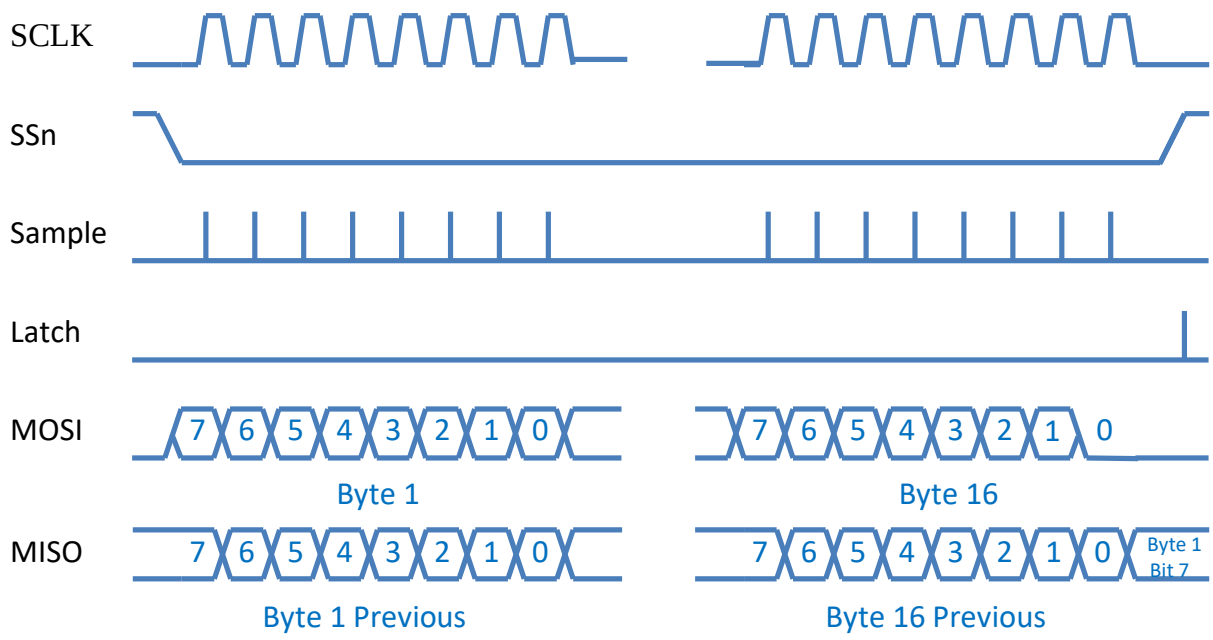


Fig. 21. SPI Timing Diagram

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Table 3. 3-Wire Interface Bit Map

Byte #	Bit #	Bit order	Signal name	Default Value	Signal function
1	From 7 to 0	MSB LSB	zcl_1	10000000	Low-frequency zero control for the first output of the selected Group
2	From 7 to 0	MSB LSB	zcm_1	10000000	Middle-frequency zero control for the first output of the selected Group
3	From 7 to 0	MSB LSB	zch_1	01000000	High-frequency zero control for the first output of the selected Group
4	From 7 to 0	MSB LSB	gc_1	10000000	Gain control for the first output of the selected Group
5	From 7 to 0	MSB LSB	pc1_1	10000000	First pole control for the first output of the selected Group
6	From 7 to 0	MSB LSB	pc2_1	10000000	Second pole control for the first output of the selected Group
7	From 7 to 0	MSB LSB	efc1	10000000	BW control for the first output of the selected Group
8	From 7 to 0	MSB LSB	zcl_2	10000000	Low-frequency zero control for the second output of the selected Group
9	7		ontrmn	1	Input termination and DC common mode control bits, see Table 1 for details
	6		offtrmp	0	
	5 to 0		-	00000	Not used
10	From 7 to 0	MSB LSB	bufc	10010010	Linearity control for both channels of a Group through stages current adjustment
11	From 7 to 0	MSB LSB	zcm_2	10000000	Middle-frequency zero control for the second output of the selected Group
12	From 7 to 0	MSB LSB	zch_2	01000000	High-frequency zero control for the second output of the selected Group
13	From 7 to 0	MSB LSB	gc_2	10000000	Gain control for the second output of the selected Group
14	From 7 to 0	MSB LSB	pc1_2	10000000	First pole control for the second output of the selected Group
15	From 7 to 0	MSB LSB	pc2_2	10000000	Second pole control for the second output of the selected Group
16	From 7 to 0	MSB LSB	efc2	10000000	BW control for the second output of the selected Group
17	From 7 to 0	MSB LSB	losth1	10000000	LOL threshold control for the selected Group
18	From 7 to 2	MSB LSB	efc12	100000	Additional BW control for both outputs of the selected Group
	1		wraddr	0	“0”– write to Group A, “1”– write to Group B
	0		-	0	Constant “0”

The SPI registers are preset to the above default states at the time of the IC power supply activation.

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TERMINAL FUNCTIONS

TERMINAL			Description
Name	**No.**	**Type**	
High-Speed I/Os			
d1p	36	CML-type Analog Inputs with switchable termination	Differential high-speed channel 1 data inputs with internal SE 46*Ohms* termination to vcc
d1n	38		
d2p	40		Differential high-speed channel 2 data inputs with internal SE 46*Ohms* termination to vcc
d2n	42		
q11p	27	CML-type Analog Outputs	Differential high-speed channel 1 path 1 data outputs with internal SE 46*Ohms* termination to vcc
q11n	25		
q12p	20		Differential high-speed channel 1 path 2 data outputs with internal SE 46*Ohms* termination to vcc
q12n	18		
q21p	16		Differential high-speed channel 2 path 1 data outputs with internal SE 46*Ohms* termination to vcc
q21n	14		
q22p	9		Differential high-speed channel 2 path 2 data outputs with internal SE 46*Ohms* termination to vcc
q22n	7		
Low-Speed I/Os			
SSn	31	3.3*V* CMOS I/Os	3-wire interface enable input with internal 474*kOhms* pull-up to vcc
SCLK	33		3-wire interface clock input with internal 474*kOhms* pull-down to vee
MOSI	1		3-wire interface data input with internal 474*kOhms* pull-down to vee
MISO	3		3-wire interface data output
pkd1	29	CMOS Output	Error Detector output and below-threshold signal amplitude indicator, with internal 6*kOhms* SE termination to vcc
pkd2	5		

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
v5p0	+5.0*V* positive power supply Negative pin to vee	11, 23
vee	Ground	12, 22, 34, 44
vcc	+3.3*V* positive power supply Negative pin to vee	2, 4, 6, 8, 10, 13, 15, 17, 19, 21, 24, 26, 28, 30, 32, 35, 37, 39, 41, 43

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 4 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

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Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Main Supply Voltage (vcc)		3.6	*V*
Additional Supply Voltage (v5p0)		5.5	*V*
RF Input Voltage Swing (SE)		750	*mV*
Case Temperature		+85	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee		0.0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	vcc in relation to vee
v5p0	4.8	5.0	5.3	*V*	v5p0 in relation to vee
I_{v5p0}	8		35	*mA*	Depending on the state of SPI control bytes
I_{vcc}	300	450	600	*mA*	
Power Consumption	0.4	1.4	2.1	*W*	
vcc ramp length			10	*ms*	For reliable SPI preset
Junction temperature	0	50	125	*°C*	
Data input (d1p/d1n, d2p/d2n)					
Data Rate	DC		32	*Gb/s*	
SE Swing (1*GHz* differential signal)	200		440	*mV*	0.3% THD, Min/Max bufc
	330		530	*mV*	0.9% THD, Min/Max bufc
CM Level	vcc-1.3		vcc-0.3	*V*	see Table 1 for details
Input termination	35		50	*Ohms*	
		25		*kOhms*	
Data output (q11p/q11n, q12p/q12n, q21p/q21n, q22p/q22n)					
Max peaking frequency	20		33	*GHz*	
Gain from Input	-3		+5	*dB*	Depending on SPI settings
CM Level		vcc-0.35		*V*	for DC output termination
Peak Detector output (pkd1, pkd2)					
Voltage range	1.6		2.8	*V*	For input swing control
	3.05		3.25	*V*	For LOS operation
Settling time	15		20	*ns*	
3-Wire Interface					
Clock frequency	0.1		50	*MHz*	
Input low logic level	vee		vee+0.4	*V*	
Input high logic level	vcc-1.3		vcc	*V*	
Output low logic level	vee		vee+0.2	*V*	
Output high logic level	vcc-0.3		vcc	*V*	
Input current			9	*uA*	For each input

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PACKAGE INFORMATION

The die is housed in a custom, 44-pin CQFN package shown in Fig. 22. The package provides a center heat slug located on the back side of the package to be used for heat dissipation. ADSANTEC recommends using extreme caution when soldering this section to the board to avoid overheating. It should be connected to the vcc plain that is ground for the negative supply, or power for the positive supply.

The part's identification label is ASNT6154-KHS. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

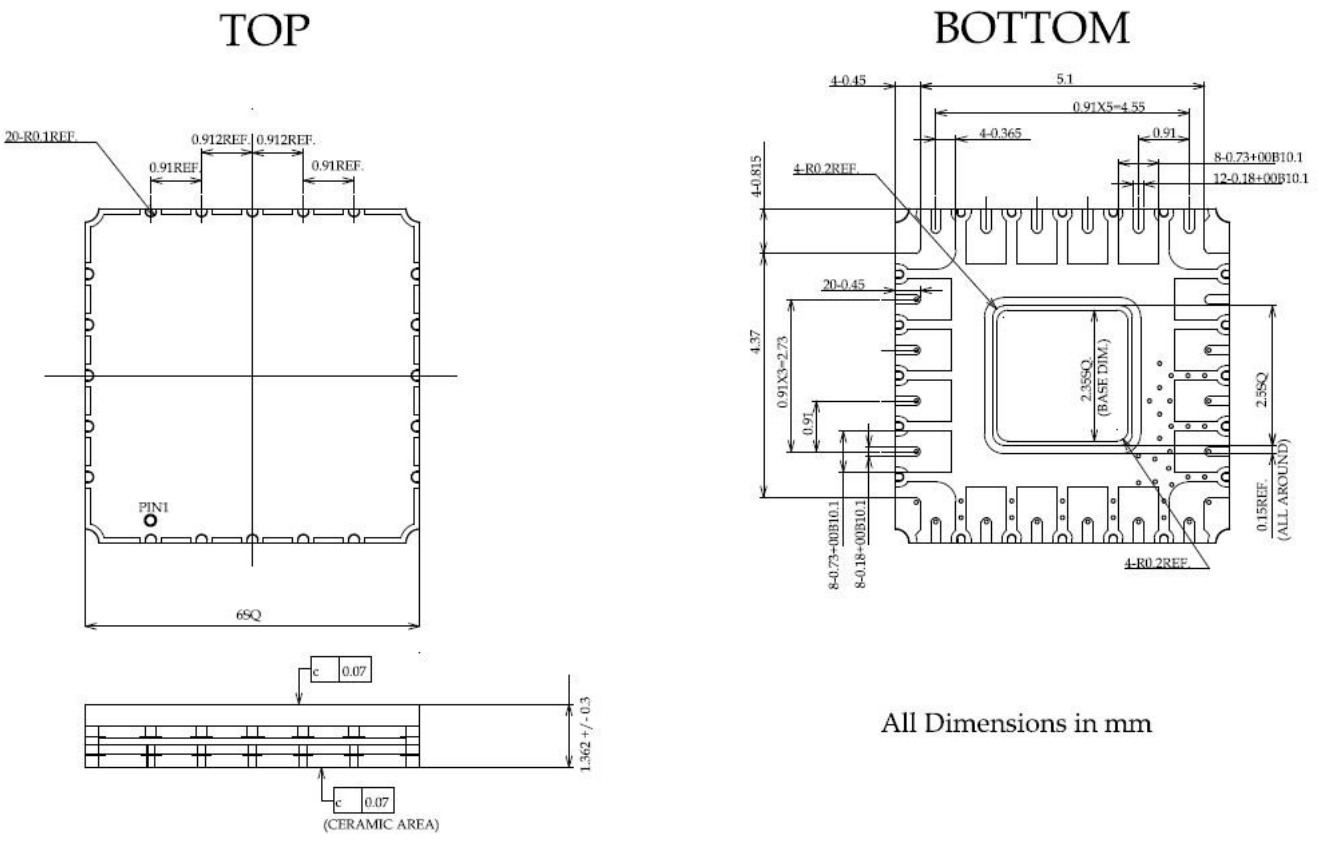

Fig. 22. CQFN44 Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.0.2	12-2023	First release
0.3.2	11-2023	Added plots of individual control ranges Added eye diagram examples
0.2.2	04-2023	Updated Package Drawing
0.1.2	04-2023	Updated Package Drawing
0.0.1	03-2022	Preliminary release