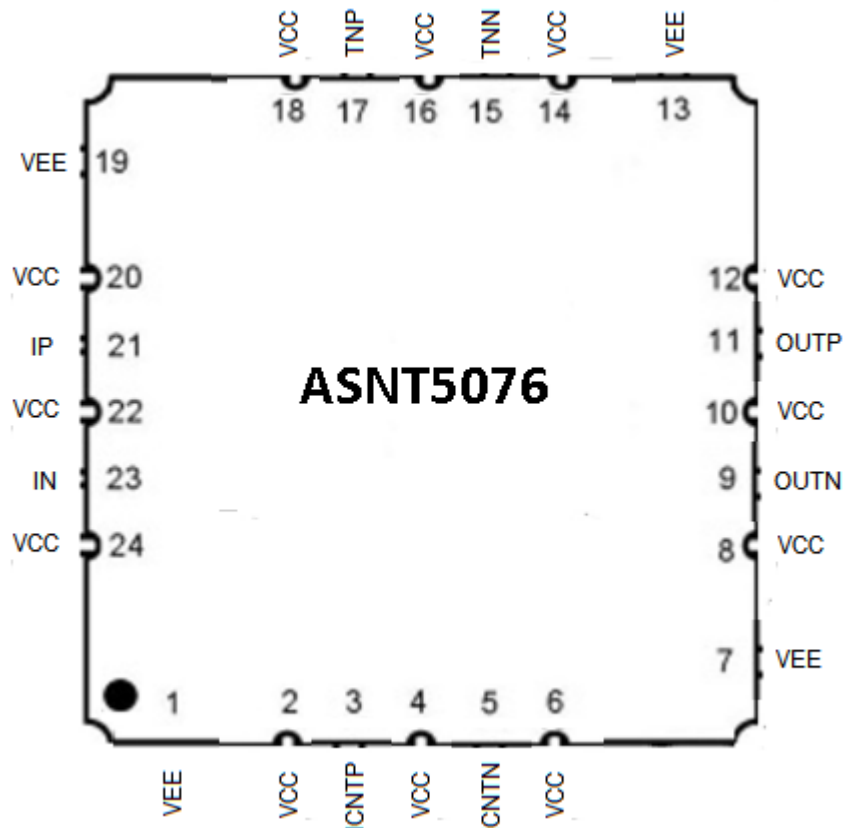# ASNT5076-KHC
DC-28*Gbps*/16*GHz* Signal Phase Shifter with Amplitude Control

- Broadband (DC-28*Gbps/*DC-16*GHz*) tunable data/clock phase shifter

- Delay adjustment range of 155*ps*

- Exhibits low jitter and limited temperature variation over industrial temperature range

- 1*GHz* of bandwidth for the phase adjustment tuning ports

- Ideal for high speed proof-of-concept prototyping

- Fully differential CML input interfaces

- Fully differential CML output interface with adjustable SE amplitude from 0 to 1.0*V*

- 10*MHz* of bandwidth for the amplitude adjustment tuning ports

- Single +3.3*V* or -3.3*V* power supply

- Power consumption: 1.36*W*

- Fabricated in SiGe for high performance, yield, and reliability
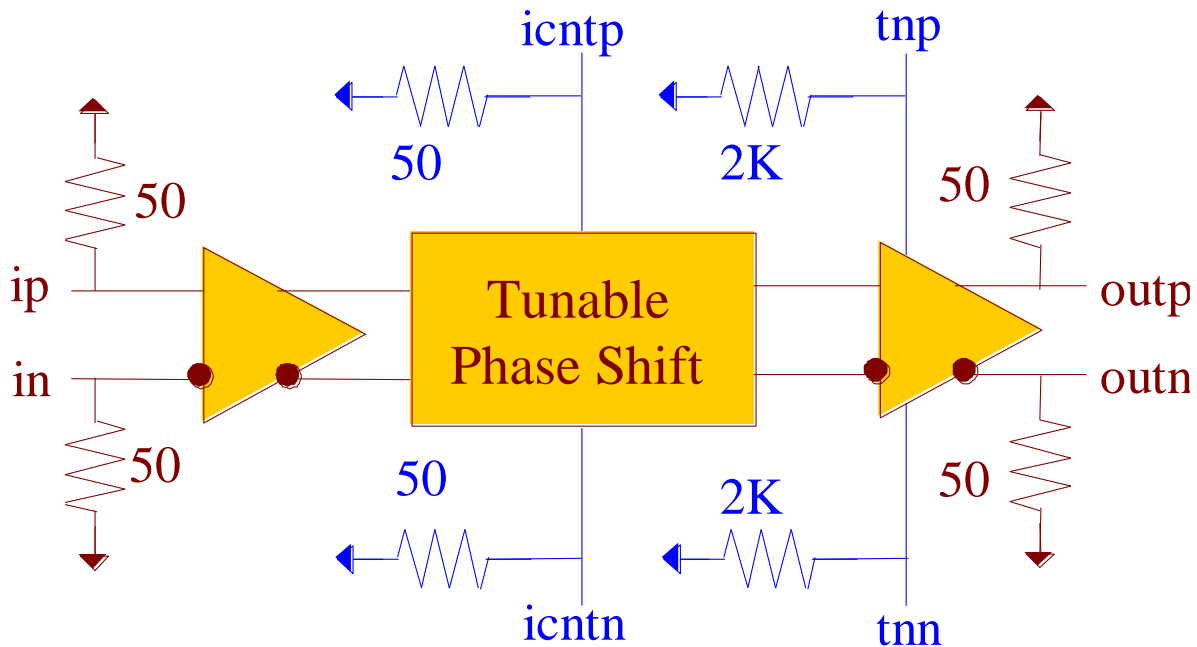
- Custom CQFN 24-pin package

DESCRIPTION

Fig. 1. Functional Block Diagram

ASNT5076-KMC is a data / clock variable delay line fabricated in SiGe technology. The IC shown in Fig. 1 provides an adjustable delay of its differential output signal outp/outn in relation to its broadband input signal ip/in. The delay adjustment range is temperature-stabilized. The delay is controlled through a wide-band differential tuning port icntp/icntn.

The part's I/O's support the CML logic interface with on chip $50 Ohm$ termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

The output amplitude is controlled through a wide-band differential tuning port tnp/tnn. Due to an extremely low jitter, the part is suitable for use in high-speed measurement / test equipment.

Delay Control Port

The delay is controlled through a wide-band differential tuning port icntp/icntn. The delay control diagram is shown in Fig. 2.
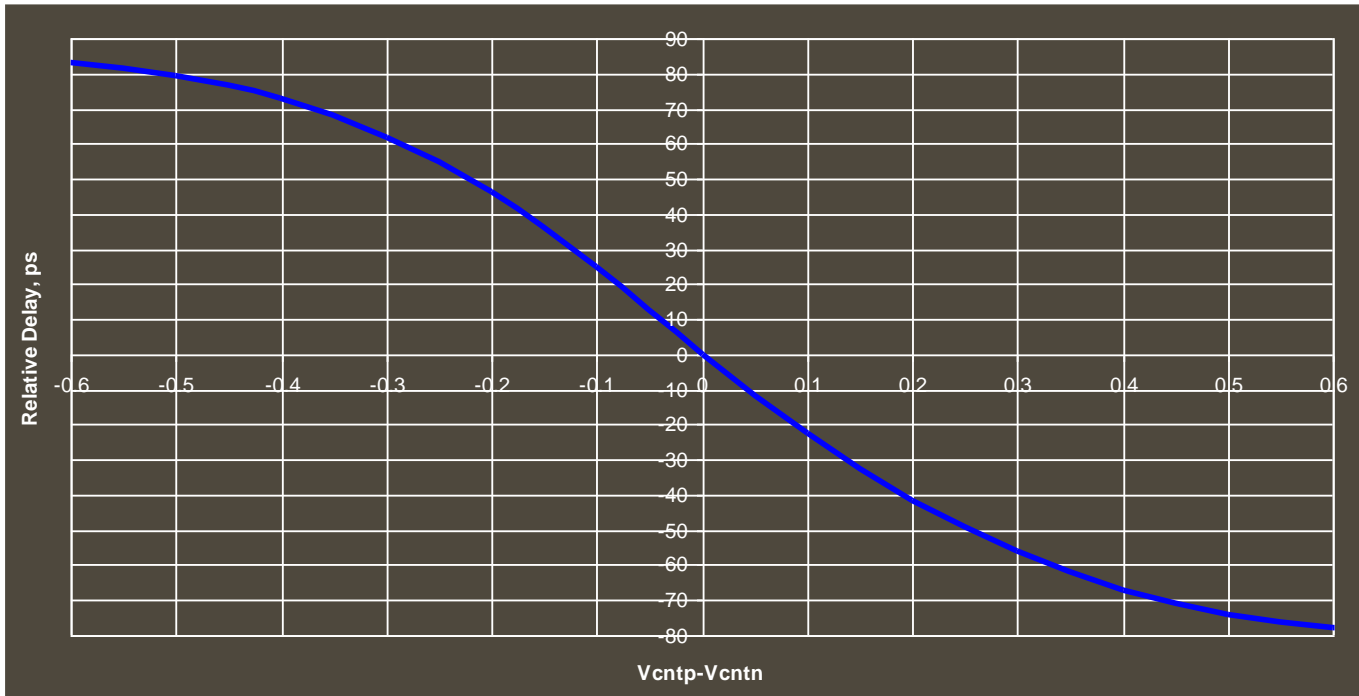
Fig. 2. Delay Control Diagram

Amplitude Control Port

The output amplitude is controlled through a wide-band differential tuning port tnp/tnn. The amplitude control diagram is shown in Fig. 3.
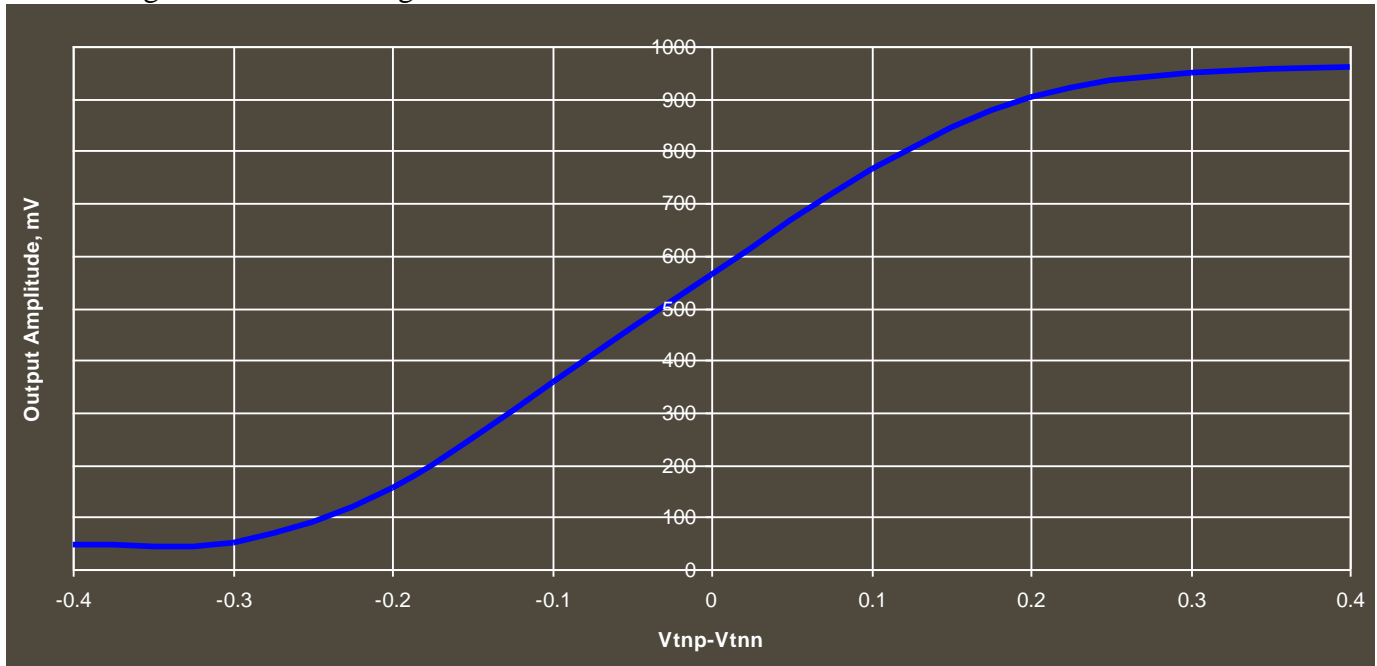

Fig. 3. Amplitude Control Diagram

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0V = ground and vee = −3.3V), or a positive supply (vcc = +3.3V and vee = 0.0V = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50Ohm termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0V and vee = -3.3V.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		1.5	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	^oC
Storage Temperature	-40	+100	^oC
Operational Humidity	10	98	$\%$
Storage Humidity	10	98	$\%$

TERMINAL FUNCTIONS

Name	No.	Type	DESCRIPTION
High-Speed I/Os			
ip	21	CML input	Differential high-speed signal inputs with internal SE 50Ohm termination to vcc
in	23		
icntp	3	CML input	Differential high-speed control inputs with internal SE 50Ohm termination to vcc
icntn	5		
tnp	17	Input	Differential low-speed control inputs with internal SE 2KOhm terminations to vcc
tnn	15		
outp	11	CML output	Differential high-speed signal outputs with internal SE 50Ohm termination to vcc. Require external SE 50Ohm termination to vcc
outn	9		

Supply and Termination Voltages

| Name	Description	Pin Number
vcc	Positive power supply (+3.3V or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0V or -3.3V)	1, 7, 13, 19

ELECTRICAL CHARACTERISTICS

| PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
Ivee		410		mA	
Power consumption		1355		mW	
Junction temperature	-40	25	125	$°C$	
HS Input Data/Clock (ip/in)					
Data Rate	DC		28	$Gbps$	
Frequency	DC		16	GHz	For clock signals
Swing	0.05		1.0	V	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
HS Output Data/Clock (outp/outn)					
Data Rate	DC		28	$Gbps$	
Frequency	DC		16	GHz	For clock signals
Logic "1" level		vcc		V	
Highest logic "0" level		vcc		V	With external $50Ohm$ DC termination
Lowest logic "0" level	vcc-1.0		vcc-0.93	V	and full range of tnp/tnn control signal
Rise/Fall times	6		10	ps	20%-80%
Output Jitter			1	ps	Peak-to-peak
Duty cycle	45	50	55	$%$	For clock signal
Output-to-Input Delay					
Adjustment range		160		ps	At $1GHz$	For the full range of
		155		ps	At $15GHz$	icntp/icntn control signals
Absolute delay stability	-2		2	ps	0-125°C
Phase Shift Control port (icntp/icntn)					
Bandwidth	DC		1000	MHz	
SE voltage level	vcc-600		vcc	mV	Half control range when the opposite pin is at vcc
SE voltage level	vcc-1200		vcc	mV	Full control range when the opposite pin is at vcc-0.6V
Differential swing	0		1200	mV	Peak-peak, full control range
CM Level		vcc-(Diff. swing)/4		V	In differential mode
Output Amplitude port (tnp/tnn)					
Bandwidth	DC		10	MHz	
SE voltage level	vcc-400		vcc	mV	Half control range when the opposite pin is at vcc
SE voltage level	vcc-800		vcc	mV	Full control range when the opposite pin is at vcc-0.4V
Differential swing	0		800	mV	Peak-peak, full control range
CM Level		vcc-(Diff. swing)/4		V	In differential mode

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFN package shown in This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

 4. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.
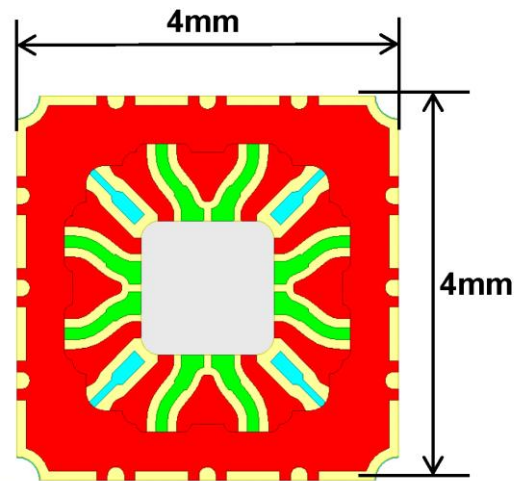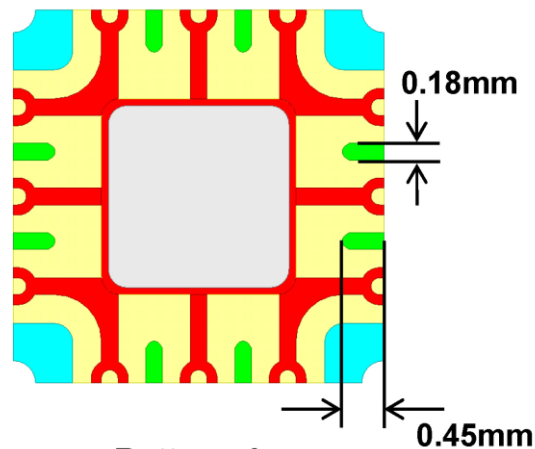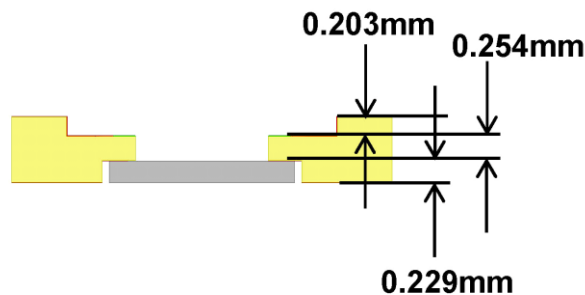
Fig. 4. CQFN 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT5076-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.0.2	11-2021	First release