ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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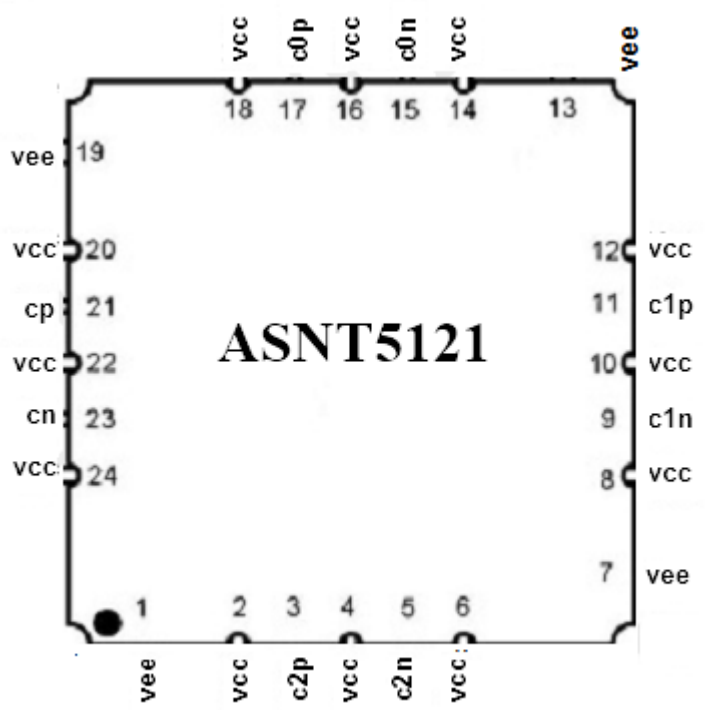
ASNT5121-KHC
DC-50*Gbps*/32*GHz* Signal Distributor 1-to-3

- High-speed broadband Data/Clock Amplifier and Distributor
- Exhibits low jitter and limited temperature variation over industrial temperature range
- One input differential signal port and three differential amplified output signal ports
- Matched phase delays for all outputs
- Fully differential CML input interfaces
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 580*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFN 24-pin package



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DESCRIPTION

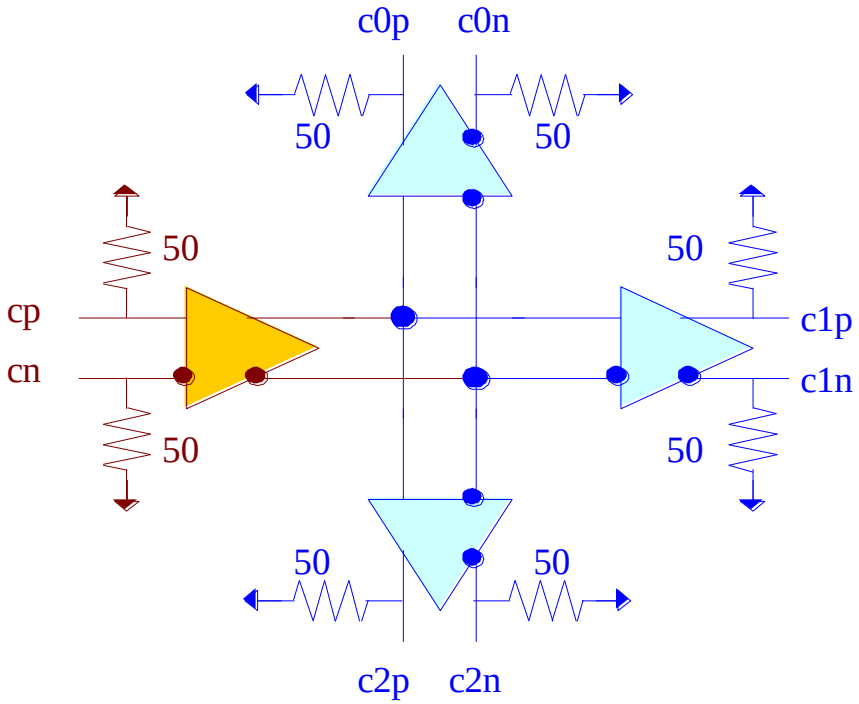

Fig. 1. Functional Block Diagram

The temperature stable ASNT5121-KHC SiGe IC provides active broadband data/clock signal splitting, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can process a broadband high-speed data/clock input signal cp/cn and deliver three broadband high-speed data/clock phase matched output signals c0p/c0n, c1p/c1n, c2p/c2n.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.64	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cp	21	CML input	Differential high speed data/clock inputs with internal SE 50*Ohm* termination to vcc.
cn	23		
c0p	17	CML output	Differential high speed data/clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc.
c0n	15		
c1p	11	CML output	Differential high speed data/clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc.
c1n	9		
c2p	3	CML output	Differential high speed data/clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc.
c2n	5		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)	1, 7, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		175		*mA*	
Power consumption		580		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data/Clock (cp/cn)					
Data Rate	DC		50	*Gbps*	
Frequency	DC		32	*GHz*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Data/Clock (c0p/c0n, c1p/c1n, c2p/c2n)					
Data Rate	DC		50	*Gbps*	
Frequency	DC		32	*GHz*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Rise/Fall times	6	8	10	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak
Duty cycle	45	50	55	*%*	For clock signal

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFN package shown in **Error! Reference source not found.**. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5121-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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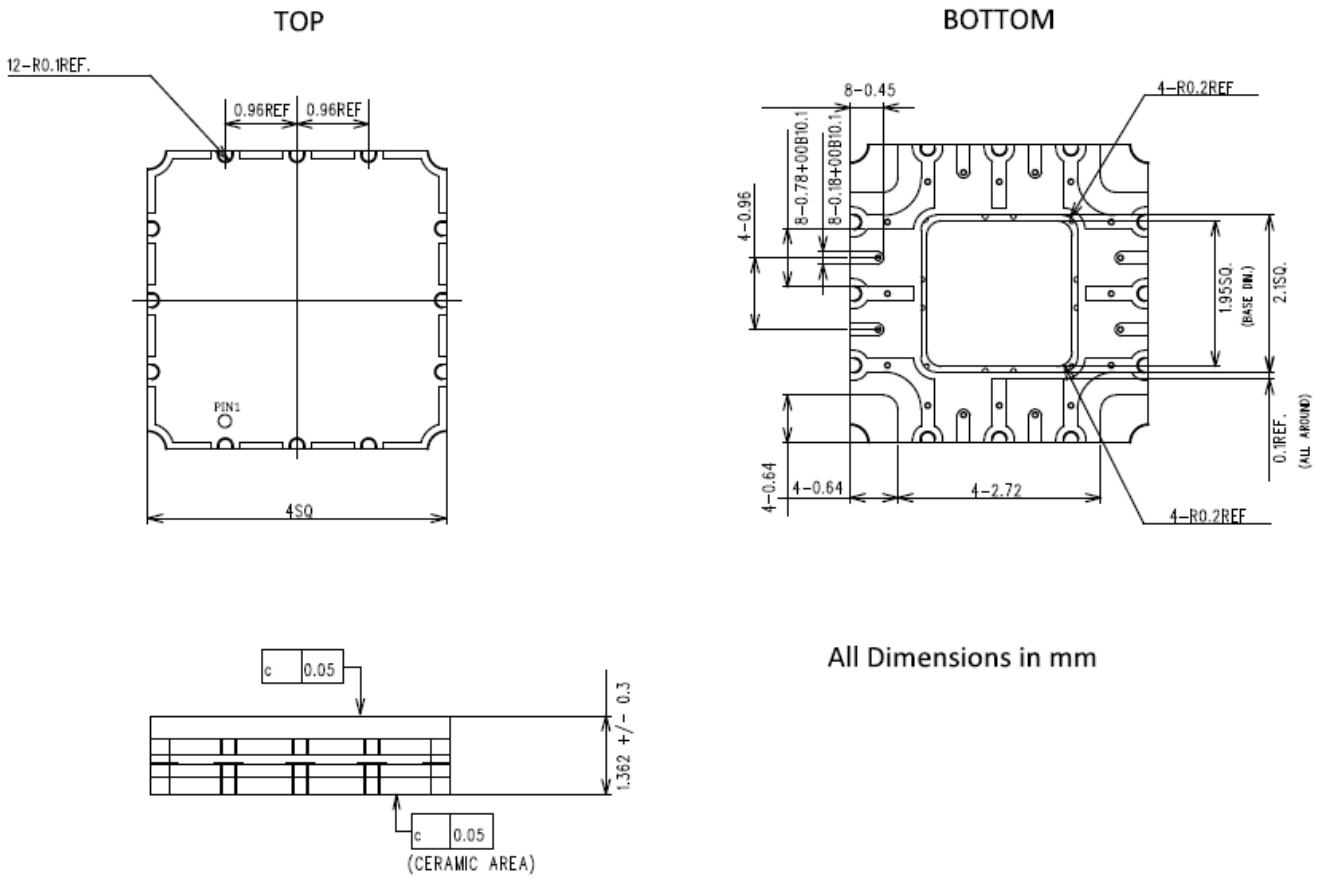

Fig. 2. CQFN 24-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.0.3	04-2023	Updated Package Drawing
1.0.2	08-2021	Initial Release