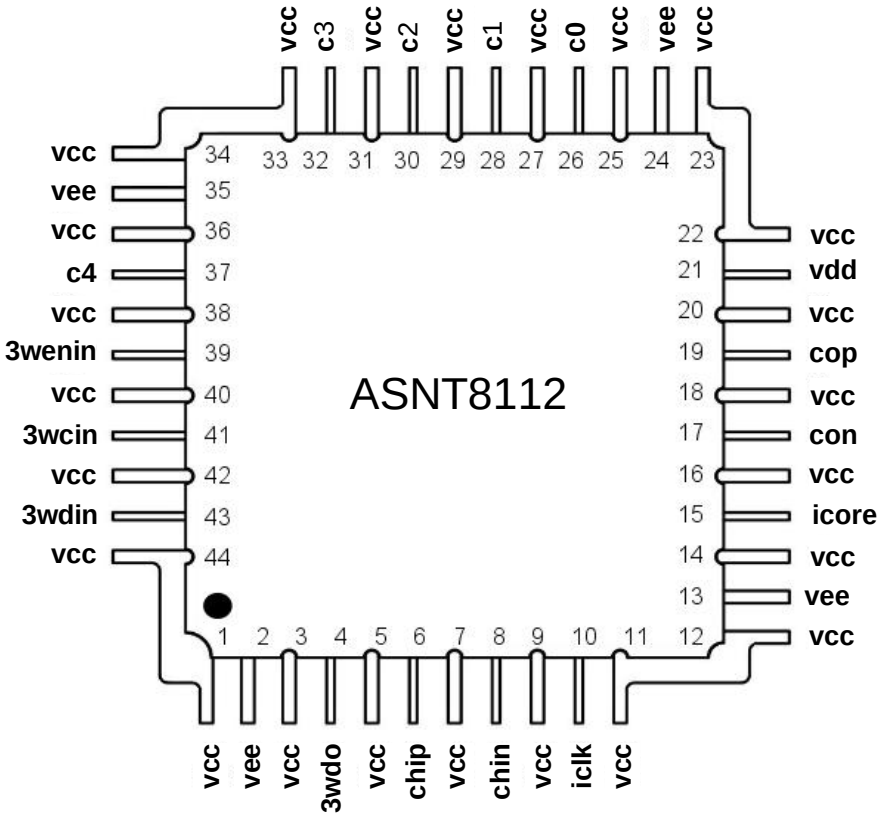
ASNT8112-KMM
DC-to-32*GHz* Programmable Integer Divider with SPI

- Wide frequency range from DC to 32*GHz*
- Continuous integer division ratios from 1 to 32
- 50% duty cycle of the output divided clock signal
- Fully differential CML input and output interfaces
- Adjustable power consumption
- Easy 5-bit parallel programming interface compatible with CMOS/LVTTL standards
- Optional controls via 3-wire SPI interface
- Dynamic division ratio adjustment with a short set-up time (about 20*ns* after the pulse edge on any control input)
- Single +2.8*V* or -2.8*V* power supply
- Industrial temperature range
- Standard 44-pin CQFP package with a thermal pad



DESCRIPTION

This part is a high-speed programmable integer clock divider with dynamic adjustment of the division ratio. The functional block diagram of the device is shown in Fig. 1.

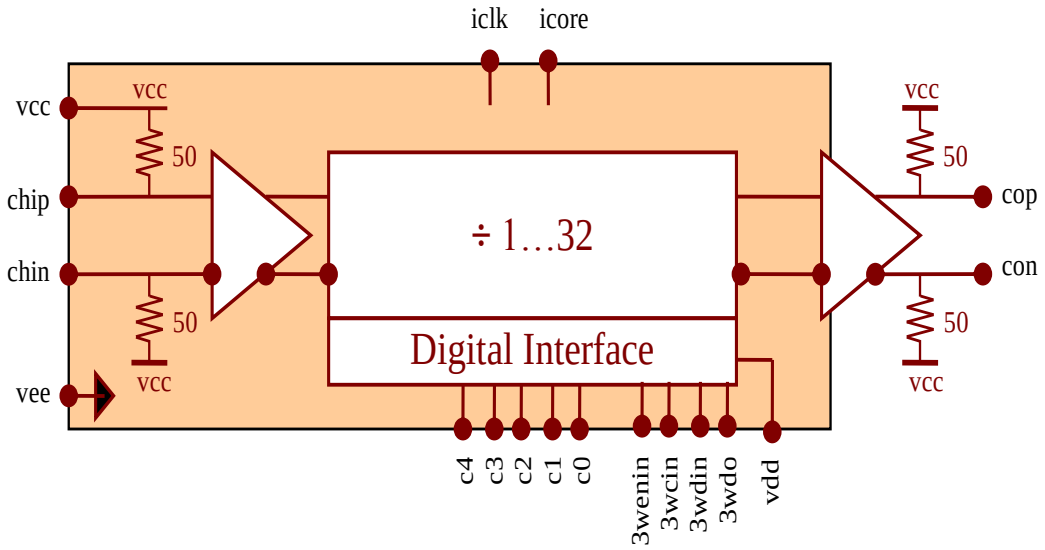


Fig. 1. Functional Block Diagram

The divider accepts an input clock signal (chip/chin) with a speed from DC to the maximum specified frequency, and provides a clean 50% duty cycle output divided clock signal (cop/con) in any operational mode. The divider allows for dynamic adjustment of the division ratio from 1 to 32 with a step of 1 through either a full-scale CMOS 5-bit parallel interface, or a 1.2*V* CMOS 3-wire SPI. The parallel or serial interface mode is selected via the SPI interface. If the SPI interface is not connected, the parallel controls are active by default.

In parallel mode, a binary code on the control inputs (c0-c4) defines the value of the ratio from 1 to 32, where c4 is the most significant bit (MSB). All "0"s ("low" state) defines division by 32. Following the change of any control signal, the divider switches to idle after (64...128) periods of the high-speed system clock plus an additional 1.6*ns* delay, and returns back to normal operation with the new division ratio after an additional delay equal to 192 periods of the high-speed system clock.

In serial mode, the 1-byte division coefficient code is supplied through the 3-wire interface with MSB first as shown in Fig. 2.

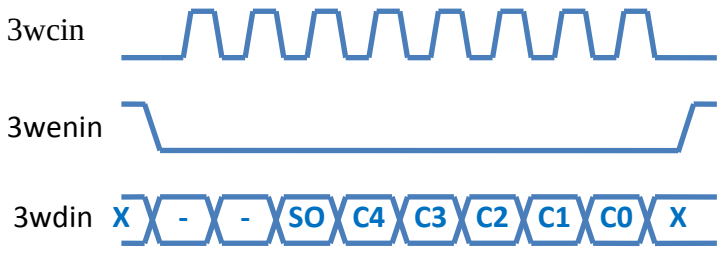


Fig. 2. SPI Bit Order

The input data 3wdin is sampled at rising edges of the SPI clock 3wcin, and the internal division coefficient value will be updated at the rising edge of the 3wenin signal. The first two bits are not functional, and the third bit SO enables the serial interface (SPI ON) which then allows bits C4 through C0 to set the division

ratio. The device automatically resets itself after initial power-up, and any change of the division control signals.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc=0.0*V*=ground), or a positive supply (vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

The parts power consumption may be reduced by up to 30% using external resistors to connect the control ports iclk and icore to vee. **It is recommended to modify iclk first, and then modify icore if required because a current reduction results in a lower maximum operational frequency and icore has a larger impact than iclk!**

All the characteristics detailed below assume vcc = +2.8*V* and vee = 0*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	**Min**	**Max**	**Units**
Supply Voltage (vcc)		+3.3	*V*
Power Consumption		3.2	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			**DESCRIPTION**
Name	**No.**	**Type**	

High-Speed I/Os			
chip	6	CML input	Differential clock inputs with internal SE 50*Ohm* termination to vcc.
chin	8		
cop	19	CML output	Differential divided clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc.
con	17		
Low-Speed I/Os			
3wenin	39	1.2*V* CMOS input	3-wire enable active-low signal (SSn), 474*KOhm* pull-up to vdd
3wcin	41		3-wire input clock (SCLK), 474*KOhm* pull-down to vee
3wdin	43		3-wire input data (MOSI) , 474*KOhm* pull-down to vee
3wdo	4	1.2*V* CMOS output	3-wire ouptut data (MISO), no internal termination
Digital Controls			
c0	26	vee/vcc CMOS input	Division binary control signals with internal 474*KOhm* termination to vee
c1	28		
c2	30		
c3	32		
c4	37		
Analog Controls			
iclk	10	Analog input	Power control ports with internal 800*Ohm* termination to vee; require external resistors between 120*Ohm* and 6*KOhm* connected to vee or external power supplies with current sinking capability; may be left not connected
icore	15		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Main positive power supply or ground	1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44
vdd	Digital positive power supply	21
vee	Negative power supply or ground	2, 13, 24, 35

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee		0.0		*V*	External ground
vcc	2.6	2.8	3.0	*V*	
vdd	1.2		1.3	*V*	negligible current consumption
*I*vee		500		*mA*	R=120*Ohm* between iclk/icore and vee

		800		*mA*	R>6*KOhm* between iclk/icore and vee
Power consumption		1.4		*W*	R=120*Ohm* between iclk/icore and vee
		2.2		*W*	R>6*KOhm* between iclk/icore and vee
Junction temperature	-25	50	125	*°C*	
Input (chip/chin)					
Frequency	0.0		32	*GHz*	
Swing	75	400	1000	*mV*	Differential or SE, p-p; at 6*GHz*
CM Level	vcc- (SE swing)/2				
Rise/Fall Times			3	*ns*	20%-80%
Output (cop/con)					
Frequency	0.0		32	*GHz*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.6		*V*	With external 50*Ohm* DC termination
Rise/Fall Times	10	13	16	*ps*	20%-80%
Additive Jitter		TBD		*ps*	Peak-to-Peak
Duty Cycle	47%	50%	53%		For clock signal
Select (c0-c4)					
Logic "1" level	V_{CC}-0.4			*V*	
Logic "0" level			V_{EE}+0.4	*V*	

PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8112-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

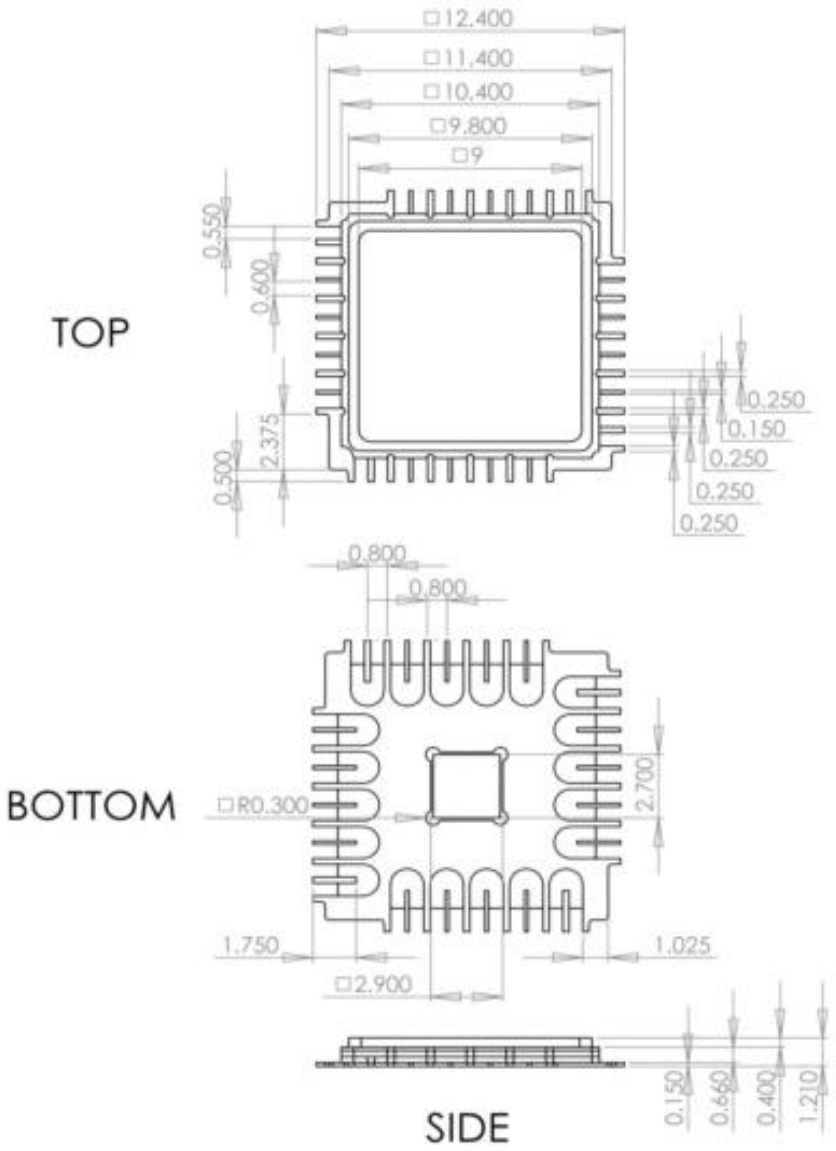


Fig. 3. CQFP 44-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.1.2	09-2021	Corrected format
1.0.2	07-2021	First release