ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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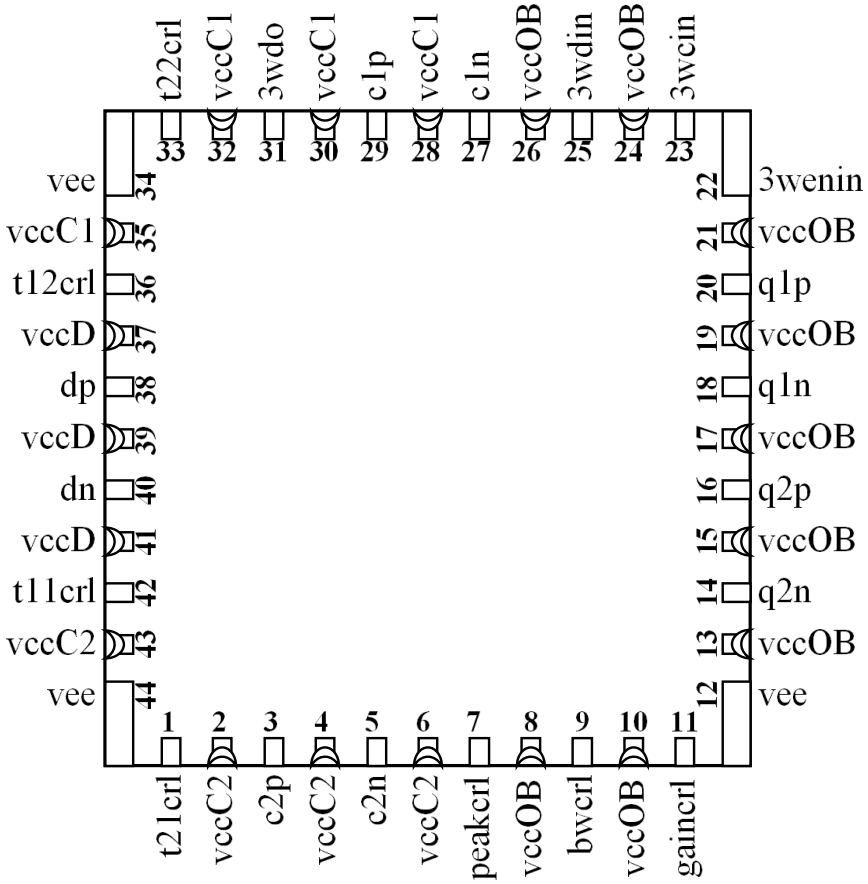
ASNT7114-KHM
6*GSps* / 32*GHz* Differential Track-and-Hold Splitter Amplifier

- Single differential CML input splits into two individually-sampled differential CML outputs
- Dual independent differential CML sampling inputs
- More than 8-bit accuracy within the full frequency range
- Input bandwidth up to 32*GHz*
- Sampling speed up to 6*GSps*
- Nominal 0*dB* differential gain with manual adjustment
- Individually-adjustable duty cycles and delays of the internal sampling clocks
- Adjustable input bandwidth and peaking
- Optional independent power supplies
- Adjustable power consumption from 1.5*W* to 2*W* for two channels
- External analog manual controls or SPI control
- Fabricated in SiGe for high performance, yield, and reliability
- Custom KHM 44-pin package



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DESCRIPTION

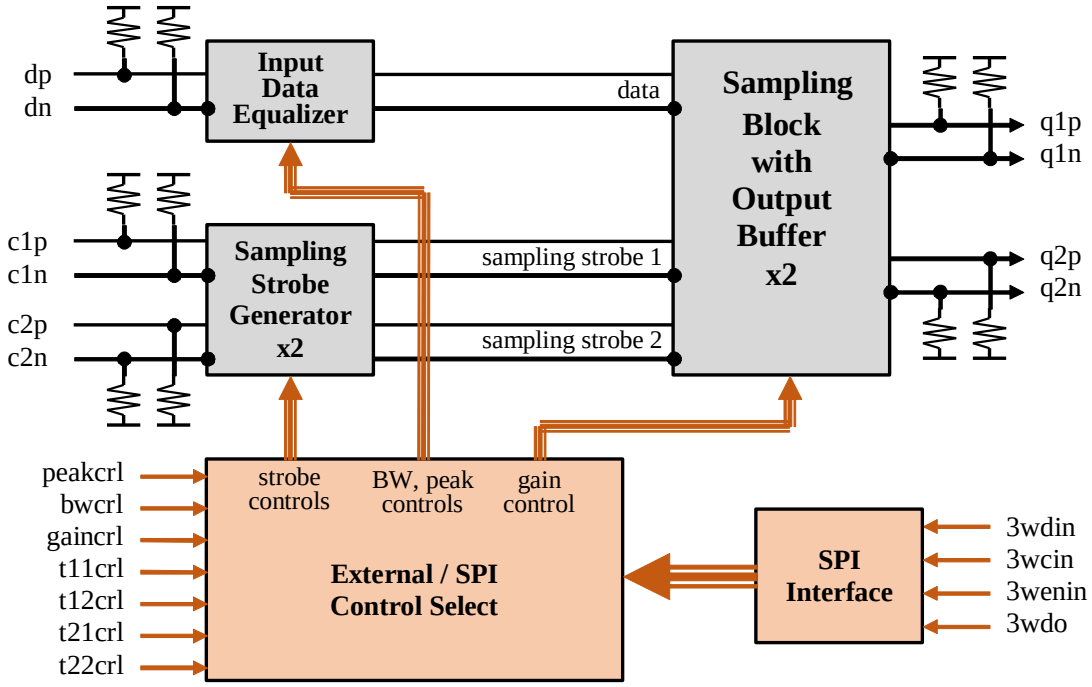

Fig. 1. Functional Block Diagram

The ASNT7114 SiGe IC is a high-speed, temperature-stable, and broadband dual-channel track-and-hold amplifier (THA). The IC shown in Fig. 1 performs sampling of the input differential analog signal dp/dn using two pairs of internally-generated strobe signals s11/s12 and s21/s22, and delivers two independent step-like differential signals q1p/q1n and q2p/q2n to the output. It features an adjustable track period length controlled by two external voltages t11crl/t12crl and t21crl/t22crl that modify the states of internal delay lines, which allows for maximizing the length of the "hold" time.

The differential gain of the chip is approximately 0*dB*, which corresponds to a single-ended-to-differential gain of -6*dB*. The gain can be adjusted using the external control voltage gaincrl. The chip supports both AC-coupled and DC-coupled inputs. In the DC-coupled mode, the input common-mode voltage must be equal to vcc for optimal performance of the chip. The input sampled data path includes an equalizer that increases the bandwidth of the chip. The level of equalization is controlled by the external voltage peakcrl. The power consumption, bandwidth and extra peaking of the input path can be adjusted via the external voltage bwcrl.

The chip may be controlled through a 3-wire SPI interface via a GUI provided by ADSANTEC. The GUI features all of the above-mentioned external controls, as well as the independent adjustment of power consumption of each element, the ability to turn off either one or both sampling channels, and independent channel peaking and gain controls. The SPI is turned off by default.

The part's inputs and outputs support the CML-type logic interface with an on-chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). Differential DC signaling is recommended for optimal performance.

Input Data Equalizer

The bandwidth of the data input can be adjusted by the internal equalizer controlled with the external voltage peakcrl. The equalizer is designed to compensate for the gain drop at high frequencies due to the characteristics of the front-end circuitry and the sampling block itself. The simulated frequency response of the IC at maximum (orange line) and minimum (blue line) values of the peakcrl is shown in Fig. 2.

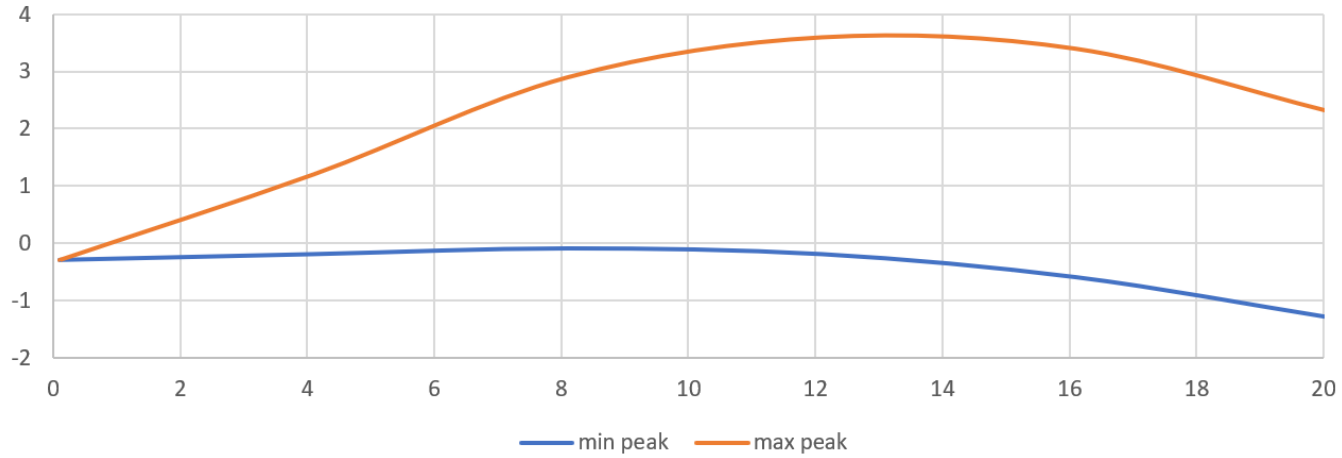

Fig. 2. Simulated Frequency Response of SHA with Max and Min Equalization

Input Clock Buffer

The input clock buffer converts the external clock c1p/c1n and c2p/c2n into two pairs of internal signals s11/s12 and s21/s22 with controlled pulse width (PW) and delay (τ) between them as shown in Fig. 3.

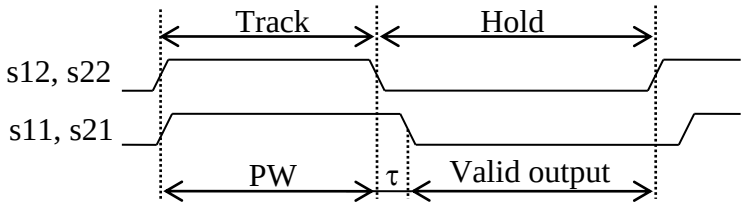

Fig. 3. Sampling Diagram

This allows for optimization of the hold time and the length of the valid output signal period. The value of PW is reverse-proportional to the t21crl/t22crl voltage, while the value of τ is proportional to the t11crl/t12crl voltage.

Sampling Block and Output Buffer

The sampling block performs conversion of the input signal into a step-like sampled signal under control of the s11/s12 and s21/s22 pulses. The sampled signal is amplified by the output buffer to achieve a total gain of approximately 0*dB*. The gain can be adjusted using the gaincrl voltage signal.

The harmonic distortion of the THA has been demonstrated by 2nd and 3rd harmonics as shown in Fig. 4 for single-ended clock input and differential data input signals at the sampling rate of 4*GSps*. The data amplitude is 125*mV* differential or 125*mV* pk-pk at both direct and inverted pins.

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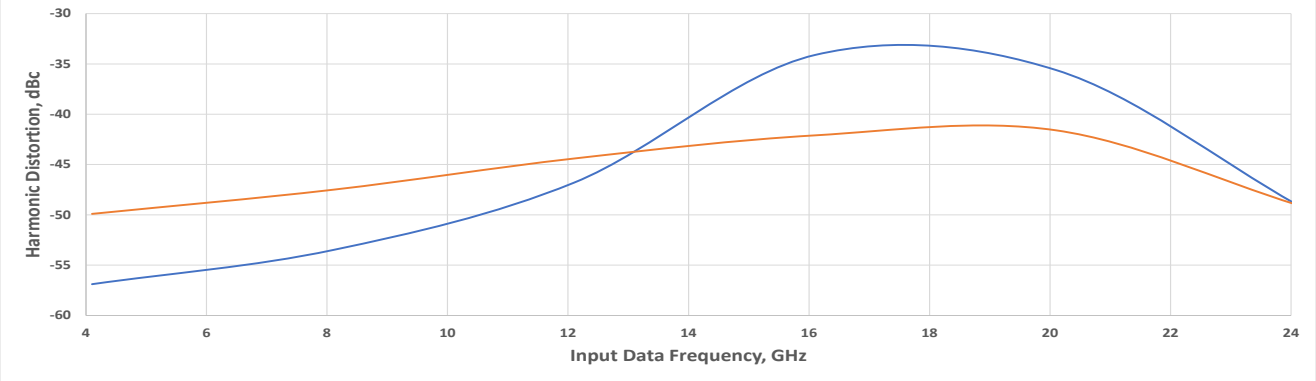

Fig. 4. 2nd (blue) and 3rd (orange) Harmonic Distortions at 4GHz Clock and 125mV Differential Data Amplitude

The linearity of the signal conversion is illustrated by Fig. 5 that demonstrates the part's gain at 4*GSps*.

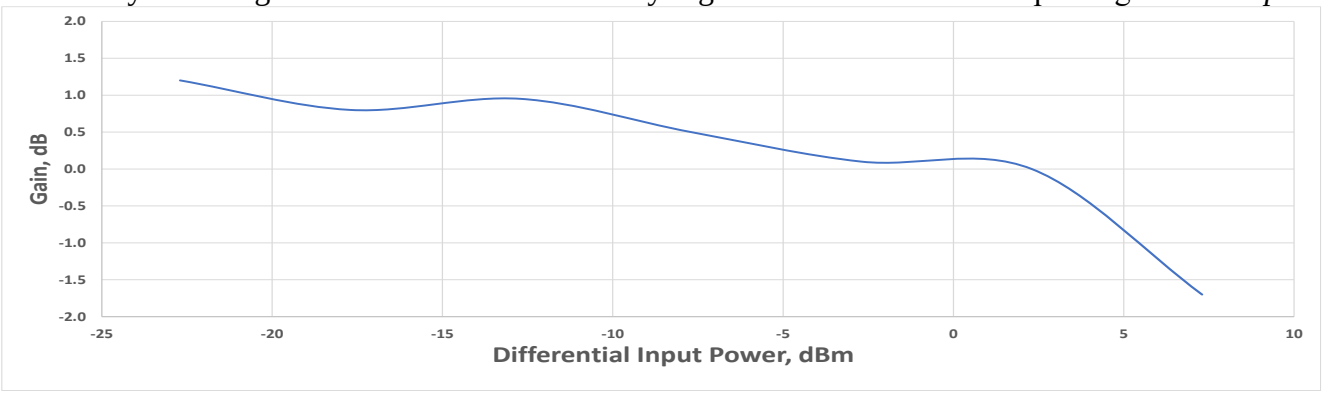

Fig. 5. THA Gain vs. Input Data Amplitude at Medium State of gaincrl

SPI Block

The SPI block provides digital controls through a 1.2*V* CMOS 3-wire interface with all voltage levels referenced to vee. The SPI is loaded by 11 bytes. All bytes have default values that are indicated in Table 1. DAC blocks convert digital controls of SPI into analog control signals for analog adjustment of internal voltage controls. Table 1 presents SPI byte order and their default settings that are shown in parentheses.

Table 1. Control Bytes

Byte Number	Bit Number							
	7	6	5	4	3	2	1	0
1	g1 (“1000000”)							ch1off (“0”)
2	g2 (“1000000”)							ch2off (“0”)
3	pk1c (“10000000”)							
4	pk2c (“10000000”)							
5	ief0c (“10000000”)							
6	ief1c (“10000000”)							
7	ief2c (“10000000”)							
8	t11c (“10000000”)							
9	t21c (“10000000”)							
10	t12c (“10000000”)							
11	t22c (“10000000”)							

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Table 2 presents a description of the SPI controls.

Table 2. Digital Control Description

Signal Name	# of bits	Description
ch1off	1	Turns off channel 1
ch2off	1	Turns off channel 2
g1	7	Controls the gain of channel 1
g2	7	Controls the gain of channel 2
pk1c	8	Controls equalizer peaking in channel 1
pk2c	8	Controls equalizer peaking in channel 2
ief0c	8	Controls bandwidth and power consumption in both channels
ief1c	8	Controls bandwidth and power consumption in channel 1
ief2c	8	Controls bandwidth and power consumption in channel 2
t11c	8	Controls the delay between two sampling clocks in channel 1
t21c	8	Controls the hold vs. track times in channel 1
t12c	8	Controls the delay between two sampling clocks in channel 2
t22c	8	Controls the hold vs. track times in channel 2

POWER SUPPLY CONFIGURATION

The part features four independent positive supply nets (vccD, vccC1, vccC2, vccOB) and can operate with either a negative supply scheme (all four vcc = 0.0*V* = ground) or a positive supply scheme (vee = 0*V* = ground). In case of the positive supply, all vcc may be powered independently to minimize the noise injection and all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume the negative supply scheme.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
First Supply Voltage (vee)	-3.5 (negative scheme)	0 (positive scheme)	*V*
Second Supply Voltage (vcc)	0 (negative scheme)	3.5 (positive scheme)	*V*
Power Consumption		2	*W*
RF Input Voltage Swing (Diff)		2.0	*V* pk-pk
Clock Input Voltage Swing (Diff)		1.0	*V* pk-pk
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational and storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
c1p	29	CML input	Sampling clock #1 inputs with internal SE 50*Ohm* termination to vccC1
c1n	27		
c2p	3		Sampling clock #2 inputs with internal SE 50*Ohm* termination to vccC2
c2n	5		
dp	38	Analog input	Analog sampled data inputs with internal SE 50*Ohm* termination to vccD
dn	40		
q1p	20	CML output	Differential data outputs #1 with internal SE 50*Ohm* termination to vccOB. Require external SE 50*Ohm* termination to vcc
q1n	18		
q2p	16		Differential data outputs #2 with internal SE 50*Ohm* termination to vccOB. Require external SE 50*Ohm* termination to vcc
q2n	14		
Controls			
t11crl	42	Analog voltage	Sampling clock #1 duty cycle control
t12crl	36	Analog voltage	Sampling clock #1 delay control
t21crl	1	Analog voltage	Sampling clock #2 duty cycle control
t22crl	33	Analog voltage	Sampling clock #2 delay control
gaincrl	11	Analog voltage	Gain adjustment
peakcrl	7	Analog voltage	Equalizer peaking control
bwcrl	9	Analog voltage	Bandwidth and current consumption control
Low-Speed I/Os			
3wenin	22	1.2*V* CMOS input referenced to vee	Enable input signal for SPI
3wcin	23		Clock input signal for SPI
3wdin	25		Data input signal for SPI
3wdo	31	1.2*V* CMOS output referenced to vee	Data output signal of SPI

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vccC2	Clock #2 supply voltage	2, 4, 6, 43
vccOB	Output buffer supply voltage	8, 10, 13, 15, 17, 19, 21, 24, 26
vccC1	Clock #1 supply voltage	28, 30, 32, 35
vccD	Data path supply voltage	37, 39, 41
vee	Negative power supply	12, 34, 44

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Input Data (dp, dn)					
Input data frequency	0.0		32	*GHz*	At nominal conditions
Swing, differential, p-p	0		200	*mV*	THD < TBD *dBc* in full data bandwidth
	0		600	*mV*	THD < TBD *dBc* in full data bandwidth
	0		1000	*mV*	THD < TBD *dBc* in full data bandwidth
CM Voltage Level		vcc		*V*	For DC coupling
S11		-10		*dB*	DC to 20*GHz*
Input Clock (cp, cn)					
Frequency	0.05		6.0	*GHz*	
Swing	80		400	*mV*	SE or differential, p-p
CM Voltage Level		vcc		*V*	
Jitter			50	*fs*	p-p
Duty cycle	48	50	52	*%*	
Duty Cycle Control Voltage (t11crl, t21crl)					
Voltage range	vcc – 1.3		vcc –0.3	*V*	
Adjustment range		50		*ps*	For the delay of s1 vs. s2
Delay Control Voltage (t12crl, t22crl)					
Voltage range	vcc – 1.3		vcc –0.3	*V*	
Adjustment range		20		*ps*	For the pulse width of s1 and s2
Bandwidth & Current Consumption Control Voltage (bwcrl)					
Voltage range	vcc – 1.8		vcc	*V*	
Adjustment range		50		*mA*	
Gain Control Voltage (gaincrl)					
Voltage range	vcc – 2.8		vcc –0.3	*V*	
Adjustment range		2		*dB*	
Equalizer Control Voltage (varcrl)					
Voltage range	vcc – 1.8		vcc	*V*	
Additional peaking		4.5		*dB*	At 20*GHz* and nominal conditions
HS Output Data (out)					
Ouput Swing			0.8	*V*	Differential, peak-peak
THD					See Fig. 4
Noise		TBD		$nV/Hz^{1/2}$	At 2.5*GSps* within full data BW
Track period length			250	*ps*	At 2.5*GSps*. Adjustable by t1crl
Total DC gain	-2		0	*dB*	Adjustable by gaincrl signal.
S22		-20		*dB*	DC to 4*GHz*
SPI I/Os (3wenin, 3wdin, 3wcin, 3wdo)					
Low logic level	vee		vee+0.2	*V*	
High logic level	vee+1.0		vee+1.3	*V*	

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.5 / 0	-3.3 / 0	-3.1 / 0	*V*	Negative scheme / Positive scheme
All vcc##	0 / 3.1	0 / 3.3	0 / 3.5	*V*	Negative scheme / Positive scheme
IvccC1		160		*mA*	
IvccC2		160		*mA*	
IvccD	40		120	*mA*	
IvccOB	265		280	*mA*	
*I*vee	500		600	*mA*	
Power consumption	1.5		2.0	*W*	
Junction temperature	-25	50	125	*°C*	

PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFN package shown in Fig. 6. The package provides a center heat slug located on the back side of the package to be used for heat dissipation. ADSANTEC recommends using extreme caution when soldering this section to the board to avoid overheating. It should be connected to the vcc plain that is ground for the negative supply, or power for the positive supply.

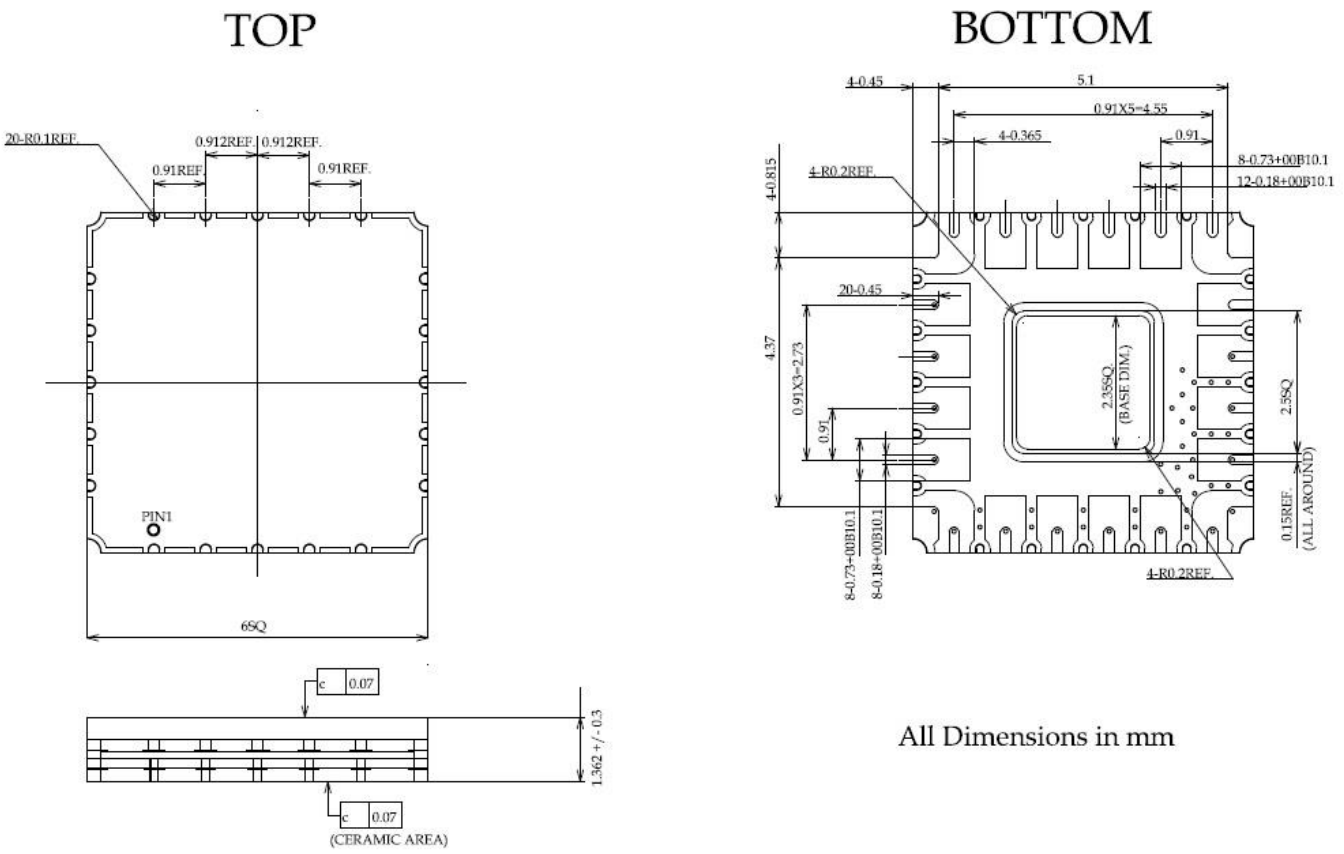

Fig. 6. CQFN44 Package Drawing (All Dimensions in mm)

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The part's identification label is ASNT7114-KHM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.6.2	02-2025	Updated SPI information Added more detailed description of the four positive supply nets
1.5.2	04-2023	Updated format
1.4.2	03-2023	Updated Package Drawing
1.3.2	03-2023	Updated Package Drawing
1.2.2	02-2022	Updated Input Data Bandwidth
1.1.2	10-2021	Updated parameters, added header/footer, updated text
1.0.2	07-2021	First release