ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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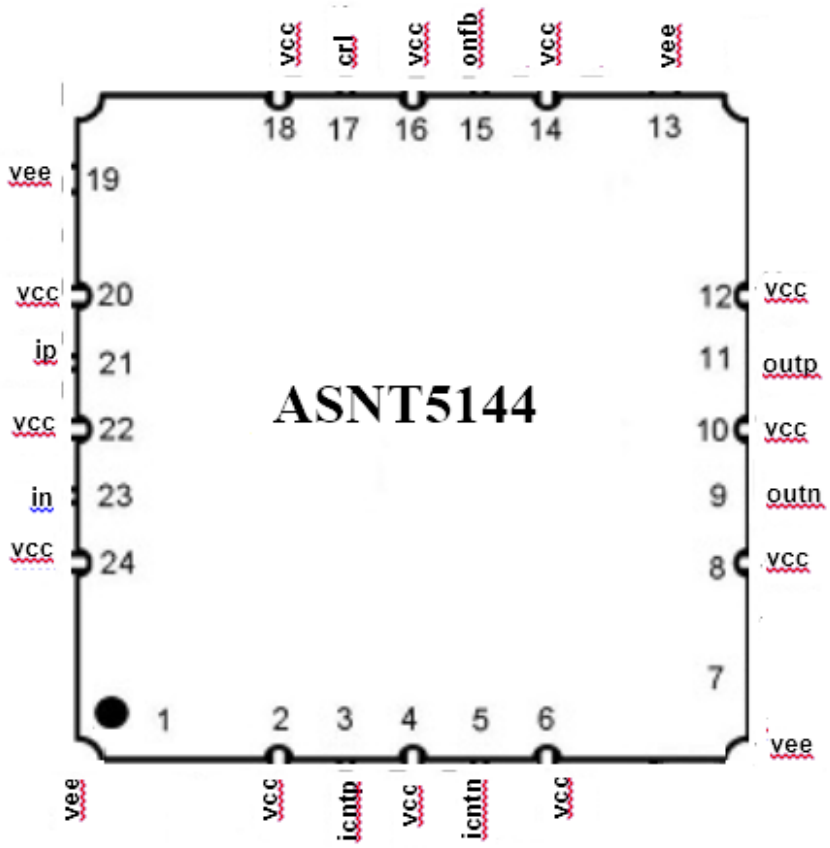
ASNT5144-KHC
8-35*GHz* Automatic Frequency Doubler

- High-speed frequency doubler with automatic output duty cycle correction.
- Output duty cycle always 50% with internal feedback turned on.
- Manual output duty cycle control available.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- Ideal for high speed proof-of-concept prototyping.
- Fully differential CML input interfaces.
- Fully differential CML output interface with 600*mV* single-ended swing.
- Single +3.3*V* or -3.3*V* power supply.
- Power consumption: 660*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFN 24-pin package



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DESCRIPTION

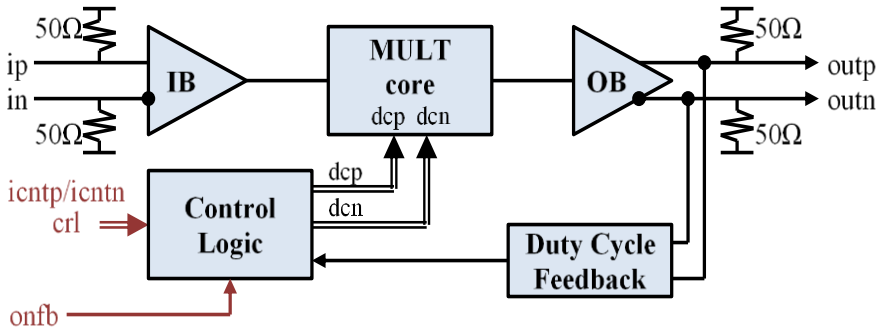

Fig. 1. Functional Block Diagram

The temperature stable ASNT5144-KHC SiGe IC provides broadband frequency multiplication, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can receive a high-speed clock input signal ip/in, and deliver a high-speed double-frequency clock output signal outp/outn. There are two duty cycle correction feedback loops. The first loop adjusts the duty cycle of the input signal, and the second loop controls the final output signal duty cycle. Activation of the loops is controlled via the onfb control port as shown in Table 1.

Table 1. Feedback Loops Activation by onfb

fbon	Input FB loop	Output FB loop
vee	off	off
vcc	off	on
not connected (nc)	on	on

When both feedback loops are activated, the output clock's duty cycle is automatically kept at about 50%. To ensure correct operation of the feedback block within a wide range of frequencies, the optional control port crl can be set to vee/vcc/nc according to Table 2. The duty cycle may also be adjusted manually via tuning ports icntp/icntn when feedback is turned off.

Table 2. Frequency Ranges at crl settings

crl	Frequency Range (GHz)
vee	4.3 - 12.9
vcc	6.6 - 19.7
not connected (nc)	13 - 38.9

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc, and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

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POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 3. Absolute Maximum Ratings.

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Supply current		200	*mA*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
ip	21	CML input	Differential clock inputs with internal SE 50*Ohm* termination to vcc.
in	23		
outp	11	CML output	Differential clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc.
outn	9		
onfb	15	3.3V CMOS	Digital Control Signal with 6.6*KOhm* termination to vee
crl	17	3.3V CMOS	3-State Digital Control Signal with 4.6*KOhm* termination to vee and 6.6*KOhm* termination to vcc
icntp	3	CML input	Differential tuning ports with internal 100*Ohm* termination to vcc.
icntn	5		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply. (+3.3*V* or 0)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply. (0*V* or -3.3*V*)		1, 7, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		200		*mA*	
Power consumption		660		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Clock (ip/in)					
Frequency	4		17.5	*GHz*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Clock (outp/outn)					
Frequency	8		35	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.6		*V*	With external 50*Ohm* DC termination
Rise/Fall times	6	8	10	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak
Duty cycle		50		*%*	For clock signal with feedback on
CMOS Control Ports (onfb, crl)					
onfb	0		3.3	*V*	See Table 1
crl	0	nc	3.3	*V*	See Table 2
Tuning Ports (icntp/icntn)					
Bandwidth	DC		100	*MHz*	
Swing		vcc-0.4		*V*	Differential
CM Voltage Level	vcc-0.4		vcc	*V*	Must match for both inputs

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PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFN package shown in **Error! Reference source not found.**. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

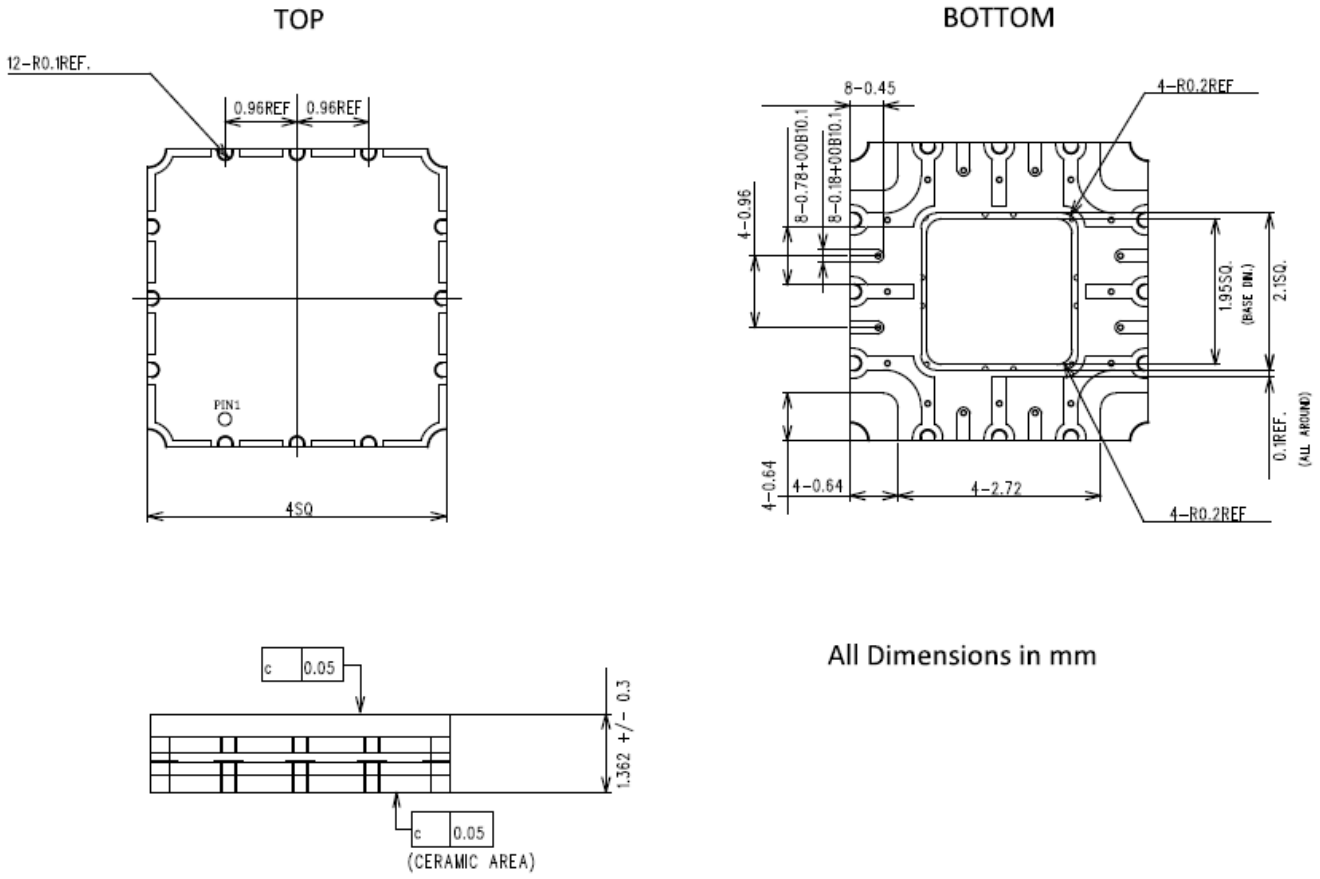

Fig. 2. CQFN 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT5144-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
1.0.3	04-2023	Updated Package Drawing
1.0.2	04-2021	First release