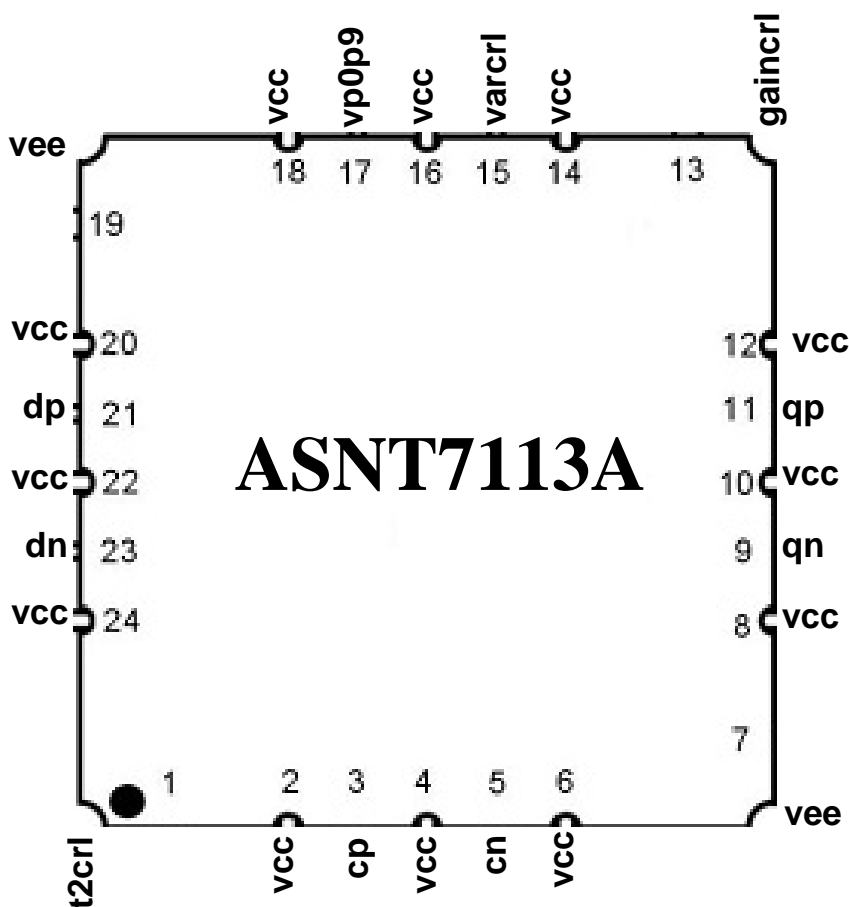




## ASNT7113A-KHC

### 4.0GSps / 20GHz Differential Track-and-Hold Amplifier

- More than 8-bit accuracy within the full frequency range
- Sampling speed from 50MSps to 4GSps
- Nominal 0dB differential gain with manual adjustment
- Adjustable duty cycle of the internal sampling clocks
- Adjustable input bandwidth
- Adjustable overall gain
- Fully differential input and output data and clock buffers with on-chip 50Ohm termination
- Dual power supply
- Total power consumption of 1.75W
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFN 24-pin package



## DESCRIPTION

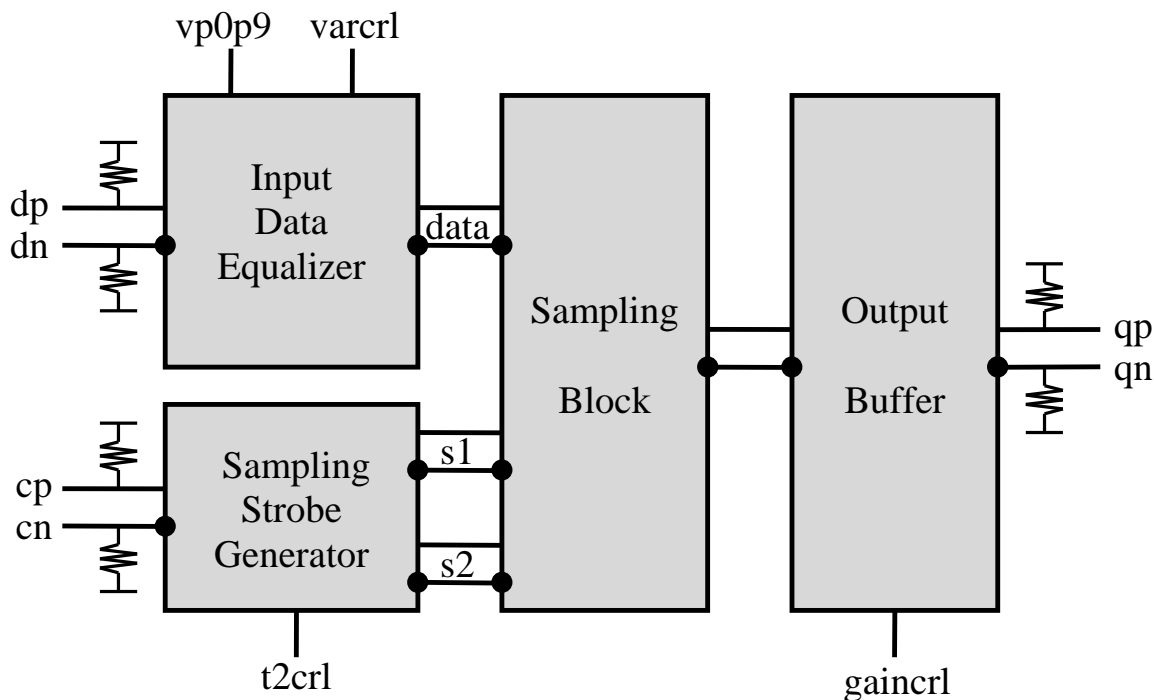


Fig. 1. Functional Block Diagram

The ASNT7113A-KHC SiGe IC is a high-speed, temperature stable, and broadband track-and-hold amplifier (THA) with improved reliability. The IC shown in Fig. 1 performs sampling of an input differential analog signal using two internally-generated strobe signals **s1** and **s2**, and delivers a step-like differential signal to the output. It features an adjustable track period length controlled by the **t2crl** voltage that modifies the states of internal delay lines. This allows for maximizing the length of the valid output step.

The differential gain of the chip is approximately  $0dB$ , which corresponds to a single-ended-to-differential gain of  $-6dB$ . The gain can be adjusted using the external control voltage **gaincrl**. The chip supports both AC-coupled, and DC-coupled inputs. In the DC-coupled mode, the input common-mode voltage must be equal to **VCC** for optimal performance of the chip. The input sampled data path includes an equalizer that increases the bandwidth of the chip. The level of equalization is controlled by the external voltage **varcrl**.

The frequency response, and gain of the part is also controlled by the positive supply voltage **vp0p9** that powers the input buffers of the Track-and-Hold. This voltage defines the common mode of the data signal at the input of the sampling switch, and thus the frequency response of the device. Lower voltages result in less peaking in the input buffer, and less overall gain of the device.

The part's outputs support the CML-type logic interface with an on-chip  $50\Omega$  termination to **VCC**, and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). The differential DC signaling mode is recommended for optimal performance.

## Input Data Equalizer

The input data's bandwidth can be adjusted by the internal equalizer controlled with the external voltage `varcrl`. The equalizer is designed to compensate for the gain drop at high frequencies due to the characteristics of the front-end circuitry, and the sampling block itself. The measured frequency response of the IC at maximum (magenta line) and minimum (orange line) values of the `varcrl` voltage is shown in Fig. 2. The measurements have been performed at the intermediate setting of the gain control (see Fig. 4).

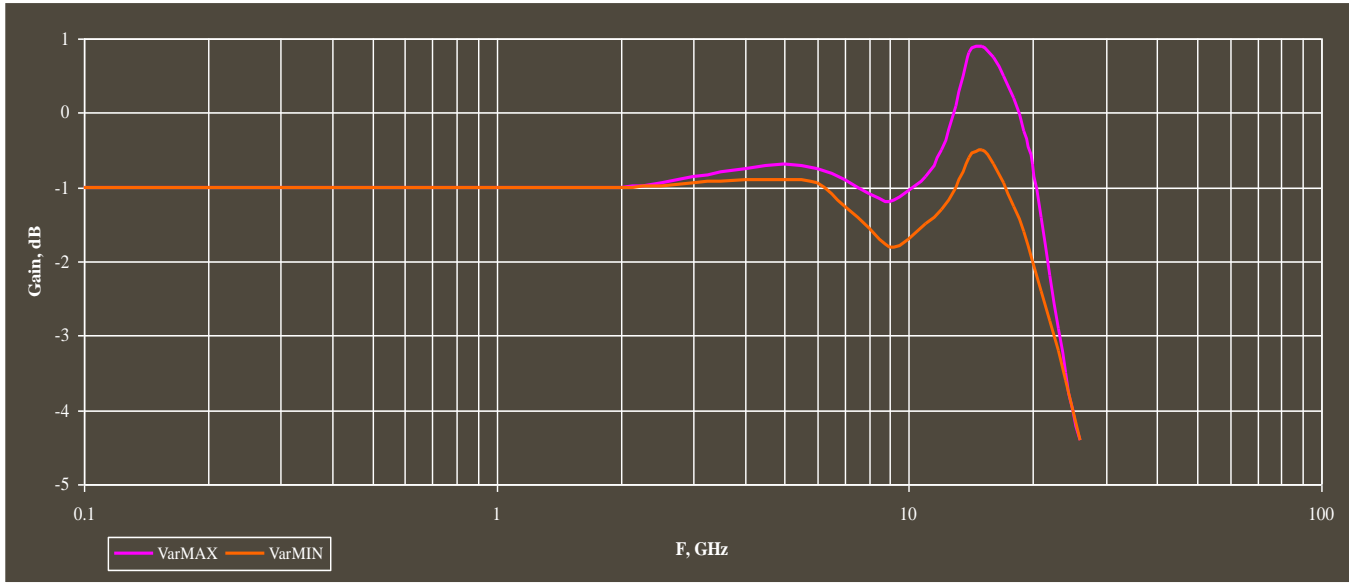


Fig. 2. Frequency Response of SHA with Max and Min Equalization

## Input Clock Buffer

The input clock buffer converts an external clock `cp/cn` into two internal signals `s1` and `s2` with controlled pulse width (PW) as shown in Fig. 3.

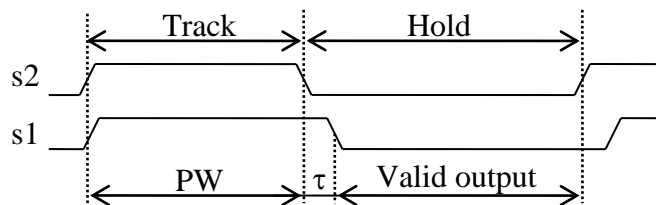


Fig. 3. Sampling Diagram

This allows for optimization of the hold time, and the length of the valid output signal period. The value of PW is reversely proportional to the `t2crl` voltage.

## Sampling Block with Output Buffer

The sampling block performs conversion of the input signal into a step-like sampled signal under control of `s1` and `s2` pulses. The sampled signal is amplified by the output buffer to achieve a total gain of approximately 0dB. The gain can be adjusted using the `gaincrl` voltage signal. The measured frequency response of the SHA with the maximum and minimum gain at 2.5GSps rate is shown in Fig. 4.

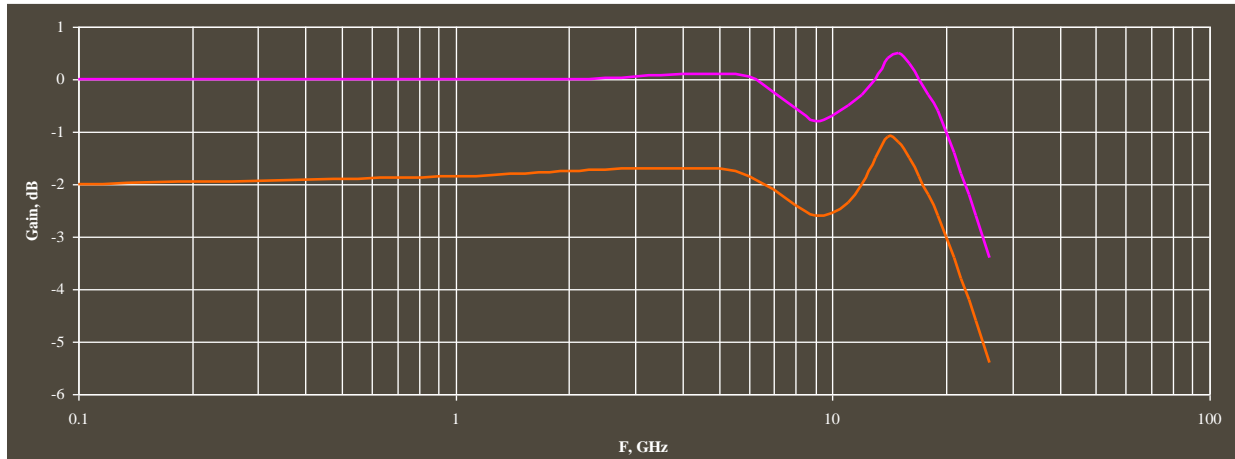


Fig. 4. THA Gain at Max and Min gaincr1 Values vs. Data Frequency

The harmonic distortion of the THA has been demonstrated by its 3<sup>rd</sup> harmonic as shown in Fig. 5 for differential clock, and data input signals at the sampling rate of 4GSps. The data amplitude is 125mV differential or 125mV pk-pk at both direct and inverted pins.

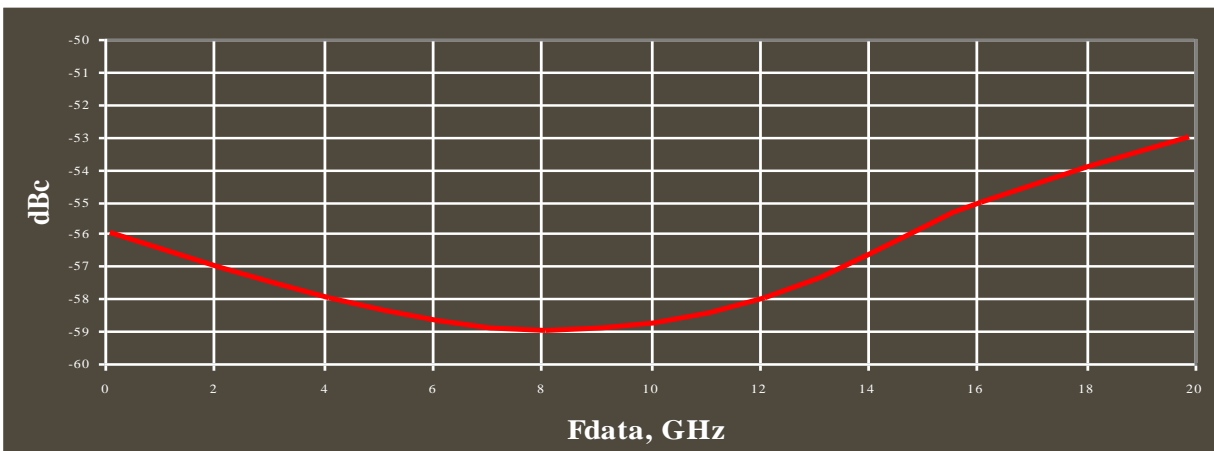


Fig. 5. 3-rd Harmonic at 4GHz Input Clock (C) and 125mV Differential Data (D) Amplitude

The linearity of the signal conversion is illustrated by Fig. 6 that demonstrates the part's gain at 2.5GSps.

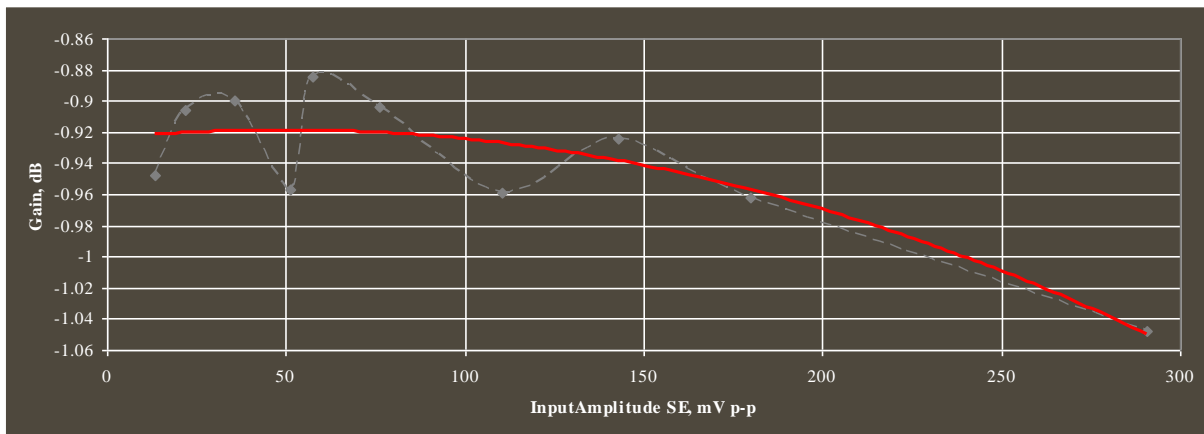


Fig. 6. THA Gain vs. Input Data Amplitude at Medium State of gaincr1



## POWER SUPPLY CONFIGURATION

The part operates with either a negative supply scheme ( $v_{cc} = 0.0V = \text{ground}$ ), or a positive supply scheme ( $v_{ee} = 0V = \text{ground}$ ). In case of the positive supply, all I/Os need AC termination when connected to any devices with  $50\Omega$  termination to ground. Different PCB layouts will be needed for each different power supply combination.

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
First Supply Voltage ( $v_{ee}$ )	-3.5 (negative scheme)	0 (positive scheme)	V
Second Supply Voltage ( $v_{cc}$ )	0 (negative scheme)	3.5 (positive scheme)	V
Third Supply Voltage ( $v_{p0p9}$ )		$v_{cc}+1.1$	V
Power Consumption		2	W
RF Input Voltage Swing (Diff)		2.0	V pk-pk
Clock Input Voltage Swing (Diff)		1.0	V pk-pk
Case Temperature		+90	$^{\circ}C$
Storage Temperature	-40	+100	$^{\circ}C$
Operational and storage Humidity	10	98	%

## TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
<b>High-Speed I/Os</b>			
cp	3	CML input	Sampling clock inputs with internal SE $50\Omega$ termination to $v_{cc}$
cn	5		
dp	21	Analog input	Analog sampled data inputs with internal SE $50\Omega$ termination to $v_{cc}$
dn	23		
qp	11	CML output	Differential data outputs with internal SE $50\Omega$ termination to $v_{cc}$ . Require external SE $50\Omega$ termination to $v_{cc}$
qn	9		
<b>Controls</b>			
t2crl	1	Analog voltage	Sampling clock delay control
gainerl	13	Analog voltage	Gain adjustment
varcrl	15	Analog voltage	Equalizer peaking control
<b>Supply and Termination Voltages</b>			
Name	Description		Pin Number
vcc	1 <sup>st</sup> positive supply voltage		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply		7, 19
vp0p9	2 <sup>nd</sup> positive power supply		17



## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee	-3.3 / 0	-3.2 / 0	-3.1 / 0	V	Negative scheme / Positive scheme
vcc	0 / 3.1	0 / 3.2	0 / 3.3	V	Negative scheme / Positive scheme
vp0p9	0.75	0.85	0.95	V	Above vcc, any scheme
Ivcc		430		mA	Ivee = Ivcc + Ivp0p9
Ivp0p9		100		mA	
Power consumption		1750		mW	
Junction temperature	-25	50	125	°C	
<b>Input Data (dp/dn)</b>					
Input data frequency	0.0		20	GHz	
Swing, differential, p-p	0		300	mV	3 <sup>rd</sup> HD < -52dBc in full data bandwidth
	0		400	mV	3 <sup>rd</sup> HD < -48dBc in full data bandwidth
	0		500	mV	3 <sup>rd</sup> HD < -45dBc in full data bandwidth
CM Voltage Level		vcc		V	For DC coupling
S11		-10		dB	DC to 20GHz
<b>Input Clock (cp/cn)</b>					
Frequency	0.05		4.0	GHz	
Swing	80		240	mV	SE or differential, p-p
CM Voltage Level		vcc		V	
Jitter			50	fs	p-p
Duty cycle	45	50	55	%	Lower variation recommended
<b>Delay Control Voltage (t2crl)</b>					
Voltage range	vcc - 1.4		vcc	V	
Adjustment range		20		ps	For the pulse width of s1 and s2
<b>Gain Control Voltage (gaincrl)</b>					
Voltage range	vcc - 1.8		vcc	V	
<b>Equalizer Control Voltage (varcrl)</b>					
Voltage range	vcc - 1.8		vcc	V	
Additional peaking		1.5		dB	At 20GHz and nominal conditions
<b>Input Data Common Mode Control (vp0p9)</b>					
Voltage Range	vcc + 0.7		vcc + 0.9	V	
<b>HS Output Data (qp/qn)</b>					
CM Level		vcc-0.4		V	
3 <sup>rd</sup> HD					See Fig. 5
Noise		12		nV/Hz <sup>1/2</sup>	At 2.5GSps within full data bandwidth
Track period length			250	ps	At 2.5GSps
Total DC gain	-2.1		0.1	dB	Adjustable by gaincrl signal
S22		-20		dB	DC to 4GHz

## PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 7. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

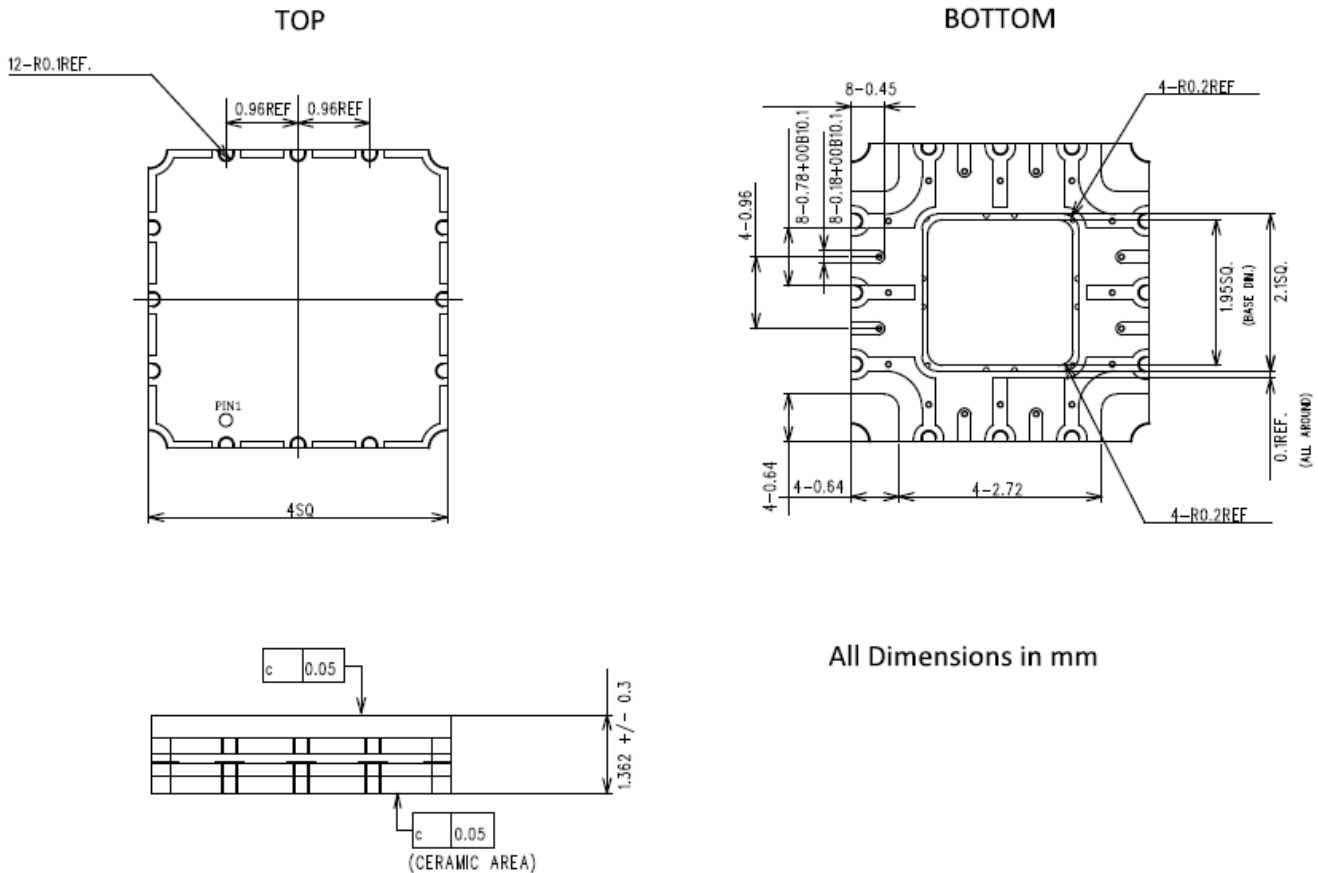


Fig. 7. CQFP 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT7113A-KHC. The first 9 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.



## REVISION HISTORY

Revision	Date	Changes
1.0.3	04-2023	Updated Package Drawing
1.0.2	03-2021	First release