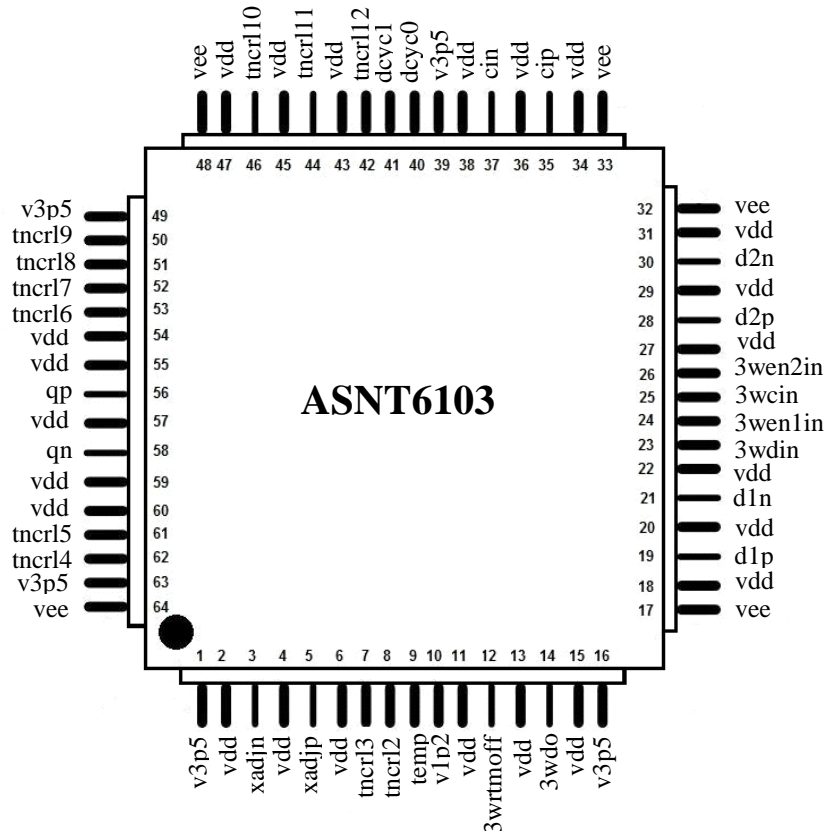




## ASNT6103-KMF 72Gbps-36Gbaud PAM4 Signal Generator/Encoder

- High-speed two input binary data signals to one PAM4 output signal
- Four pre-emphasis taps for each of 2 data channels with controlled weight and inversion
- Adjustable data output amplitude for all 3 levels and eye quality control
- Single-ended output data eye cross point adjustment
- All analog controls are compatible with PCI express standards
- Optional clock frequency multiplier by 2
- Main clock duty cycle indicators located before and after the multiplier
- Opposite and parallel adjustment of the main clock and data delays
- Fully differential CML input and output data, and input clock interfaces
- High-speed CML 3-wire interface for digital controls
- On-chip linear temperature sensor
- Two power supplies: negative -4.3V, floating positive +3.5V
- Maximum power consumption: 4.0W
- Power consumption depends on amplitude settings
- External high-speed analog amplitude controls
- Custom CQFP 64-pin package





## DESCRIPTION

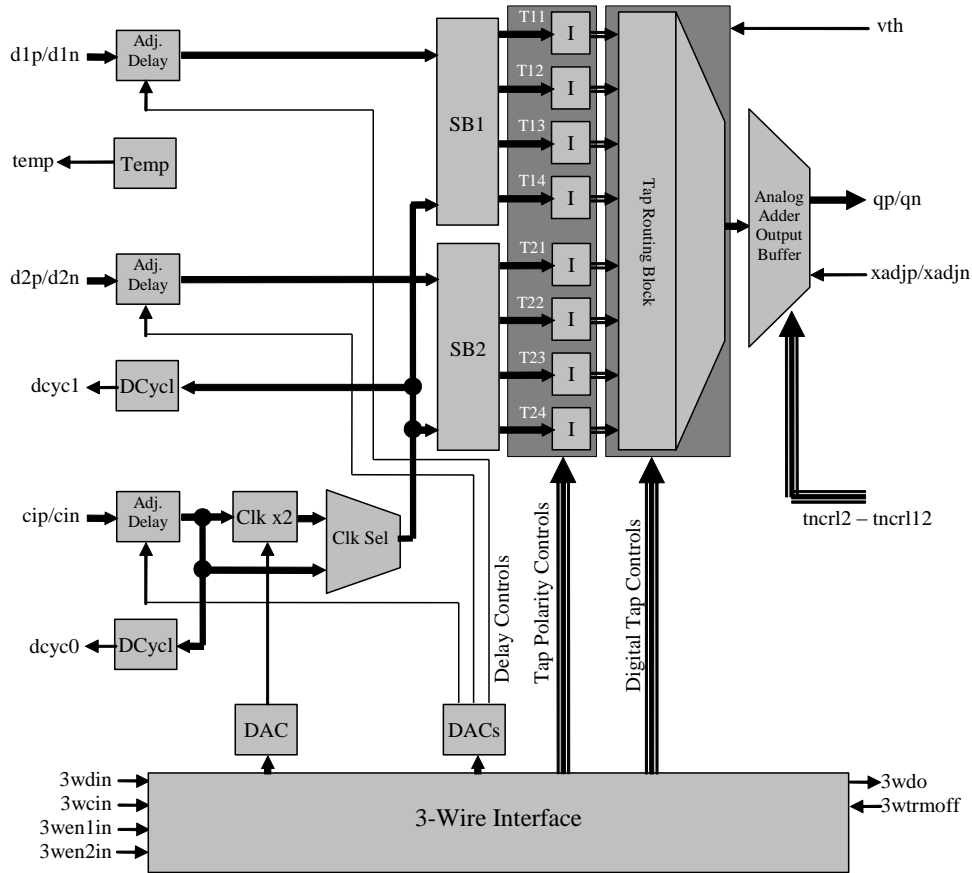


Fig. 1. Functional Block Diagram

The ASNT6103-KMF SiGe IC shown in Fig. 1 is a PAM4 encoder with built-in 4-tap pre-emphasis in each of the two input data channels. Each of the two differential input NRZ data streams is processed by a 4-tap shift register. Both 4-bit shift registers are activated by the same internal high-speed clock signal. As a result, the two registers provide 8 delayed copies of the two data input signals d1p/d1n (MSB Signal) and d2p/d2n (LSB Signal). These copies are combined together with certain user-defined weights and polarities, and are added together. The resulting differential analog data output data is sent to the output port qp/qn. In order to get a PAM4 signal at the output, the combined tap weight of the MSB signal should be two times greater than the combined tap weight of the LSB signal. For more information see **Sampling Block and Taps**, and **Data Output Buffer**.

All internal analog control signals, with the exception of the eye crossing adjustment signal xadjp/xadjn and eleven output amplitude controls tncr12 through tncr12, are generated with 8-bit or 12-bit digital-to-analog converter (DAC) blocks. Digital inputs of these DAC blocks are provided by a 3-wire serial interface (SPI) block. All operational modes of the chip are controlled through the SPI block. The SPI block is split into two sections. Each section of digital controls may be accessed independently via two separate control signals. The SPI block is powered by an internally generated supply voltage of +1.2V from vee. For more details see **3-Wire Interface Control Block**.



The internal clock signal that latches data in the sampling blocks is a copy of the input clock signal `cip/cin` with either matching, or doubled (multiplied-by-2) frequency. In the multiply-by-2 clock mode, the duty cycles of the input, and internal clock signals are monitored, and the output duty cycle can be adjusted through a designated control (see **Clock Multiplier**). For the part's correct operation, the input data rate in *Gbps* should be equal to the internal clock frequency in *GHz*.

Input clock, and two data signals can be delayed independently by three control signals to ensure their correct phase relation at the inputs of the shift registers, and at the chip outputs (see **Input Delay Section**).

The part's I/Os support CML logic interface with on-chip *50Ohm* termination to ground. External *50Ohm* termination is also required. DC-coupling for data, and clock output ports is strongly recommended. The input ports can use DC, or AC coupling. Differential connections of input clock, and data are strongly recommended. Amplitude and peaking in the data output signal can be adjusted. Both single-ended data output signals also have controlled eye crossing points (see **Data Output Buffer**).

The chip operates from one negative power supply (positive pin connected to external Ground,) and one floating positive power supply (negative pin connected to `vee` and positive pin `v3p5 = 3.5V`). It is recommended to keep the relative deviation of `v3p5` from Ground within less than  $\pm 0.1V$ . The additional supply voltage for internal CMOS circuitry is generated inside the chip, or may be applied externally to the pin `v1p2`.

## Input Delay Section

As shown in Fig. 1, the encoder accepts two differential input data signals `d1p/d1n` and `d2p/d2n` as well as the input clock signal `cip/cin`. The signals go through identical adjustable delay blocks `Adj. Delay`. Phase shifts of the three blocks are controlled independently by three digital bytes `skwadj1`, `skwadj2`, and `skwadjc` of the 3-wire interface block. The signals `skwadj1`, `skwadj2`, and `skwadjc` control the delays of the signals `d1p/d1n`, `d2p/d2n`, and `cip/cin` respectively.

## Clock Multiplier

The clock multiplier `Clkx2` uses a "delay and XOR" mechanism to create output clock pulses from each edge of the input clock `cip/cin`. The multiplier is intended for operation with input clock signals within a certain frequency range specified in ELECTRICAL CHARACTERISTICS. A 12-bit digital signal `ckdbradj` performs a dual function of multiplier activation, and linear phase control. Voltages within the linear control range activate the multiplication function, and are used for tuning the block's internal delay in order to achieve 50% duty cycle of the multiplied clock. The clock multiplier block may be turned off with the differential digital signal `byp/byn`. In order for the multiplier to turn off, `byp` bit should have the value of 1, and the `byn` bit should have the value of 0. When the clock multiplier is off, the delayed version of the input clock signal `cip/cin` is delivered to the sampling block with an unaltered frequency, and an unaltered duty cycle. The opposite states of the `byp/byn` controls turn the multiplier on.

Two duty cycle control blocks `DCycl` are used for monitoring the clock pulse shapes before, and after the multiplier. The first block is positioned before the multiplier, and delivers single-ended analog voltage `dcyc0` that indicates the input clock's duty cycle deviation from 50%. The second block is positioned after the multiplier, and delivers a similar signal `dcyc1` for the output clock. Both generated output

voltages can be used in combination with the `ckdbradj` input within external control loops for getting an optimal shape of the multiplied clock.

### ***Sampling Block and Taps***

Sampling blocks SB1 and SB2 are 4-bit shift registers that generate 8 delayed data streams. The data streams T11, T12, T13, and T14 are the delayed versions of the input data signal `d1p/d1n`, MSB data. Similarly, the data streams T21, T22, T23, and T24 are the delayed versions of the input data signal `d2p/d2n`, LSB data. The delays between versions of the input signals are equal to one period of the original or doubled clock. These data streams are needed for the 4-tap pre-emphasis capability. As stated above, the control bytes `skwadj1`, `skwadj2`, and `skadjc` are used to adjust the phase relationship between clock and data signals to ensure optimum sampling in both sampling blocks. The eight samples of the data streams with certain weights and polarities are delivered to the output, and combined into a single analog differential output signal. The polarities of the data streams can be independently inverted with the digital control byte `tapinv` (“0”=direct, “1”=inverted) provided by the 3-wire interface.

### ***Data Output Buffer***

The 8 data streams from SB1 and SB2 are distributed among 12 identical parallel channels. Data is delivered through these channels to the output buffer. The output buffer consists of 12 identical open-collector buffers that deliver currents to two 50-*Ohm* resistors at the output. The resulting differential voltage on these resistors at the output of the chip represents a linear summation of all the taps. Twelve digital controls `ochoff<1>` through `ochoff<12>` can be used to turn any of the 12 channels on or off independently. If the control bit `ochoff<X>` has a value of 0, the channel X is on. If the control bit `ochoff<X>` has a value of 1, currents in two stages before the output stage are zero in channel X (where X is the number from 1 to 12), and the channel X does not pass data through. Shutting down unused channels before the output buffer stage reduces overall power consumption, and minimizes cross-talk between taps.

Digital controls `ochoff<1>` through `ochoff<12>` do not control currents in the 12 output buffers. The currents of the output buffers are linearly controlled through eleven external analog high-speed controls `tncl2` through `tncl12`. These controls can be used to independently adjust amplitudes of channels 2 through 12 from zero to maximum continuously. The time delay between control adjustment, and output buffer current settling does not exceed 200ns. Fig. 2 presents the simulated dependence of output buffer total current in any channel on the corresponding control voltage `tnclX` with respect to `vdd` where X is the number of the channel. In simulations `vdd` is at ground level (0.0V).

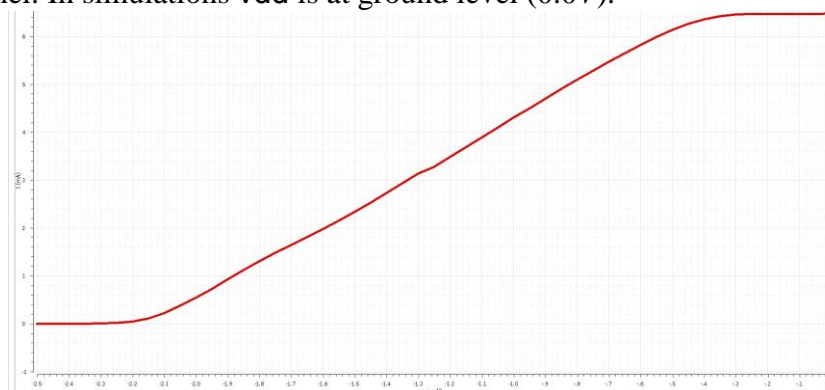


Fig. 2. Output Buffer Current of a Single Channel vs. Control Voltage `tncl`



The amplitude of the output buffer of channel 1 is always at maximum, and cannot be adjusted. The only way to reduce the amplitude of channel 1 is to completely turn it off by using **ochoff<1>** control.

As was mentioned earlier, 8 data streams (Tap11/12/13/14/21/22/23/24) from the sampling blocks are routed to twelve channel inputs of the output stage. After routing, data is retimed and is sent to the output stage. The input of channel 1 is hardwired to Tap12. Each input of the other 11 channels may receive 1 of 2 tap data streams. The routing combinations depend on user-defined settings of digital controls **ddr<2>** through **ddr<12>**. The control bit **ddr<X>** determines which data stream is routed to the input of channel X. Table 1 presents tap assignment to channels depending on **ddr<X>** settings.

Table 1. Tap Assignment to Channels

Channel	ddr<x>	
	0	1
2	Tap12	Tap11
3	Tap12	Tap11
4	Tap12	Tap13
5	Tap12	Tap13
6	Tap13	Tap11
7	Tap12	Tap14
8	Tap22	Tap21
9	Tap22	Tap23
10	Tap22	Tap23
11	Tap23	Tap21
12	Tap22	Tap24

Since the currents of the output stages of all the channels are added together, the maximum weight of each tap at the output is determined by digital control settings of controls **ddr<2>** through **ddr<12>** and **ochoff<1>**. Table 2 presents all valid pre-emphasis combinations of maximum tap weights for MSB data input **d1p/d1n** along with the corresponding digital control settings.

Table 2. Maximum Tap Weight Combinations for MSB Data Stream

Tap11	Tap12	Tap13	Tap14	ochoff<1>	ddr<2>	ddr<3>	ddr<4>	ddr<5>	ddr<6>	ddr<7>
0	6	1	0	0	0	0	0	0	0	0
1	6	0	0	0	0	0	0	0	1	0
0	5	2	0	0	0	0	0	1	0	0
0	5	2	0	0	0	0	1	0	0	0
2	5	0	0	0	0	1	0	0	1	0
2	5	0	0	0	1	0	0	0	1	0
1	5	1	0	0	0	0	0	1	1	0
1	5	1	0	0	0	1	0	0	0	0
1	5	1	0	0	0	0	1	0	1	0
1	5	1	0	0	1	0	0	0	0	0
0	5	1	1	0	0	0	0	0	0	1
0	4	3	0	0	0	0	1	1	0	0
0	4	2	1	0	0	0	0	1	0	1
0	4	2	1	0	0	0	1	0	0	1
1	4	2	0	0	0	0	1	1	1	0
1	4	2	0	0	0	1	0	1	0	0



Tap11	Tap12	Tap13	Tap14	ochoff<1>	ddr<2>	ddr<3>	ddr<4>	ddr<5>	ddr<6>	ddr<7>
1	4	2	0	0	0	1	1	0	0	0
1	4	2	0	0	1	0	0	1	0	0
1	4	2	0	0	1	0	1	0	0	0
1	4	1	1	0	0	0	0	1	1	1
1	4	1	1	0	0	0	1	0	1	1
1	4	1	1	0	0	1	0	0	0	1
1	4	1	1	0	1	0	0	0	0	1
2	4	1	0	0	0	1	0	1	1	0
2	4	1	0	0	0	1	1	0	1	0
2	4	1	0	0	1	0	0	1	1	0
2	4	1	0	0	1	0	1	0	1	0
2	4	1	0	0	1	1	0	0	0	0
3	4	0	0	0	1	1	0	0	1	0
0	3	3	1	0	0	0	1	1	0	1
1	3	3	0	0	1	0	1	1	0	0
1	3	3	0	0	0	1	1	1	0	0
1	3	2	1	0	0	0	1	1	1	1
1	3	2	1	0	0	1	0	1	0	1
1	3	2	1	0	0	1	1	0	0	1
1	3	2	1	0	1	0	0	1	0	1
1	3	2	1	0	1	0	1	0	0	1
2	3	2	0	0	0	1	1	1	1	0
2	3	2	0	0	1	0	1	1	1	0
2	3	2	0	0	1	1	0	1	0	0
2	3	2	0	0	1	1	1	0	0	0
2	3	1	1	0	0	1	0	1	1	1
2	3	1	1	0	0	1	1	0	1	1
2	3	1	1	0	1	0	0	1	1	1
2	3	1	1	0	1	0	1	0	1	1
2	3	1	1	0	1	1	0	0	0	1
3	3	1	0	0	1	1	0	1	1	0
3	3	1	0	0	1	1	1	0	1	0
2	2	3	0	0	1	1	1	1	0	0
1	2	3	1	0	0	1	1	1	0	1
1	2	3	1	0	1	0	1	1	0	1
3	2	1	1	0	1	1	0	1	1	1
3	2	1	1	0	1	1	1	0	1	1
3	2	2	0	0	1	1	1	1	1	0
2	2	2	1	0	0	1	1	1	1	1
2	2	2	1	0	1	0	1	1	1	1
2	2	2	1	0	1	1	0	1	0	1
2	2	2	1	0	1	1	1	0	0	1
0	5	1	0	1	0	0	0	0	0	0
1	5	0	0	1	0	0	0	0	1	0
0	4	2	0	1	0	0	0	1	0	0
0	4	2	0	1	0	0	1	0	0	0
0	4	1	1	1	0	0	0	0	0	1



Tap11	Tap12	Tap13	Tap14	ochoff<1>	ddr<2>	ddr<3>	ddr<4>	ddr<5>	ddr<6>	ddr<7>
1	4	1	0	1	0	0	0	1	1	0
1	4	1	0	1	0	0	1	0	1	0
1	4	1	0	1	0	1	0	0	0	0
1	4	1	0	1	1	0	0	0	0	0
2	4	0	0	1	0	1	0	0	1	0
2	4	0	0	1	1	0	0	0	1	0
0	3	3	0	1	0	0	1	1	0	0
0	3	2	1	1	0	0	0	1	0	1
0	3	2	1	1	0	0	1	0	0	1
1	3	2	0	1	0	0	1	1	1	0
1	3	2	0	1	0	1	0	1	0	0
1	3	2	0	1	0	1	1	0	0	0
1	3	2	0	1	1	0	0	1	0	0
1	3	2	0	1	1	0	1	0	0	0
1	3	1	1	1	0	0	0	1	1	1
1	3	1	1	1	0	0	1	0	1	1
1	3	1	1	1	0	1	0	0	0	1
1	3	1	1	1	1	0	0	0	0	1
2	3	1	0	1	0	1	0	1	1	0
2	3	1	0	1	0	1	1	0	1	0
2	3	1	0	1	1	0	0	1	1	0
2	3	1	0	1	1	0	1	0	1	0
2	3	1	0	1	1	1	0	0	0	0
3	3	0	0	1	1	1	0	0	1	0
0	2	3	1	1	0	0	1	1	0	1
1	2	3	0	1	0	1	1	1	0	0
1	2	3	0	1	1	0	1	1	0	0
1	1	3	1	1	0	1	1	1	0	1
1	1	3	1	1	1	0	1	1	0	1
1	2	2	1	1	0	0	1	1	1	1
1	2	2	1	1	0	1	0	1	0	1
1	2	2	1	1	0	1	1	0	0	1
1	2	2	1	1	1	0	1	0	0	1
2	2	1	1	1	0	1	0	1	1	1
2	2	1	1	1	0	1	1	0	1	1
2	2	1	1	1	1	0	1	0	1	1
2	2	1	1	1	1	1	0	0	0	1
2	2	2	0	1	0	1	1	1	1	0
2	2	2	0	1	1	0	1	1	1	0
2	2	2	0	1	1	1	1	0	0	0
2	2	2	0	1	1	1	1	0	0	0
3	2	1	0	1	1	1	0	1	1	0
3	2	1	0	1	1	1	1	0	1	0
3	1	1	1	1	1	1	0	1	1	1
3	1	1	1	1	1	1	1	0	1	1





When the control **ochoff<1>** is 0, channel 1 is on. The amplitude of channel 1, which is always connected to Tap12, cannot be lowered through the analog controls. Other tap weights can be lowered to zero through analog controls **tncriX**. As a result, if **ochoff<1>** is 0, Tap12 is always present at the output with the minimum weight of 1. If **ochoff<1>** is 1, then the weight of each tap can be set to any fraction of full weight between zero, and the maximum value presented in the table.

Table 3 presents all valid pre-emphasis combinations of maximum tap weights for LSB data input d2p/d2n along with the corresponding digital control settings.

Table 3. Maximum Tap Weight Combinations for LSB Data Stream

Tap21	Tap22	Tap23	Tap24	ddr<8>	ddr<9>	ddr<10>	ddr<11>	ddr<12>
0	4	1	0	0	0	0	0	0
1	4	0	0	0	0	0	1	0
0	3	2	0	0	0	1	0	0
0	3	2	0	0	1	0	0	0
0	3	1	1	0	0	0	0	1
1	3	1	0	0	0	1	1	0
1	3	1	0	0	1	0	1	0
1	3	1	0	1	0	0	0	0
2	3	0	0	1	0	0	1	0
0	2	3	0	0	1	1	0	0
1	1	3	0	1	1	1	0	0
0	1	3	1	0	1	1	0	1
0	2	2	1	0	0	1	0	1
0	2	2	1	0	1	0	0	1
1	2	2	0	0	1	1	1	0
1	2	2	0	1	0	1	0	0
1	2	2	0	1	1	0	0	0
1	2	1	1	0	0	1	1	1
1	2	1	1	0	1	0	1	1
1	2	1	1	1	0	0	0	1
2	2	1	0	1	1	0	1	0
1	1	2	1	0	1	1	1	1
1	1	2	1	1	0	1	0	1
1	1	2	1	1	1	0	0	1
2	2	1	0	1	0	1	1	0
2	2	1	0	1	1	0	1	0
2	1	1	1	1	0	1	1	1
2	1	1	1	1	1	0	1	1

The weight of each tap for LSB data stream can be set to any fraction of full weight between zero, and the maximum value presented in the table. Weight settings for MSB data and LSB data streams are independent of each other. In order to form a PAM4 signal, the combined weight of the LSB taps should be equal to half of the combined weight of the MSB taps.



The quality of the output signal shape can be optimized using digital control bytes `vshcrID1`, and `vshcrID2`. Internal DAC blocks provide two analog voltages that are connected to bases of cascode transistors of output buffers. Higher values of digital codes `vshcrID1` and `vshcrID2` correspond to lower voltage levels. Voltages on bases of cascode transistors control peaking on falling edges of the output signals. More positive voltages correspond to higher peaking. The control byte `vshcrID1` adjusts peaking of MSB channels. The control byte `vshcrID2` adjusts peaking of LSB channels.

The internal common-mode level reference voltage for analog amplitude control of all output buffers can be adjusted through the control byte `vthcrl`. Maximum or minimum amplitude settings may be adjusted with this control for all output buffers simultaneously. Differential analog control voltage `xadjp/xadjn` can be utilized to adjust the crossing points of single-ended output eyes. At the default state of `xadjp = xadjn = 0V`, the crossing points in both direct and inverted eyes should be centered. The crossing points are moving up in the direct eye, and down in the inverted eye if `xadjp = -xadjn > 0`, or in the opposite directions if `xadjp = -xadjn < 0`.

An example of the PAM4 output eye at 32GBaud is shown in Fig. 3.

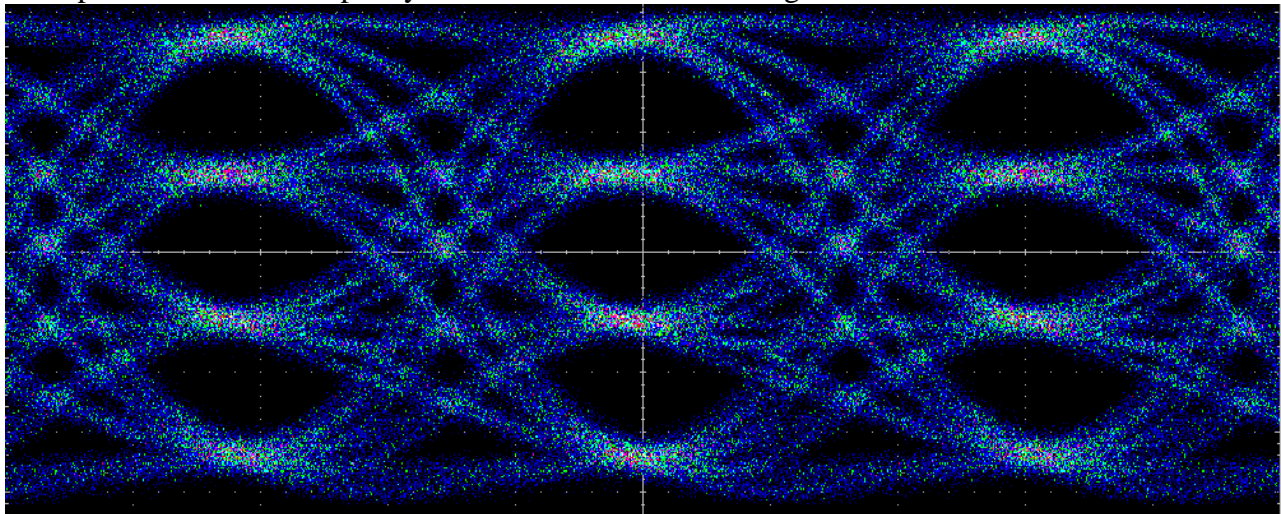


Fig. 3. PAM4 Output Eye at 32GBaud

## Temperature Sensor

A linear temperature sensor is included on chip. Its behavior is illustrated in Fig. 4 below. The demonstrated voltage has been generated on the internal 11KOhm resistor connected to vdd.

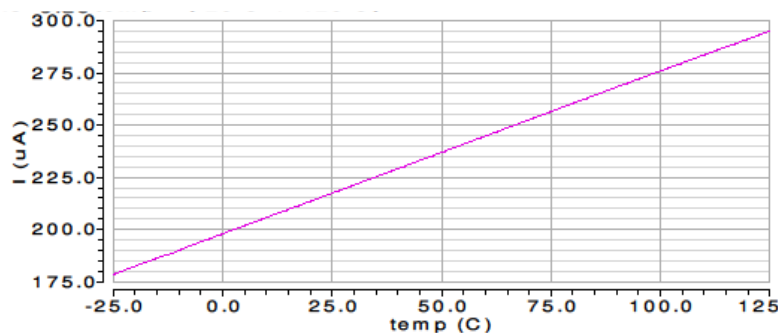


Fig. 4. Temperature Sensor's Characteristic

### 3-Wire Interface Control Block

To reduce the physical number of control inputs to the encoder chip, internal shift registers with a 3-wire input interface have been included on chip. The inputs of the 3-wire interface control block are internally terminated to vdd. The value of the termination resistors depends on the value of the DC CMOS input control  $3wtermoff$ . Table 4 presents the dependence of the input termination resistances on the value of the input  $3wtermoff$ . The default value of each input termination resistor is 50 Ohms.

Table 4. 3-Wire Interface Input Termination Resistance Dependence

Value of $3wtermoff$ , V	Input Termination Resistance, Ohms
vdd-2.5 (default)	50
vdd	102000

The SPI block is powered by an internally generated supply voltage of +1.2V from  $vee$ . External pins  $v1p2$  can be used for monitoring and adjustment (if needed) of the internal power supply voltage of the SPI block. For normal operation, the pins  $v1p2$  should be left not connected. The digital control bits applied through  $3wdin$  input are latched in, and shifted down the register with the clock  $3wcin$ . The SPI block includes two shift registers of 4 bytes and 8 bytes. They have separate write enable signals but share input data and clock signals. The 4-byte register is controlled by the signal  $3wen1in$ . The 8-byte register is controlled by the signal  $3wen2in$ .

The 4-byte register provides controls to digital switches with relatively high transition speed. This allows dynamic tap reconfiguration in accordance with PCI control regulations. The total reconfiguration time does not exceed 100ns from the external assignment of new control signals of the 4-byte register to the final settling of the output data amplitude.

The 8-byte register uses identical components, and the same input clock and input data signals as the 4-byte one. So it is capable of dynamic reconfiguration as well. However, it provides controls to low-speed switches and DACs. These controls should be considered to be DC. Separate write enable signals for the two sections allow independent write, and read access for dynamic and DC digital controls.

SPI load order is illustrated in Fig. 5.

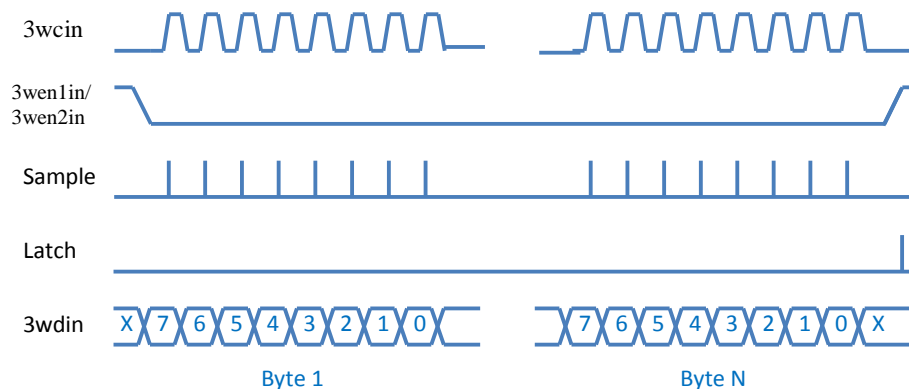


Fig. 5. SPI Load Order

Write enable signals  $3wen1in$  and/or  $3wen2in$  must be set to logic “0” during the data read-in phase. The SPI data can be monitored through the output  $3wdo$ . It should be noted that the output data present the previous state of the corresponding register.

Table 5 presents the byte order of the 3-wire interface block.

Table 5. Control Bytes

EN #	Byte Number	Bit Number							
		7	6	5	4	3	2	1	0
3wen1in	1	ddcrl(12:5)							
	2	ddcrl(4:2)			X	ochoff(12:9)			
	3	ochoff(8:2)						ochoff(1)	
	4	tapinv(8:1)							
3wen2in	1	skwadj1(7:0)							
	2	skwadj2(7:0)							
	3	skwadjc(7:0)							
	4	ckdbrbyp*	XXX			ckdbradj(11:8)			
	5	ckdbradj(7:0)							
	6	vthcrl(7:0)							
	7	vshcrlD1(7:0)							
	8	vshcrlD2(7:0)							

\*) – SPI outputs both  $\_p$  and  $\_n$  copies of this signal

## POWER SUPPLY CONFIGURATION

The part operates with the floating supply configuration shown in Fig. 6. The first negative supply (PSU1 source) is referenced to  $vdd$ , which is assumed to be the external ground (GND). Its negative pin provides the chip’s internal common node voltage. The second supply (PSU2) is floating (not connected to GND) and has its negative pin connected to the negative pin of PSU1 ( $vee$ ), and thus to the on-chip common node. The second power supply unit PSU2 provides a floating positive supply voltage  $v3p5$  for the high-speed internal circuitry. The third positive supply voltage  $v1p2$  for the internal CMOS circuitry is generated inside the chip but also can be supplied from outside using a third power supply unit PSU3 as shown in Fig. 6.

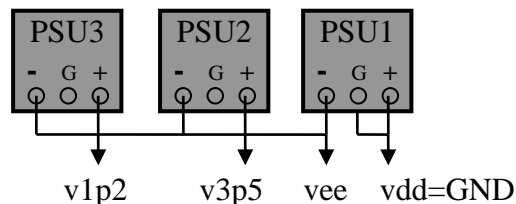


Fig. 6. Floating Supply Configuration

The part’s output signals are referenced to  $vdd$ . If a different output reference voltage is required,  $vdd$  can be changed to any voltage. In this case, a fourth power supply is required and all other power supplies should be floating. For more details see the AN\_ASNT6103-KMF document.



All the characteristics detailed below assume  $v_{dd} = GND = 0.0V$ .

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 6 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed  $v_{dd}$ ).

Table 6. Absolute Maximum Ratings

Parameter	Min	Max	Units
Negative Supply Voltage ( $v_{ee}$ )		-4.8	V
Positive Supply Voltage ( $v_{3p5}$ )		3.8	V
Positive Supply Voltage ( $v_{1p2}$ )		1.5	V
Power Consumption		5.0	W
RF Input Voltage Swing (SE)		1.2	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## TERMINAL FUNCTIONS

Supply And Termination Voltages		
Name	Description	Pin Number
$v_{dd}$	External ground	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 54, 55, 57, 59, 60
$v_{ee}$	-4.3V negative power supply	17, 32, 33, 48, 64
$v_{3p5}$	+3.5V positive power supply, negative pin to $v_{ee}$	1, 16, 39, 49, 63
$v_{1p2}$	Positive power supply, negative pin to $v_{ee}$ . Generated inside the chip and may be applied externally.	10



TERMINAL			Description
Name	No.	Type	
<b>High-Speed I/Os</b>			
d1p	19	CML input with internal SE 500hm termination to vdd	Differential high-speed data input
d1n	21		
d2p	28		
d2n	30		
cip	35		
cin	37		
qp	56	CML output requires external SE 500hm termination to vdd	Differential high-speed clock output
qn	58		
<b>Low-Speed I/Os</b>			
3wen1in	24	CML-type SE input with internal 500hm or 102kOhm termination to vdd	Enable input signal for higher speed section of 3-wire interface
3wen2in	26		Enable input signal for lower speed section of 3-wire interface
3wcin	25		Clock input signal for 3-wire interface
3wdin	23		Data input signal for 3-wire interface
3wtrmoff	12	2.5V CMOS input	Switches internal terminations to vdd of 3-wire interface inputs from 500hms to 102kOhms
3wdo	14	1.2V CMOS output	Data output signal of 3-wire interface
<b>Analog Control Voltage Inputs</b>			
xadjp	5	Analog input	Output data eye cross point adjustment, Differential
xadjn	3		
tncl2	8	Analog input	Output amplitude adjustment of Channel 2
tncl3	7		Output amplitude adjustment of Channel 3
tncl4	62		Output amplitude adjustment of Channel 4
tncl5	61		Output amplitude adjustment of Channel 5
tncl6	53		Output amplitude adjustment of Channel 6
tncl7	52		Output amplitude adjustment of Channel 7
tncl8	51		Output amplitude adjustment of Channel 8
tncl9	50		Output amplitude adjustment of Channel 9
tncl10	46		Output amplitude adjustment of Channel 10
tncl11	44		Output amplitude adjustment of Channel 11
tncl12	42		Output amplitude adjustment of Channel 12
<b>Analog Control Indicators</b>			
temp	9	Analog output	Linear temperature-dependent voltage output with internal 11KOhm termination to vdd.
dcyc1	41		Linear voltage indicating output clock duty cycle
dcyc0	40		Linear voltage indicating main input clock duty cycle





## ELECTRICAL CHARACTERISTICS

### Main Parameters

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee	-4.1	-4.3	-4.5	V	
vdd		0.0		V	External ground
v3p5	3.4	3.5	3.6	V	“-“ pin to vee
$I_{-4.3}$	120		220	mA	Depending on the settings of data amplitudes <sup>1)</sup>
$I_{v3p5}$	850		1020	mA	
Power	3.5	4.0	4.5	W	
Junction temperature	0	50	100	°C	
<b>Data input (d1p/d1n, d2p/d2n)</b>					
Rate	1.0		36	Gb/s	
SE Swing	50	200	500	mV	Peak-to-peak
CM Level	vdd-(SE swing)/2				
<b>Clock inputs (cip/cin)</b>					
Frequency (Ci input)	1.0		16	GHz	Fx1 mode
	4.0		18	GHz	Fx2 mode, ckdbadj needs tuning
SE Swing	50	200	500	mV	Peak-to-peak
CM Level	vdd-(SE swing)/2				
<b>Data output (qp/qn)</b>					
Rate	1.0		36	Gb/s	
SE Swing	0.0		1400	mV	Peak-to-peak
CM Level	vdd-0.1		vdd-0.70	V	Depends on the amplitude <sup>2)</sup>
Rise/Fall Times	12	13	14	ps	20%-80%
<b>Cross point control (xadjp/xadjn)</b>					
Differential voltage range	vdd-8.0		vdd+8.0	V	±4V at each input
CM Level	vdd				
Current in/out of the pin		+4 / -4		mA	at +4V / -4V
<b>Output Amplitude Controls (tncl2-tncl12)</b>					
Voltage range	vdd-2.5		vdd	V	
<b>PARAMETER      MIN    TYP    MAX    UNIT      COMMENTS</b>					
<b>Externally Controlled Operational Ranges</b>					
Input Clock delay	0		+26	ps	
Input Data delay	0		+26	ps	
Output eye cross point	-25		+25	%	of the eye amplitude



## Power Supply Currents (Preliminary Data, for Reference Only)

q amplitude	Clock multiplier	I <sub>4.3</sub> , mA	I <sub>v3p5</sub> , mA
min (0 segments 1/6, OCH off)	off		
min (0 segments 1/6, OCH on)	on		
max (11 segments 1/6, OCH off)	off		
max (11 segments 1/6, OCH on)	on		

## Data Output Common Mode Voltage (Preliminary Data, for Reference Only)

Amplitude			V <sub>CM</sub> , V	Amplitude			V <sub>CM</sub> , V
Total, mV	Segments 1/6	OCH		Total, mV	Segments 1/6	OCH	
	0	off	vdd-		6	off	vdd-
	0	on	vdd-		6	on	vdd-
	1	off	vdd-		7	off	vdd-
	1	on	vdd-		7	on	vdd-
	2	off	vdd-		8	off	vdd-
	2	on	vdd-		8	on	vdd-
	3	off	vdd-		9	off	vdd-
	3	on	vdd-		9	on	vdd-
	4	off	vdd-		10	off	vdd-
	4	on	vdd-		10	on	vdd-
	5	off	vdd-		11	off	vdd-
	5	on	vdd-		11	on	vdd-

## Additional Parameters

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>Duty Cycle Indicator (dcyc0/dcyc1)</b>					
Voltage range	vdd-3.3		vdd-0.8	V	
<b>Temperature Sensor (temp)</b>					
Voltage range	vdd-3.3		vdd-2.3	V	
<b>Internally Generated Supply Voltages (v1p2)</b>					
Voltage range	vee+1.1		vee+1.55	V	
<b>3-Wire Inputs (3wdin, 3wcin, 3wen1in, 3wen2in)</b>					
High voltage level	vdd-0.3		vdd	V	
Low voltage level	vdd-2		vdd-0.55	V	
Clock speed			1000	MHz	
<b>3-Wire Termination Control Switch (3wtrmoff)</b>					
High voltage level	vdd-0.3		vdd	V	
Low voltage level	vdd-2.5		vdd-2.2	V	





## PACKAGE INFORMATION

The chip die is housed in a custom 64-pin CQFP package. The dimensioned drawings are shown in Fig. 7. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vdd plane, which is ground for a negative supply, or power for a positive supply.

## 64-PIN KMF Package

All Dimensions are in millimeters

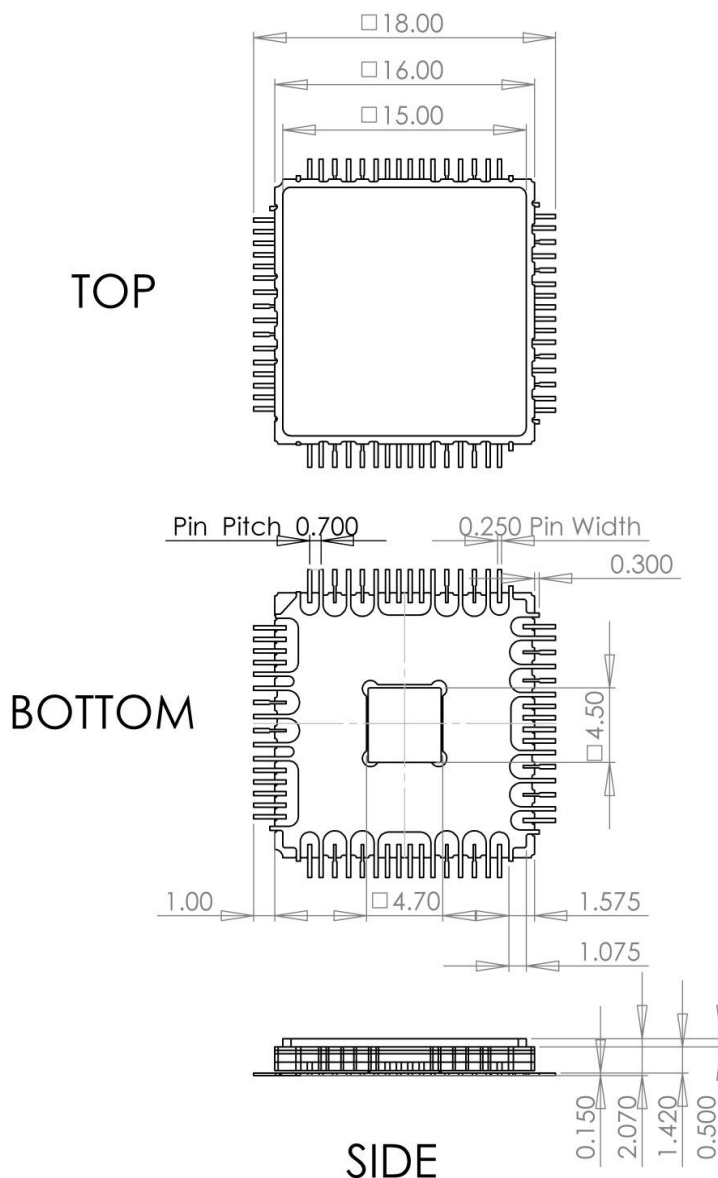


Fig. 7. CQFP 64-Pin Package Drawing (All Dimensions in mm)



The part's identification label is ASNT6103-KMF. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

## REVISION HISTORY

Revision	Date	Changes
1.3.2	01-2023	Corrected SPI description
1.2.2	06-2021	Formatting updates
1.1.2	06-2021	Updated Fig. 3 picture
1.0.2	06-2021	First release
0.0.2	10-2020	Preliminary release