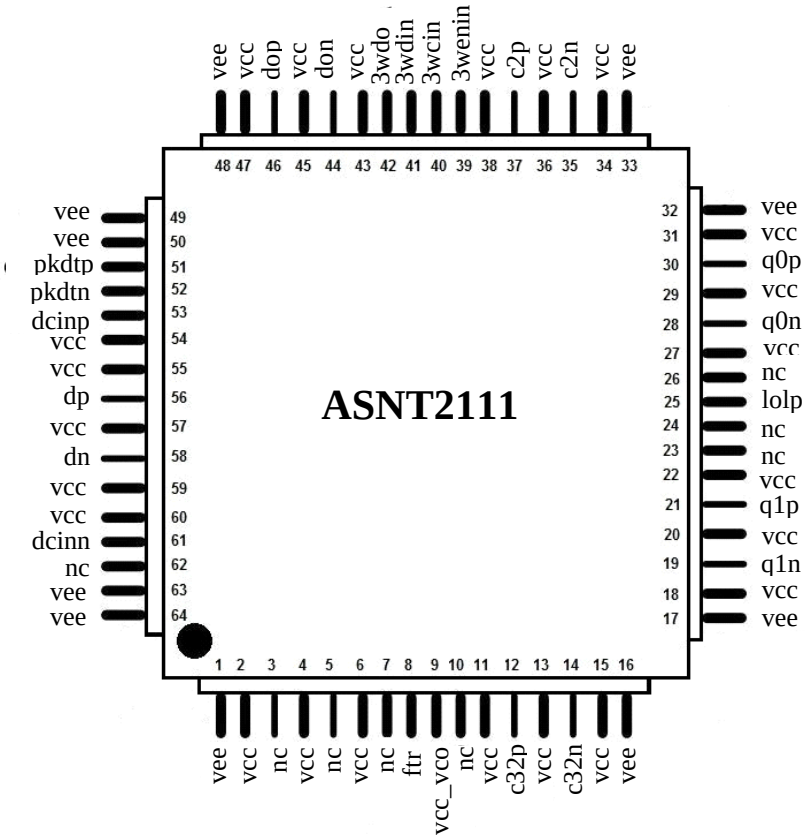
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ASNT2111-KMF
Programmable CDR DMUX 1-to-2

- 1:2 demultiplexer (DMUX) with integrated full-rate CDR
- Input data range from 18*Gb/s* to 36*Gb/s*
- NRZ input data format
- CML compliant differential input and output high-speed data and clock interfaces
- 1.3*V* CMOS 3-wire interface for digital controls
- LVDS or CML compliant input reference clock interface
- Full-rate clock and retimed data output for 1:1 CDR operation
- Half-rate data outputs with toggle synchronization functionality
- Signal inversion and muting capabilities in all output buffers
- Single +3.3*V* or -3.3*V* power supply
- Low power consumption of 1.8*W* at the maximum operational speed
- Industrial temperature range
- Custom CQFP 64-pin package



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DESCRIPTION

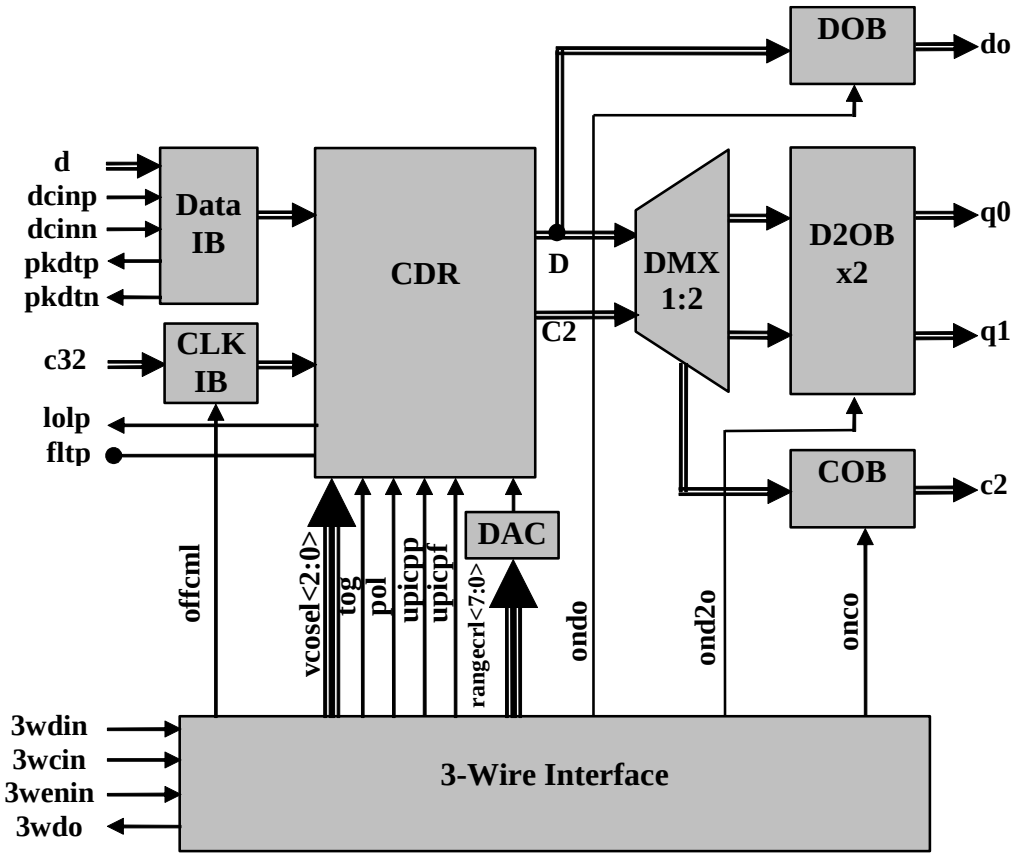

Fig. 1. Functional Block Diagram

ASNT2111-KMF is a 1:2 demultiplexer (DMUX) with full-rate integrated clock and data recovery (CDR). The IC shown in Fig. 1 functions in CDR mode covering a wide range of input data rates (f_{bit}) by utilizing its six on-chip VCOs (voltage-controlled oscillators). To reduce the physical number of control inputs to the chip, a shift register with a 3-wire input interface (SPI) has been included on chip. The SPI block provides all the digital controls for the chip. It also provides digital controls for digital-to-analog converters (DACs) that handle internal analog DC voltage adjustments.

Selection of the desired working data rate of the CDR is accomplished through the digital control vcosel (see Table 1). An external low speed system clock c32p/c32n running at 1/32 the frequency of the active VCO must be applied to the low-speed clock input buffer (CLK IB).

The main function of the chip is to convert a RZ or NRZ input data signal dp/dn with a bit rate of f_{bit} accepted by CML buffer (Data IB) into 2 parallel NRZ data signals q0p/q0n and q1p/q1n running at bit rates of $f_{bit}/2$ and delivered to the outputs by CML data output buffers (D2OBx2). The clock and data are recovered from the input data stream by the CDR.

A full rate retimed NRZ data output signal dop/don is also available through the CML data output buffer (DOB) allowing the part to be used as a 1:1 CDR. Half rate clock c2p/c2n delivered through the CML clock output buffer (COB) has a tight phase alignment to the demultiplexed data output signals q0p/q0n and q1p/q1n.

Data IB can operate with either differential or single-ended input signals. It includes tuning pins dcinp/dcinn for DC offset of the input signals in case of AC termination. When the buffer is operating with a DC-terminated single ended input signal, a correct threshold voltage should be applied to the unused input pin. A peak detector is also included to provide means of demodulating AM components carried by the input data with frequency ranges of up to a few hundred *kHz*. The peak detector's output signal is delivered to the differential port pkdtp/pkdtn.

All CML I/Os provide on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). Output buffers DOB, COB, and D2OBx2 can be individually disabled through control bits ondo, onco, and ond2o to save power.

Utilizing control bit pol, the deserializer can invert the polarity of the three output data signals. Control bit tog flips the order of q0p/q0n and q1p/q1n signals thus simplifying the interface between the DMUX and a following ASIC. It also allows for synchronization of the bit order of two or more DMUXes working in parallel.

A loss of lock CMOS alarm signal lolp is generated by the CDR to indicate its locking state. An off chip passive filter is required by the CDR, and should be connected to pin ftr (see CDR).

The deserializer is characterized for operation from 0°*C* to 125°*C* of junction temperature. The package temperature resistance is 15°*C* /*W*.

Data IB

The Data Input Buffer (Data IB) can process an input CML data signal dp/dn in either RZ or NRZ format due to its high analog bandwidth. It provides on-chip single-ended termination of 50*Ohm* to vcc for each input line. The buffer can also accept a single-ended signal to one of its input ports dp or dn with a threshold voltage applied to the unused pin in case of DC termination. In case of AC termination, tuning pins dcinp/dcinn allow for data common mode adjustment. The tuning pins have 1*kOhm* terminations to vcc and allow the user to change the slicing level before the data is sampled by the recovered clock. Tuning voltages from vcc to vee deliver 150*mV* of DC voltage shift.

Also included in Data IB is an input signal peak detector that delivers its response through the output differential signal pkdtp/pkdtn. The detector can demodulate AM component(s) carried by the input data with frequency ranges of up to a few hundred *kHz*. The detector's output impedance is 4*kOhm* single ended to vcc.

CLK IB

The Clock Input Buffer (CLK IB) consists of a proprietary universal input buffer (UIB) that can operate in either CML or LVDS mode depending on the state of digital control bit offcml. This control should be set to "low" for CML mode and to "high" for LVDS mode. Depending on the mode of operation, the input impedance switches between 50 *Ohms* to vcc single-ended in CML mode, and 100 *Ohms* differential in LVDS mode. The input buffer exceeds LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with a speed up to 1*Gb/s*, DC common mode voltage variation between vcc and vee, AC common mode noise with a frequency up to

5*MHz*, and voltage levels ranging from 0 to 2.4*V*. It can also receive a DC-terminated single-ended signal with a threshold voltage between vcc and vee applied to the unused pin.

CDR

The Clock and Data Recovery Block (CDR) contains a phase acquisition loop, and a frequency acquisition loop. The frequency loop works in concert with low-speed clock c32p/c32n while the phase loop utilizes input data signal dp/dn. The CDR requires a single off-chip filter shown in Fig. 2 to be connected to the pin ftr.

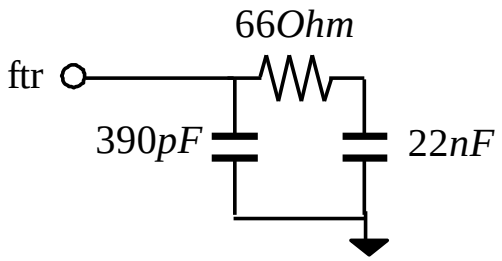

Fig. 2. External Loop Filter

The main function of the CDR is to frequency-lock the selected on-chip VCO to the input data signal (clock recovery) while phase-aligning it to latch in the incoming data with minimal error (data recovery). By default, the CDR aligns the recovered clock's working edge in the middle of the incoming data bits. The recovered clock is divided down in frequency by two (C2), and utilized by DMX 1:2 for demultiplexation of the recovered data.

By utilizing the 3-bit digital control vcosel, the desired working frequency of the CDR can be selected in accordance with Table 1 below to cover the entire operating range. Fig. 3 shows the measured average VCO operating ranges to visually demonstrate the frequency overlap between the 6 VCOs.

Table 1. CDR Mode Selection

vcosel	vcosel<2>	vcosel<1>	vcosel<0>	VCO Operation Frequency (*GHz*)
0	0	0	0	off
1	0	0	1	f_{min}≤18.0, f_{max}≥20.5
2	0	1	0	f_{min}≤20.5, f_{max}≥22.5
3	0	1	1	f_{min}≤24.5, f_{max}≥26.0
4	1	0	0	f_{min}≤27.0, f_{max}≥30.5
5	1	0	1	f_{min}≤31.0, f_{max}≥32.5
6	1	1	0	f_{min}≤33.5, f_{max}≥36.0
7	1	1	1	off

The loop gain can be adjusted by two control bits upicpp and upicpf that control the charge pump current as shown in Table 2.

Table 2. Charge Pump Current Control

upicpp	upicpf	Charge Pump current, *mA*
0	0	*I*max-0.31
0	1	*I*max-0.27
1	0	*I*max-0.04
1	1	*I*max

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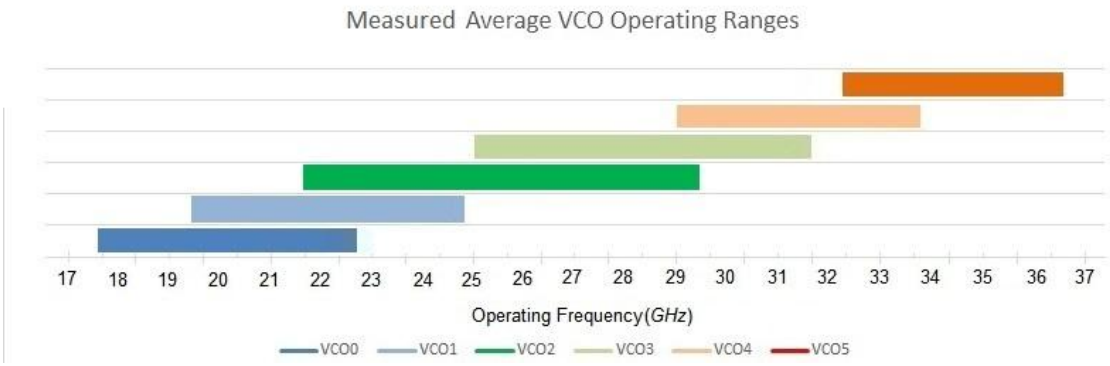

Fig. 3 Measured Average VCO Operating Ranges

By utilizing the control byte rngcrl the DC current of the control emitter follower of the active VCO can be adjusted linearly. Higher values of the control result in higher emitter follower currents. Higher emitter follower currents result in a more linear VCO frequency dependence on the control voltage at the expense of the frequency range.

The lock detect circuitry signals an alarm through the 2.5*V* CMOS signal lolp when a frequency difference exists between an applied system reference clock c32p/c32n and a recovered full rate clock divided-by-32 that is greater than ±1000*ppm*.

Another feature included in the CDR is the ability to simultaneously invert the polarity of all three data outputs through the 2.5*V* CMOS input pin pol (pol = "1" (default): direct; pol = "0": inverted). The order of the half-rate output data streams can be inverted by using the 2.5*V* CMOS input pin tog, which provides means to synchronize two adjacent DMUXes operating in parallel. The synchronization process may be accomplished by the "blind" toggling in one of the chips and leaving the task of recognizing the "right" position to downstream components (e.g. FEC chip).

DMX1:2

The 1 to 2 Demultiplexer (DMX1:2) latches in the retimed data stream D from the CDR on both edges of the half rate clock signal C2. The high speed data signal is subsequently demultiplexed into two half rate NRZ data signals, and delivered to D2OBx2 in parallel fashion as a 2-bit wide word with the order defined by the tog signal.

DOB

The Data Output Buffer (DOB) receives a full rate retimed serial data stream D from the CDR and converts it into a CML output signal dop/don. This CML buffer requires 50*Ohm* external termination resistors connected between vcc and each output. The buffer can be enabled or disabled by the control bit ondo (ondo = "1": enabled; ondo = "0": disabled).

D2OBx2

The Half Rate Data Output Buffer (D2OBx2) receives two half rate data signals from DMX1:2 and converts them into CML output signals q0p/q0n and q1p/q1n. The buffer requires 50*Ohm* external termination resistors connected between vcc and each output. The buffer can be enabled or disabled by the control bit ond2o (ond2o = "1": enabled; ond2o = "0": disabled).

COB

The Clock Output Buffer (COB) receives a half rate clock signal from DMX1:2 and converts it into CML output signal c2p/c2n. The buffer requires 50*Ohm* external termination resistors connected between vcc and each output. The buffer can be enabled, or disabled by the control bit onco (onco = "1": enabled; onco = "0": disabled). The negative edge of the c2 signal is aligned to the half rate output data crossing points.

3-Wire Interface Control Block

To reduce the physical number of control inputs to the chip, a 3-byte shift register with a 3-wire input interface has been included on chip. The SPI block is powered by an internally generated supply voltage of +1.2*V* from vee. The digital control bits applied through 3wdin input are latched in and shifted down the register with the clock 3wcin. Write enable signal 3wenin must be set to logic "0" during the data read-in phase. The SPI data can be monitored through the output 3wdo. Table 3 presents the byte order of the 3-wire interface block.

Table 3. Control Bytes

Byte Number	Bit Number							
	7	6	5	4	3	2	1	0
1	rngcrl(7:0)							
2	upicpf	upicpp	tog	onco	ond2o	ondo	pol	offcml
3	X	X	X	X	X	vcosel(2:0)		

SPI load order is illustrated in Fig. .

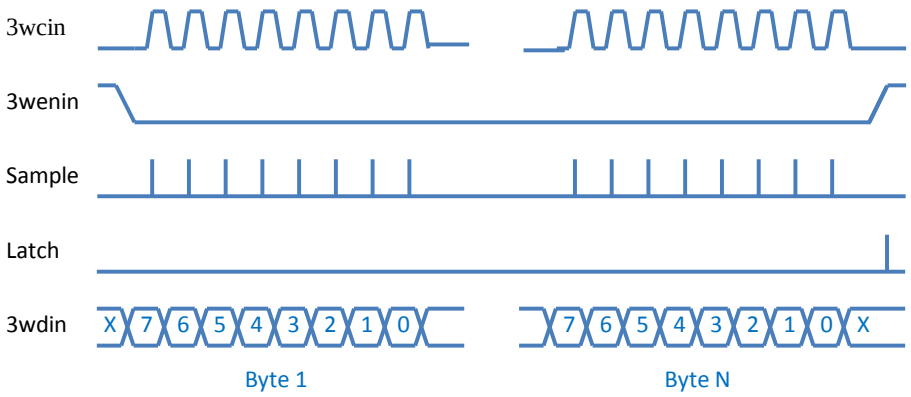

Fig. 4. SPI Load Order

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POWER SUPPLY CONFIGURATION

The ASNT2111-KMF can operate with either a negative supply (vcc = 0.0*V* = ground and vee = -3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 3.3*V* and vee = 0*V* (external ground)

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only that are specified in ELECTRICAL CHARACTERISTICS. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.8	*V*
Power Consumption		1.8	*W*
Input Voltage Swing (SE)		1.0	*V*
Case Temperature*)		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

*) - Operating the part at temperatures over this value could/will damage the part. Operating at this temperature or any temperatures above the recommended maximum value specified in ELECTRICAL CHARACTERISTICS does not guarantee correct functionality as is stated above.

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TERMINAL FUNCTIONS

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 54, 55, 57, 59, 60
vcc_vco	Positive power supply for VCO (+3.3*V*)	9
vee	Negative power supply (GND or 0*V*)	1, 16, 17, 32, 33, 48, 49, 50, 63, 64
nc	Not connected pins	3, 5, 7, 10, 23, 24, 26, 62

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	56	Input	CML differential data inputs with internal SE 50*Ohm* termination to VCC
dn	58		
q1p	21	Output	CML differential half rate data outputs. Require external SE 50*Ohm* termination to VCC
q1n	19		
q0p	30		
q0n	28		
c2p	37	Output	CML differential half rate clock outputs. Require external SE 50*Ohm* termination to VCC
c2n	35		
dop	46	Output	CML differential full rate data outputs. Require external SE 50*Ohm* termination to VCC
don	44		
Low-Speed I/Os			
c32p	12	Input	CML or LVDS clock input with internal SE 50*Ohm* SE or differential 100*Ohm* termination
c32n	14		
pkdtp	51	Output	Peak detector outputs
pkdtn	52		
3wenin	39	1.2*V* CMOS input	Enable input signal for 3-wire interface
3wcin	40		Clock input signal for 3-wire interface
3wdin	41		Data input signal for 3-wire interface
3wdo	42	1.2*V* CMOS output	Data output signal of 3-wire interface
Controls			
lolp	25	LS out, 2.5*V* CMOS	CDR lock indicator (high: no lock; low: locked)
dcinp	53	LS IN	Input data common mode voltage adjustment
dcinn	61		
ftr	8	I/O	External CDR filter connection

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.0	+3.3	+3.6	*V*	±9%
vee		0.0		*V*	
I_{vcc}		535		*mA*	All functions active
Power Consumption		1.8		*W*	
Junction Temperature	-25	50	125	*°C*	
Case temperature			75	*°C*	Recommended value
HS Input Data (dp/dn)					
Data Rate	18		36	*Gbps*	NRZ
Swing p-p (Diff or SE)	0.05		0.6	*V*	
CM Voltage Level	vcc-0.8		vcc	*V*	
LS Input Reference Clock (c32p/c32n)					
Frequency	562.5		1125	*MHz*	
Swing p-p (Diff or SE)	0.06		0.8	*V*	
CM Voltage Level	vee		vcc	*V*	
Duty Cycle	40	50	60	*%*	
HS Output Full Rate Data (dop/don)					
Data Rate	18		36	*Gbps*	NRZ
Logic “1” level		vcc		*V*	
Logic “0” level		vcc -0.4	vcc -0.3	*V*	
Jitter		7	8	*ps*	p-p
HS Output Half Rate Data (q0p/q0n, q1p/q1n)					
Data Rate	9		18	*Gbps*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc -0.4	vcc -0.3	*V*	
Jitter		7		*ps*	p-p
HS Output Half Rate Clock (c2p/c2n)					
Clock Rate	9		18	*GHz*	24 to 36*Gbps* input
Logic “1” level		vcc		*V*	
Logic “0” level	vcc -0.4		vcc -0.15	*V*	
Jitter		5	8	*ps*	p-p
Input Data Common Mode Control (dcinp/dcinn)					
Input DC Voltage	vee		vcc	*V*	
Input Data Voltage Shift	0		-150	*mV*	Referenced to vcc
Output of Peak Detector (pkdtp/pkdtn)					
Swing p-p (Diff)	-1		1	*V*	Over full input range
CM Voltage Level		vcc -1.0		*V*	
3-Wire Inputs (3wdin, 3wcin, 3wenin)					
High voltage level	vee+1.1		vee+1.35	*V*	
Low voltage level	vee		vee+0.35	*V*	
Clock speed		350	400	*MHz*	

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PACKAGE INFORMATION

The chip die is housed in a custom 64-pin CQFP package. The dimensioned drawings are shown in Fig. . The package's leads will be trimmed to a length of 1.0*mm*. After trimming, the package's leads will be further processed as follows:

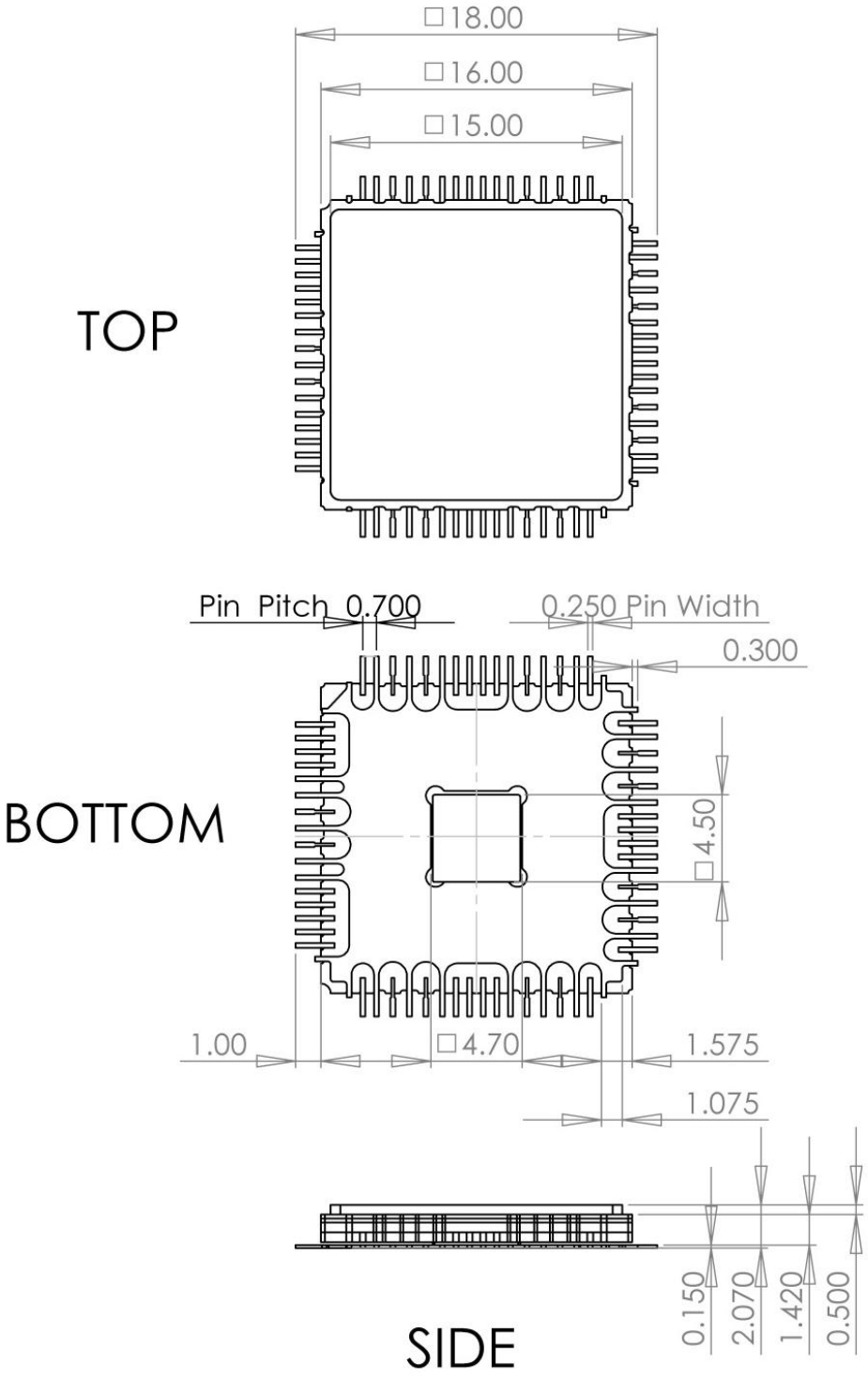

Fig. 5. CQFP 64-Pin Package Drawing (All Dimensions in mm)

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT2111-KMF. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2011/65/EU for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.2.2	09-2022	Revised CR section and added Fig. 3 Corrected Electrical Characteristics values
1.1.2	07-2022	Corrected frequency range Updated Electrical Characteristics values
1.0.2	10-2020	Official release Corrected frequency range Corrected filter schematic
0.0.1	03-2020	Preliminary release