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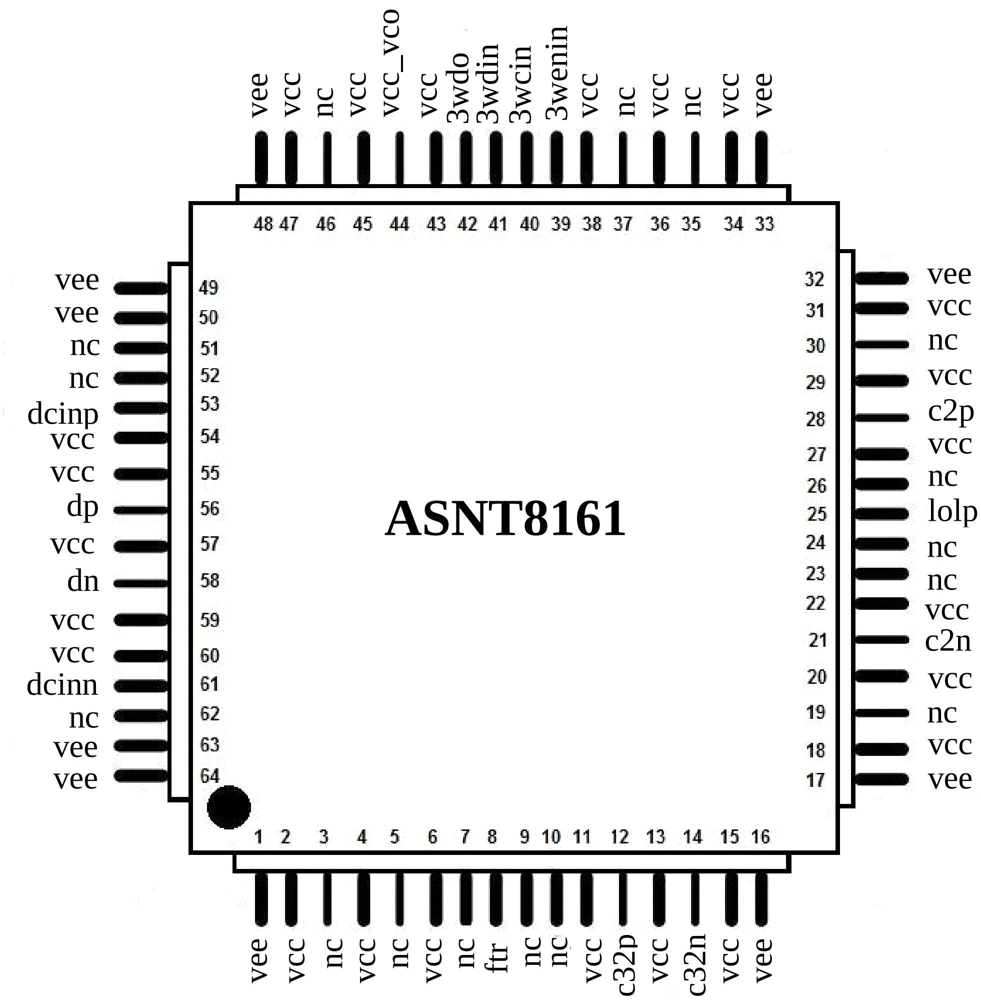
ASNT8161-KMF
Programmable CR with Peaking Adjustment

- Up to 72*Gb/s* half-rate clock recovery circuit
- Input data range from 36*Gb/s* to 72*Gb/s*
- NRZ and PAM4 input data format
- Input data and output clock peaking adjustment
- CML compliant differential input and output high-speed data and clock interfaces
- LVDS or CML compliant input reference clock interface
- Half rate clock output up to 36*GHz* for a 72*Gb/s* input data signal
- Single +3.3*V* or -3.3*V* power supply
- Low power consumption of 1.7*W* at the maximum operational speed
- Industrial temperature range
- Custom CQFP 64-pin package



DESCRIPTION

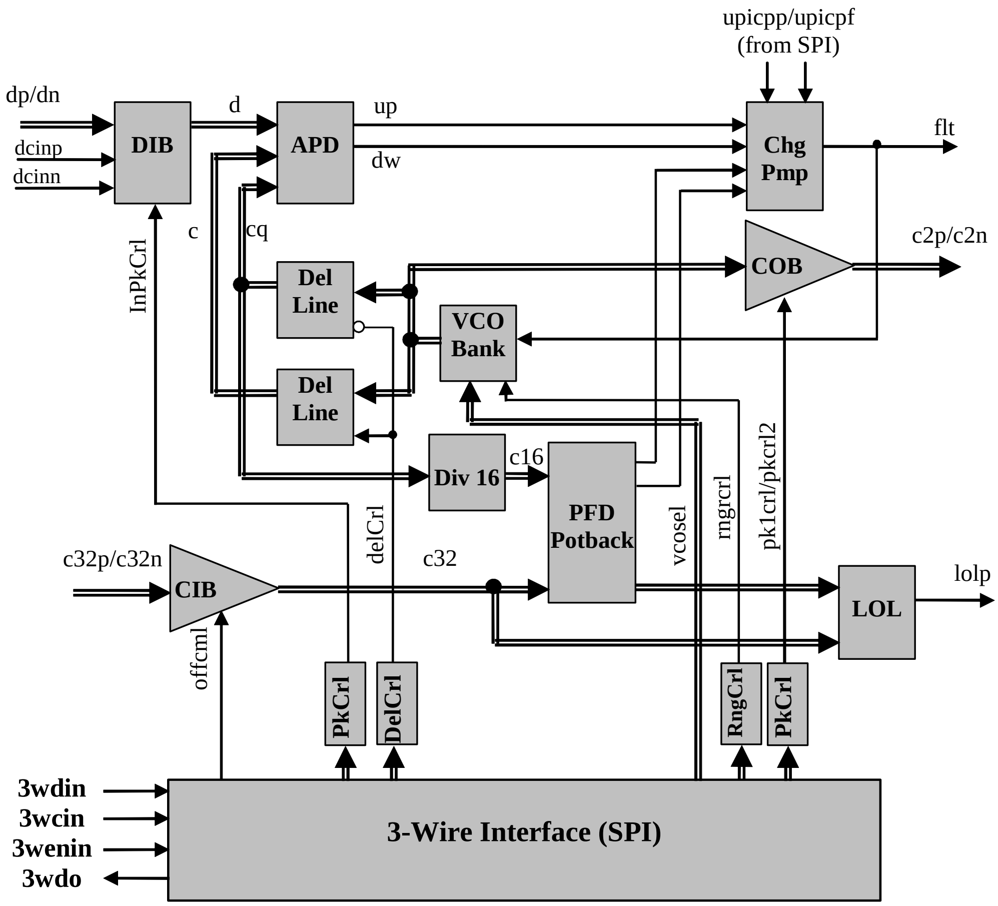


Fig. 1. Functional Block Diagram

ASNT8161-KMF is a half-rate integrated clock recovery (CR) circuit. The IC shown in Fig. 1 covers a wide range of input data rates (f_{bit}) by utilizing its six on-chip VCOs (voltage-controlled oscillators). To reduce the physical number of control inputs to the chip, a shift register with a 3-wire input interface (SPI) has been included on chip. The SPI block provides all the digital controls for the chip. It also provides digital controls for digital-to-analog converters (DACs) that handle internal analog DC voltage adjustments.

Selection of the desired working data rate of the CR is accomplished through the digital control vcosel (see Table 1). An external low speed system clock c32p/c32n running at 1/32 the frequency of the active VCO must be applied to the low-speed clock input buffer (CLK IB).

The main function of the chip is to recover from an NRZ or PAM4 input data signal dp/dn with a bit rate of f_{bit} accepted by CML buffer (Data IB) a half-rate clock c2p/c2n that is delivered to the output by the CML clock output buffer (COB). For example, a 28*GHz* clock signal will be generated from a 56*Gb/s* input data signal. The digital byte delCrl of SPI is used to properly set phases of the internal clock signals.

Data IB can operate with either differential or single-ended input signals. The buffer can provide a controlled peaking for the input signal (through the SPI). The buffer also includes tuning pins dcinp/dcinn for DC offset of the input signals in case of AC termination. When the buffer is operating with a DC-terminated single ended input signal, a correct threshold voltage should be applied to the unused input pin.

All CML I/Os provide on chip 50*Ohms* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION).

A loss of lock CMOS alarm signal lolp is generated by the CR to indicate its locking state. An off chip passive filter is required by the CR, and should be connected to pin ftr (see Core section).

The clock recovery circuit is characterized for operation from 0°*C* to 125°*C* of junction temperature. The package temperature resistance is 15°*C* /*W*.

Data IB

The Data Input Buffer (Data IB) can process an input CML data signal dp/dn in NRZ format. It provides on-chip single-ended termination of 50*Ohms* to vcc for each input line. The buffer can also accept a single-ended signal to one of its input ports dp, or dn with a threshold voltage applied to the unused pin in case of DC termination. In case of AC termination, tuning pins dcinp/dcinn allow for data common mode adjustment. The tuning pins have 1*KOhms* terminations to vcc, and allow the user to change the slicing level before the data is sent to the clock recovery section. Tuning voltages from vcc to vee deliver 150*mV* of DC voltage shift. SPI digital control byte inPkCrl may be used to linearly control DC currents of the input emitter followers. Higher values of the control result in greater peaking of the signal at the input of the phase detector.

CLK IB

The Clock Input Buffer (CLK IB) consists of a proprietary universal input buffer (UIB) that can operate in either CML, or LVDS mode depending on the state of digital control bit offcml. This control should be set to “low” for CML mode, and to “high” for LVDS mode. Depending on the mode of operation, the input impedance switches between 50*Ohms* to vcc single-ended in CML mode, and 100*Ohms* differential in LVDS mode. The input buffer exceeds LVDS standards IEEE Std. 1596.3-1996, and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with a speed up to 1*Gb/s*, DC common mode voltage variation between vcc and vee, AC common mode noise with a frequency up to 5*MHz*, and voltage levels ranging from 0 to 2.4*V*. It can also receive a DC-terminated single-ended signal with a threshold voltage between vcc, and vee applied to the unused pin.

Core

The main function of the CR is to frequency-lock the selected on-chip VCO to the input data signal (clock recovery). The CR core contains a phase acquisition loop, and a frequency acquisition loop. The phase acquisition loop includes a high-speed Alexander Phase Detector (APD) that processes the input data stream dp/dn, and two shifted clock signals that are provided by two parallel Delay Lines with oppositely connected delay controls. Using the SPI digital control byte delCrl, the phases of these two half-rate clock signals need to be lined up correctly with the incoming data dp/dn in the phase loop to ensure proper CR functionality. The frequency loop consists of a clock divider-by-16, and a PFD Potback block. The frequency acquisition loop works in concert with low-speed clock c32p/c32n. Both acquisition loops generate signals that control a single charge pump. The charge pump in combination with a filter generates an analog signal that controls the active VCO. The on-chip filter is small, so the CR requires a single off-chip filter shown in Fig. 2 to be connected to pin ftr.

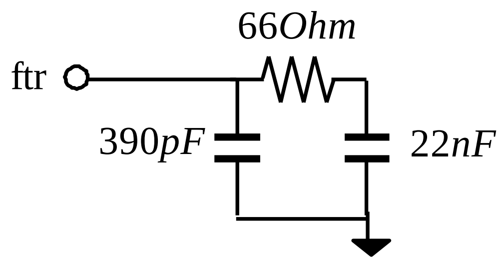


Fig. 2. External Loop Filter

By utilizing the 3-bit digital control vcosel, the desired working frequency of the CR can be selected in accordance with Table 1 below.

Table 1. CR Mode Selection

vcosel	vcosel<2>	vcosel<1>	vcosel<0>	**VCO Operation Frequency (*GHz*)**
0	0	0	0	off
1	0	0	1	f_{min}≤16.7, f_{max}≥24.5
2	0	1	0	f_{min}≤19.4, f_{max}≥28.2
3	0	1	1	f_{min}≤22.2, f_{max}≥31.6
4	1	0	0	f_{min}≤25.1, f_{max}≥34.7
5	1	0	1	f_{min}≤27.8, f_{max}≥37.2
6	1	1	0	f_{min}≤31.0, f_{max}≥39.9
7	1	1	1	off

The loop gain can be adjusted by two control bits upicpp, and upicpf that control the charge pump current as shown in Table 2.

Table 2. Charge Pump Current Control

upicpp	upicpf	**Charge Pump current, *mA***
0	0	*I*max-0.31
0	1	*I*max-0.27
1	0	*I*max-0.04
1	1	*I*max

By utilizing the control byte rngcrl, the DC current of the control emitter follower of the active VCO can be adjusted linearly. Higher values of the control result in higher emitter follower currents. Higher emitter follower currents result in a more linear VCO frequency dependence on the control voltage at the expense of the frequency range.

The lock detect circuitry signals an alarm through the 2.5*V* CMOS signal lolp when a frequency difference exists between an applied system reference clock c32p/c32n, and a recovered half rate clock divided-by-32 that is greater than ±1000*ppm*.

COB

The Clock Output Buffer (COB) receives a half-rate clock signal from CR, and converts it into CML output signal c2p/c2n. The buffer requires 50*Ohm* external termination resistors connected between vcc, and each output (usually supplied by the downstream chip that the buffer is driving). SPI digital control bytes pk1crl, and pk2crl may be used to linearly control DC currents of the two emitter followers of the COB. Higher values of the control result in greater peaking of the output signal.

3-Wire Interface Control Block

To reduce the physical number of control inputs to the chip, a 6-byte shift register with a 3-wire input interface has been included on chip. The SPI block is powered by an internally generated supply voltage of +1.2*V* from vee. The digital control bits applied through 3wdin input are latched in, and shifted down the register with clock 3wcin. Write enable signal 3wenin must be set to logic "0" during the data read-in phase. The SPI data can be monitored through the output 3wdo. Table 3 presents the byte order of the 3-wire interface block.

Table 3. Control Bytes

Byte Number	Bit Number							
	7	6	5	4	3	2	1	0
1	vcosel(2:0)			X	X	upicpf	offcml	upicpp
2	delCrl(7:0)							
3	inPkCrl(7:0)							
4	rangecrl(7:0)							
5	pk2crl(7:0)							
6	pk1crl(7:0)							

The SPI load order is illustrated in Fig. 3.

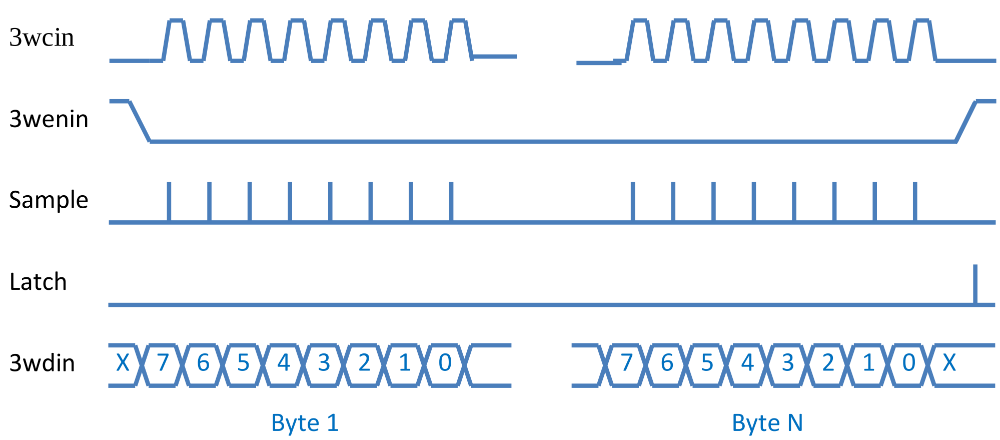


Fig. 3. SPI Load Order

POWER SUPPLY CONFIGURATION

The ASNT8161-KMF can operate with either a negative supply (vcc = 0.0*V* = ground, and vee = -3.3*V*), or a positive supply (vcc = +3.3*V*, and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 3.3*V* and vee = 0*V* (external ground)

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 4 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.8	*V*
Power Consumption		1.7	*W*
Input Voltage Swing (SE)		1.0	*V*
Case Temperature*)		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
c2p	28	Output	CML differential half rate clock outputs. Require external SE 50*Ohm* termination to vcc
c2n	21		
dp	56	Input	CML differential data inputs with internal SE 50*Ohm* termination to vcc
dn	58		
Low-Speed I/Os			
c32p	12	Input	CML or LVDS clock input with internal SE 50*Ohm* SE or differential 100*Ohm* termination
c32n	14		
3wenin	39	1.2*V* CMOS input	Enable input signal for 3-wire interface
3wcin	40		Clock input signal for 3-wire interface
3wdin	41		Data input signal for 3-wire interface
3wdo	42	1.2*V* CMOS output	Data output signal of 3-wire interface
Controls			
lolp	25	LS out, 2.5*V* CMOS	CDR lock indicator (high: no lock; low: locked)
dcinp	53	LS IN	Input data common mode voltage adjustment
dcinn	61		
ftr	8	I/O	External CR filter connection

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Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 54, 55, 57, 59, 60
vcc_vco	Positive power supply for VCO (+3.3*V*)	44
vee	Negative power supply (GND or 0*V*)	1, 16, 17, 32, 33, 48, 49, 50, 63, 64
nc	Not connected pins	3, 5, 7, 9, 10, 19, 23, 24, 26, 30, 35, 37, 46, 51, 52, 62

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.0	+3.3	+3.6	*V*	±9%
vee		0.0		*V*	
I_{vcc}		515		*mA*	All functions active
Power Consumption		1.7		*W*	
Junction Temperature	-25	50	125	*°C*	
Case temperature			75	*°C*	Recommended value
HS Input Data (dp/dn)					
Data Rate	36		72	*Gbps*	NRZ
Swing p-p (Diff or SE)	0.3		0.6	*V*	
CM Voltage Level	vcc-0.8		vcc	*V*	
LS Input Reference Clock (c32p/c32n)					
Frequency	562.5		1125	*MHz*	For LOL operation it must be ±10*KHz* from the selected VCO frequency
Swing p-p (Diff or SE)	0.06		0.8	*V*	
CM Voltage Level	vee		vcc	*V*	
Duty Cycle	40	50	60	*%*	
HS Output Half-Rate Clock (c2p/c2n)					
Clock Rate	18		36	*GHz*	36 to 72*Gbps* input
Logic "1" level		vcc		*V*	
Logic "0" level	vcc -0.4		vcc -0.15	*V*	
Jitter		5	8	*ps*	p-p
Input Data Common Mode Control (dcinp/dcinn)					
Input DC Voltage	vee		vcc	*V*	
Input Data Voltage Shift	0		-150	*mV*	Referenced to vcc
3-Wire Inputs (3wdin, 3wcin, 3wenin)					
High voltage level	vee+1.1		vee+1.35	*V*	
Low voltage level	vee		vee+0.35	*V*	
Clock speed		350	400	*MHz*	

PACKAGE INFORMATION

The chip die is housed in a custom 64-pin CQFP package. The dimensioned drawings are shown in Fig. 4. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8161-KMF. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

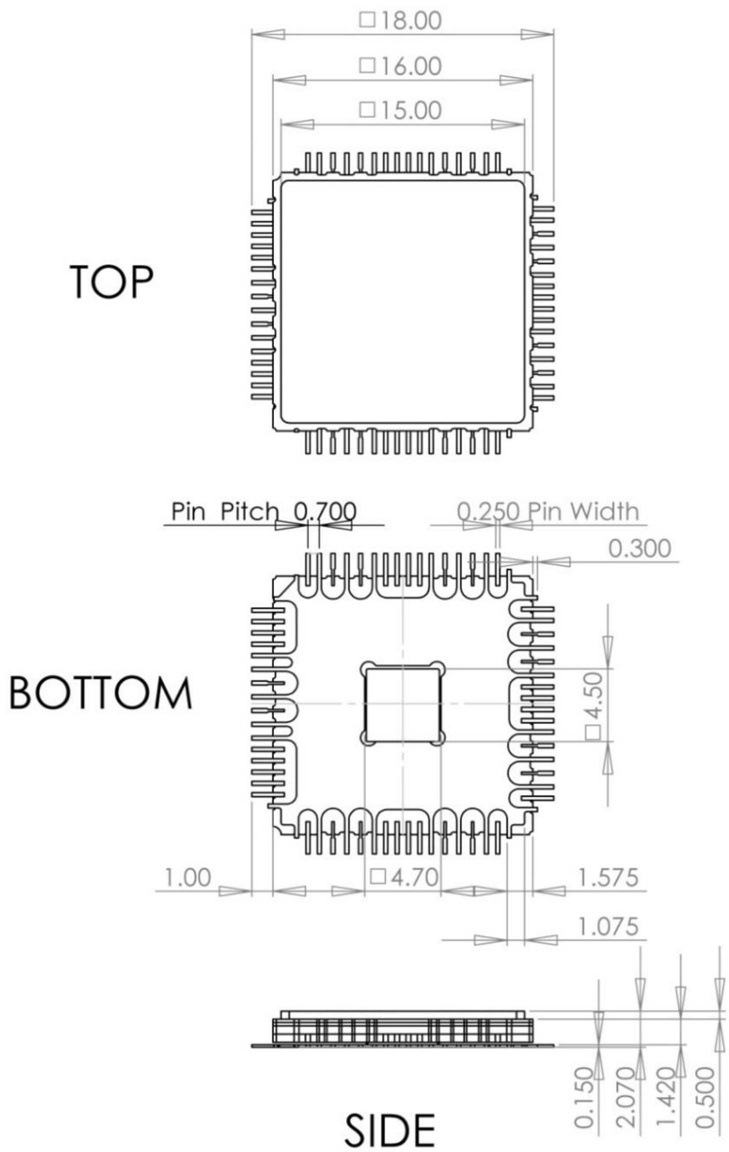

Fig. 4. CQFP 64-Pin Package Drawing (All Dimensions in mm)

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This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.2.2	05-2024	Corrected Reference Clock Frequencies
1.1.2	03-2022	Corrected Terminal Functions
1.0.2	11-2020	Official release Corrected filter schematic Added comment for reference clock frequency Updated package information
0.1.2	10-2020	Corrected BW
0.0.2	09-2020	Preliminary release