ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Dr., Ste #112, Torrance, CA 90505

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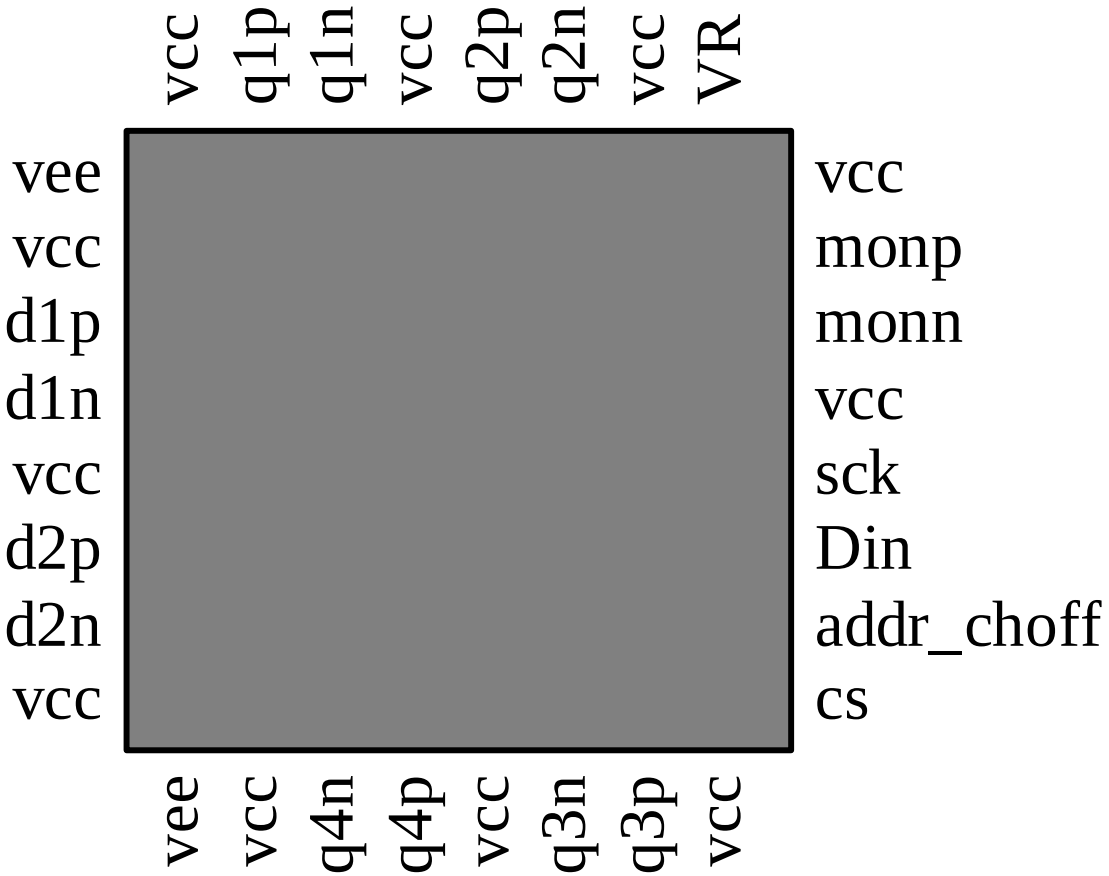
IFC151 / ASNT5142-ALP
DC-32*GHz* XOR Logic Gate with 5 Output Drivers

- High speed broadband Exclusive-OR (XOR) Boolean logic gate with 1:5 splitter and 5 independent output drivers
- Fully differential CML input interfaces
- Fully differential CML output interfaces with externally adjustable voltage swings
- Optional SPI interface for external adjustment of peaking/bandwidth and output voltage swings
- Dual power supply with a possibility of output common mode voltage control
- Ground-independent floating supplies to allow for the output common mode voltage adjustment
- Maximum power consumption: 1.15*W* at 2.8*V* supply
- Fabricated in SiGe for high performance, yield, and reliability
- Custom 32-pin LGA package with exposed die substrate at the top



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DESCRIPTION

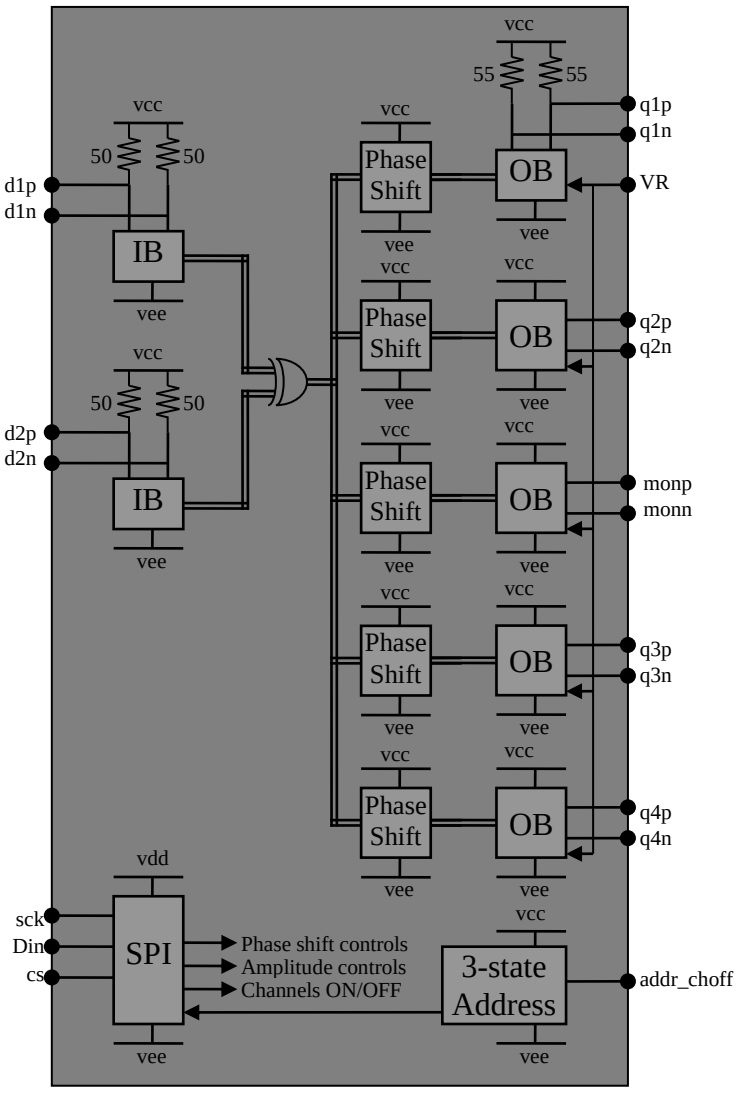

Fig. 1. Functional Block Diagram

This SiGe IC provides broadband Exclusive-OR (XOR) Boolean logic functionality in combination with a 1-to-5 output signal splitter, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can perform XOR operation with a high-speed data or clock input signal d1p/d1n and another high-speed data or clock input signal d2p/d2n. The resulting high-speed double-rate or double-frequency output signal is splitted into 5 identical signals and delivered to the output ports q1p/q1n, q2p/q2n, q3p/q3n, q4p/q4n, monp/monn. Independently controllable peakings and delays with an adjustable maximum value are provided in each channel.

The part's inputs and outputs support the CML logic interface with on chip 50*Ohm* or 55*Ohm* termination to vcc respectively, and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS.

In the input AC-coupling mode, the input termination provides the required common mode voltage automatically. In this case, the output can be used in DC-coupling mode and its common mode voltage can be adjusted using floating power supplies as described in the POWER SUPPLY CONFIGURATION section below.

Several operational features of the part including output amplitude, peaking/bandwidth, and delay can be controlled through on-chip SPI independently for each of the 5 outputs. The SPI message includes an address field that can activate up to three different chips identified by the voltage at their 3-state address pin addr_choff as shown in Table 1. If SPI is in its default state as defined below, then the output signal amplitude can be controlled jointly for all outputs by applying external voltage to the port VR. Also, several outputs can be disabled using the addr_choff pin as shown in Table 1.

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Table 1. Address Pin Configurations

Ext. voltage, *V*	Assigned chip #, SPI On="1"	Internal bits and corresponding output channels, SPI On="0"				
		Bit0/Ch1	Bit1/Ch2	Bit2/MON	Bit3/Ch3	Bit4/Ch4
vcc	2	"1"/OFF	"0"/ON	"0"/ON	"0"/ON	"1"/OFF
n/c	0	"0"/ON	"0"/ON	"0"/ON	"0"/ON	"0"/ON
vee	1	"0"/ON	"0"/ON	"1"/OFF	"0"/ON	"0"/ON

The on-chip 17-byte SPI block operates in slave mode. The SPI message consists of 18 bytes as shown in Fig. 2: 1 address byte (Byte #0 in Table 2) and 17 data bytes (Bytes #1-17 in Table 2). At the chip power-up, all 17 internal registers are preset to the initial state described in Table 2.

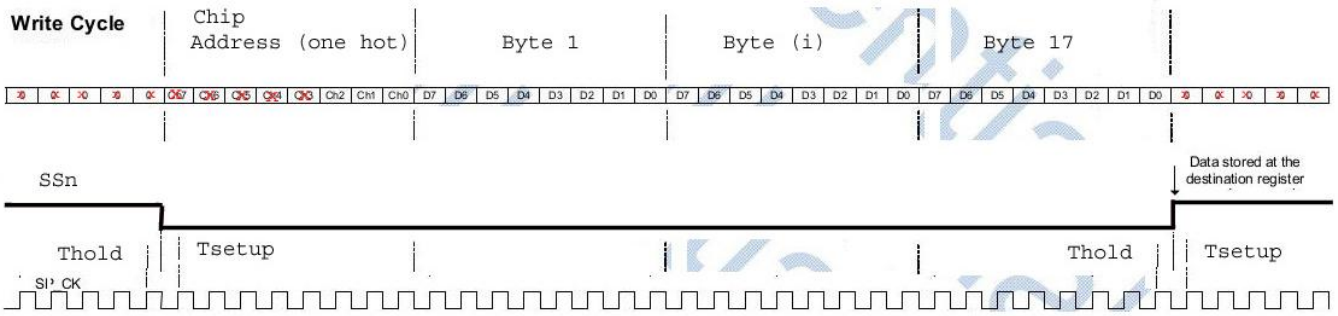

Fig. 2. SPI Message

Table 2. SPI Configuration

Byte #	Bit #	Bit function	Default state	Byte #	Bit #	Bit function	Default state	Byte #	Bit #	Bit function	Default state
0 (address) Write data into chip #	7	x		1	7		x	2	7	SPI "on"	0
	6	x			6		x		6		x
	5	x			5	Maximum delay control (less delay at higher numbers)	1		5		x
	4	x			4		1		4	Ch4 off	See Table 1
	3	x			3		1		3	Ch3 off	
	2	chip #2			2		0		2	MON off	
	1	chip #1			1		1		1	Ch2 off	
	0	chip #0			0		0		0	Ch1 off	
3	7	Ch. 1 delay control (higher delay at higher numbers)	1	4	7	Ch. 2 delay control (higher delay at higher numbers)	1	5	7	Mon delay control (higher delay at higher numbers)	1
	6		0		6		0		6		0
	5		0		5		0		5		0
	4		0		4		0		4		0
	3		0		3		0		3		0
	2		0		2		0		2		0
	1		0		1		0		1		0
	0		0		0		0		0		0
6	7	Ch. 3 delay control (higher delay at higher numbers)	1	7	7	Ch. 4 delay control (higher delay at higher numbers)	1	8	7	Ch. 1 amplitude control (higher amplitude at higher numbers)	1
	6		0		6		0		6		0
	5		0		5		0		5		0
	4		0		4		0		4		0
	3		0		3		0		3		0
	2		0		2		0		2		0
	1		0		1		0		1		0
	0		0		0		0		0		0

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9	7	Ch. 2 amplitude control (higher amplitude at higher numbers)	1	10	7	Mon amplitude control (higher amplitude at higher numbers)	1	11	7	Ch. 3 amplitude control (higher amplitude at higher numbers)	1
	6		0		6		0		6		0
	5		0		5		0		5		0
	4		0		4		0		4		0
	3		0		3		0		3		0
	2		0		2		0		2		0
	1		0		1		0		1		0
	0		0		0		0		0		0
12	7	Ch. 4 amplitude control (higher amplitude at higher numbers)	1	13	7	Ch. 1 peaking control (higher peaking at higher numbers)	1	14	7	Ch. 2 peaking control (higher peaking at higher numbers)	1
	6		0		6		1		6		1
	5		0		5		1		5		1
	4		0		4		1		4		1
	3		0		3		1		3		1
	2		0		2		1		2		1
	1		0		1		1		1		1
	0		0		0		1		0		1
15	7	Mon peaking control (higher peaking at higher numbers)	1	16	7	Ch. 3 peaking control (higher peaking at higher numbers)	1	17	7	Ch. 4 peaking control (higher peaking at higher numbers)	1
	6		1		6		1		6		1
	5		1		5		1		5		1
	4		1		4		1		4		1
	3		1		3		1		3		1
	2		1		2		1		2		1
	1		1		1		1		1		1
	0		1		0		1		0		1

POWER SUPPLY CONFIGURATION

The part operates with a floating supply configuration shown in Fig. 3. The part's output common mode voltage can be adjusted by modifying the voltage of the first power supply unit PSU1. This power supply unit defines the chip's positive supply voltage vcc. The second power supply unit PSU2 provides a floating negative supply voltage that defines the difference between the chip's supply voltages (vcc-vee). The second power supply unit can be replaced by a DC-DC converter.

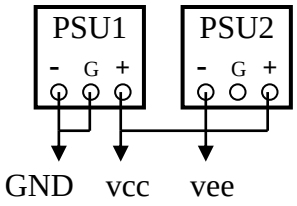

Fig. 3. Floating Supply Configuration

All the characteristics detailed below assume GND = 0.0*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Positive supply voltage (vcc)	0	3.6	*V*
Negative supply voltage (vee)	vcc-3.6	0	*V*
RF Input voltage swing (SE)		0.8	*V*
Case temperature		+105	*ºC*
Storage temperature	-40	+100	*ºC*
Operational/storage humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
d1p	27	CML input	Differential data/clock inputs with internal SE 50*Ohm* termination to vcc
d1n	28		
d2p	30	CML input	Differential data/clock inputs with internal SE 50*Ohm* termination to vcc
d2n	31		
q1p	23	CML output	Differential data outputs with internal SE 55*Ohm* termination to vcc. Require either external SE 55*Ohm* terminations to vcc, or differential 110*Ohm* termination.
q1n	22		
q2p	20		
q2n	19		
q3p	7		
q3n	6		
q4p	4		
q4n	3		
monp	15		
monn	14		
Low-Speed Control and SPI Ports			
addr_choff	10	Analog	DC control input with internal 90*KOhm* termination to vcc and 100*KOhm* termination to vee
VR	17	Analog	DC control input with internal 38*KOhm* termination to vcc
cs	9	Low voltage CMOS inputs	Chip select port with internal 568*KOhm* termination to vcc
Din	11		Data and Clock ports with internal 379*KOhm* termination to vcc and 284*KOhm* termination to vee
sck	12		

Supply and Termination Voltages		
Name	Description	Pin Number
vcc	Positive power supply	2, 5, 8, 13, 16, 18, 21, 24, 26, 29, 32
vee	Negative power supply	1, 25

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
General Parameters						
Positive supply voltage	vcc	0.9		1.6	*V*	*For SPI Mode (SPI on="1")*
		0		2.8	*V*	*For Hardwired Mode (SPI on="0")*
Negative supply voltage	vee	vcc-3.1	vcc-2.8	vcc-2.5	*V*	
Power consumption		365		1270	*mW*	*at 3.1V supply*
		330		1150	*mW*	*at 2.8V supply*
		310		1030	*mW*	*at 2.5V supply*
Junction temperature		-40		125	*°C*	
High-Speed Inputs						
Number of ports			2			*Differential*
On-chip termination	Rin		50		*Ohm*	*Each input pin to vcc*
Input resistance			100		*Ohm*	*Differential*
Data rate		DC		28	*Gbps*	*for PRBS-type input signal*
Clock Speed		DC		28	*GHz*	
Voltage swing	ΔV_{in}	50		400	*mV*	*pk-pk, each SE input pin*
Common mode level		vcc-0.4		vcc-$\Delta V_{in}/2$	*V*	
Input return loss	S11		TBD		*dB*	*in BW*
High-Speed Outputs						
Number of ports			5			*Differential*
On-chip termination	Rout		55		*Ohm*	*Each output pin to vcc*
Data rate at t_D=0		DC		32	*Gbps*	*PRBS eye opening >600mV*
		DC		36	*Gbps*	*PRBS eye opening >530mV*
Clock Speed at t_D=0		DC		32	*GHz*	
Propagation delay control range	t_D	110		120	*ps*	*Controlled from SPI; 8-bit DAC, for up to 14GHz*
Rise/Fall time	t_R/t_F	10		16	*ps*	
Jitter				2	*ps*	*Peak-to-peak, PRBS7 input*
Logic "1" voltage level	V^1		vcc		*V*	
Logic "0" voltage level	V^0	vcc-0.8		vcc-0.1		*For VR from Max to Min*
Voltage swing	ΔV_{out}	1600		200	*mV*	*Differential, pk-pk*
Latency	t_L		TBD		*ps*	*Packaged die*
Manual Amplitude Control Port (VR)						
Input voltage range		vcc-0.6	vcc-0.3	vcc	*V*	*Max output swing at or above vcc-0.3*
Address and Channel Control Port (addr_choff)						
Input voltage range		vee		vcc	*V*	
SPI Input Ports (cs, Din, sck)						
Input high voltage level	$V_{"1"}$	1.0		1.2	*V*	
Input low voltage level	$V_{"0"}$	0		0.1	*V*	
Clock frequency				10	*MHz*	

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PACKAGE INFORMATION

The flip-chip die is housed in a custom 32-pin LGA package shown in Fig. 4. The back side of the die is exposed at the top of the package to provide the heat dissipation path. An external heat sink can be attached to the exposed top.

The InfoCube part's identification label is IFC151. The Adsnatec part's identification label is ASNT5142-ALP. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

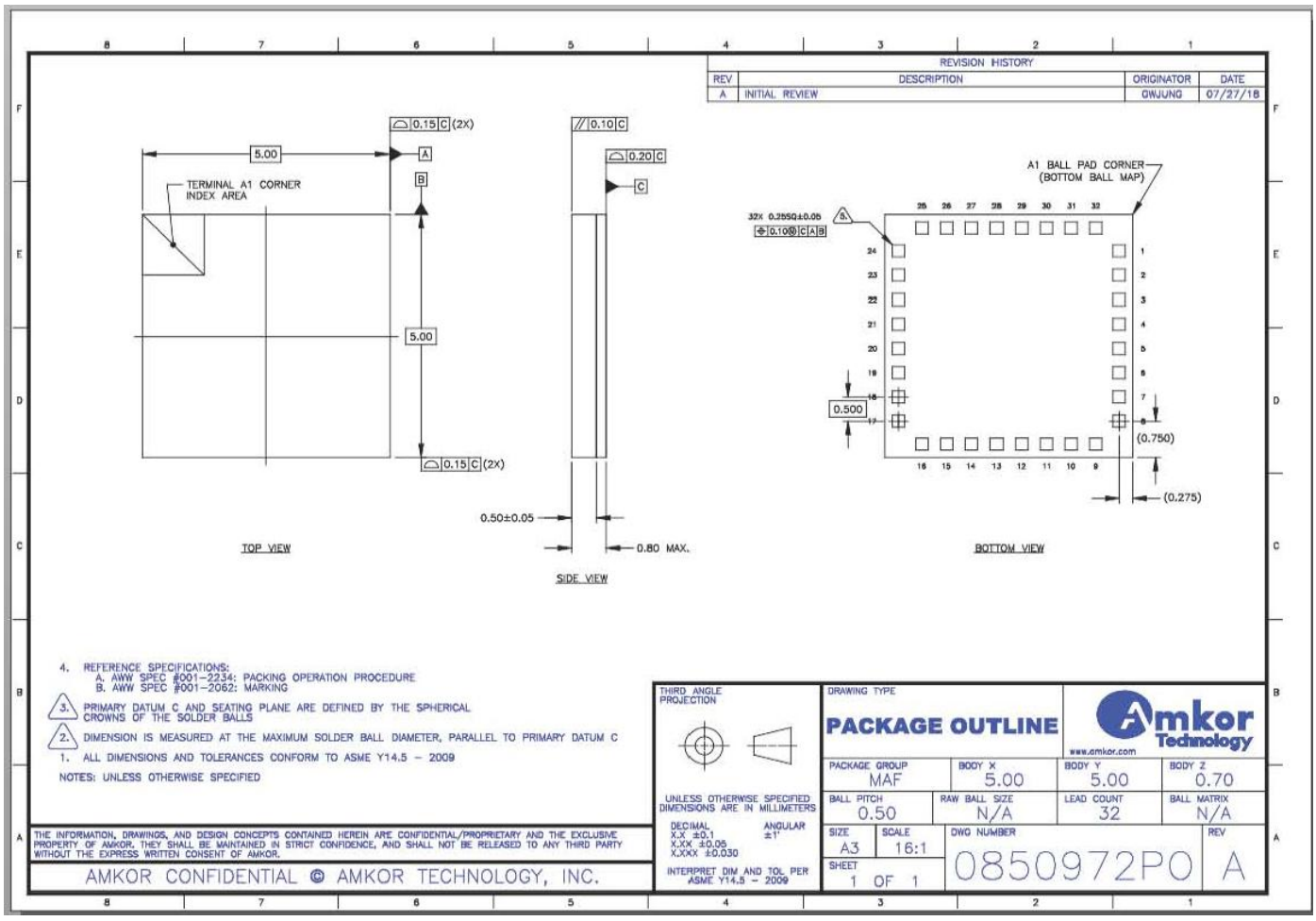

Fig. 4. LGA 32-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.6.2	01-2020	Updated clock speed
1.5.2	11-2019	Updated speed Corrected Header
1.4.1	02-2019	Corrected supply values
1.3.1	01-2019	Corrected ADSANTEC chip name Corrected electrical Specifications Added package drawing
1.2.1	11-2018	Corrected Table 1 Corrected Byte 2 in Table 2 Corrected Power Supply Configuration Corrected Absolute Maximum Ratings for vee Corrected Positive supply voltage in Electrical Characteristics
1.1.1	04-2018	Corrected pin out diagram Corrected pin number assignment Added SPI description
1.0.1	04-2018	Preliminary release.