ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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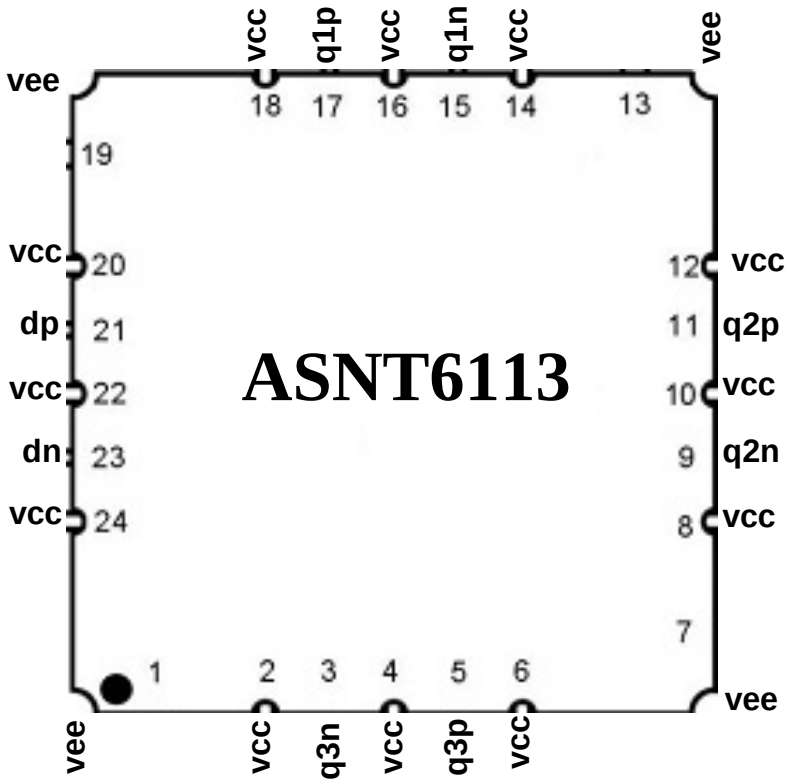
ASNT6113-KHC
DC-25*GHz* 1-to-3 Analog Signal Splitter

- DC to 25*GHz* broadband linear signal splitter
- One differential CML-type input port and three phase-matched differential CML-type output ports
- Differential input linearity range up to 1000*mV* p-p
- Differential gain of approximately 0*dB*
- Low jitter and limited temperature variation over industrial temperature range
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 1.0*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFN 24-pin package



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DESCRIPTION

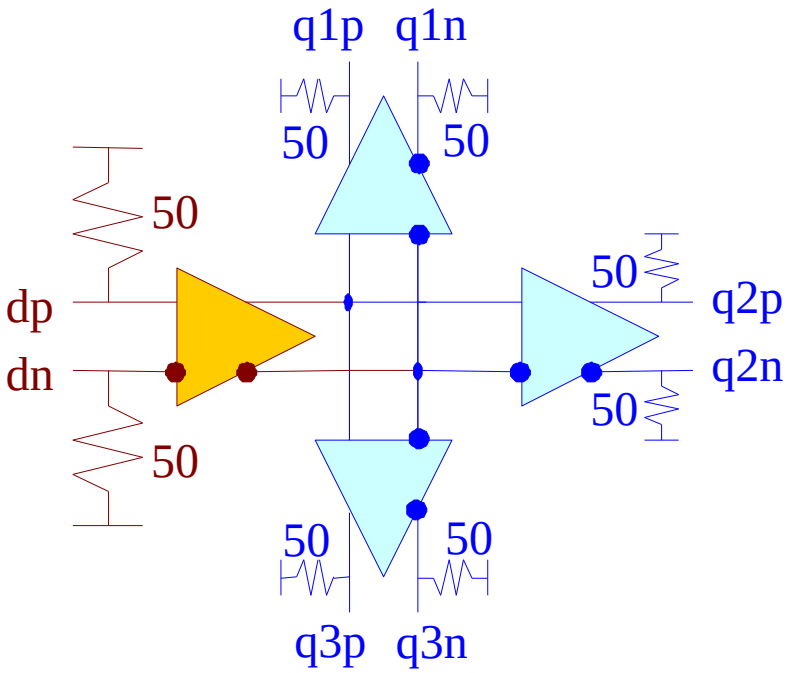

Fig. 1. Functional Block Diagram

The temperature stable ASNT6113-KHC 1-to-3 analog signal splitter is intended for use in high-speed interleaved ADCs or similar systems. The IC shown in Fig. 1 can receive a broad-band analog signal at its differential input dp/dn and effectively distribute it to three separate phase matched differential outputs q1p/q1n, q2p/q2n, q3p/q3n with a nominal gain of 0*dB*.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance. In particular, the specified output common-mode voltage level is guaranteed only in case of external single-ended 50*Ohm* DC termination to vcc.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.1	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTION

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
dp	21	CML input	Differential high speed data inputs with internal SE 50*Ohm* termination to vcc
dn	23		
q1p	17	CML output	Differential high speed data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
q1n	15		
q2p	11	CML output	
q2n	9		
q3p	5	CML output	
q3n	3		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)	1, 7, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		300		*mA*	
Power consumption		1000		*mW*	
Junction temperature	-25	50	125	*°C*	
Input Analog (dp/dn)					
Bandwidth	DC		25	*GHz*	-3*dB*
Common mode level	vcc-0.6	vcc-0.5	vcc-0.4	*mV*	
Input Noise Density		1.5		*nV*/sqrt*(Hz)*	
S11		-10		*dB*	DC to 30*GHz*
Output Analog (q1p/q1n, q2p/q2n, q3p/q3n)					
Common mode level		vcc-0.55		*V*	With external 50*Ohm* DC termination
S22		-8		*dB*	DC to 30*GHz*
Small Signal Differential Gain		0		*dB*	at 10*GHz*
Output referred 1*dB* Compression Point		2.7		*dBm*	Single-Ended, 20*GHz*
THD		0.2		*%*	

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFN package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6113-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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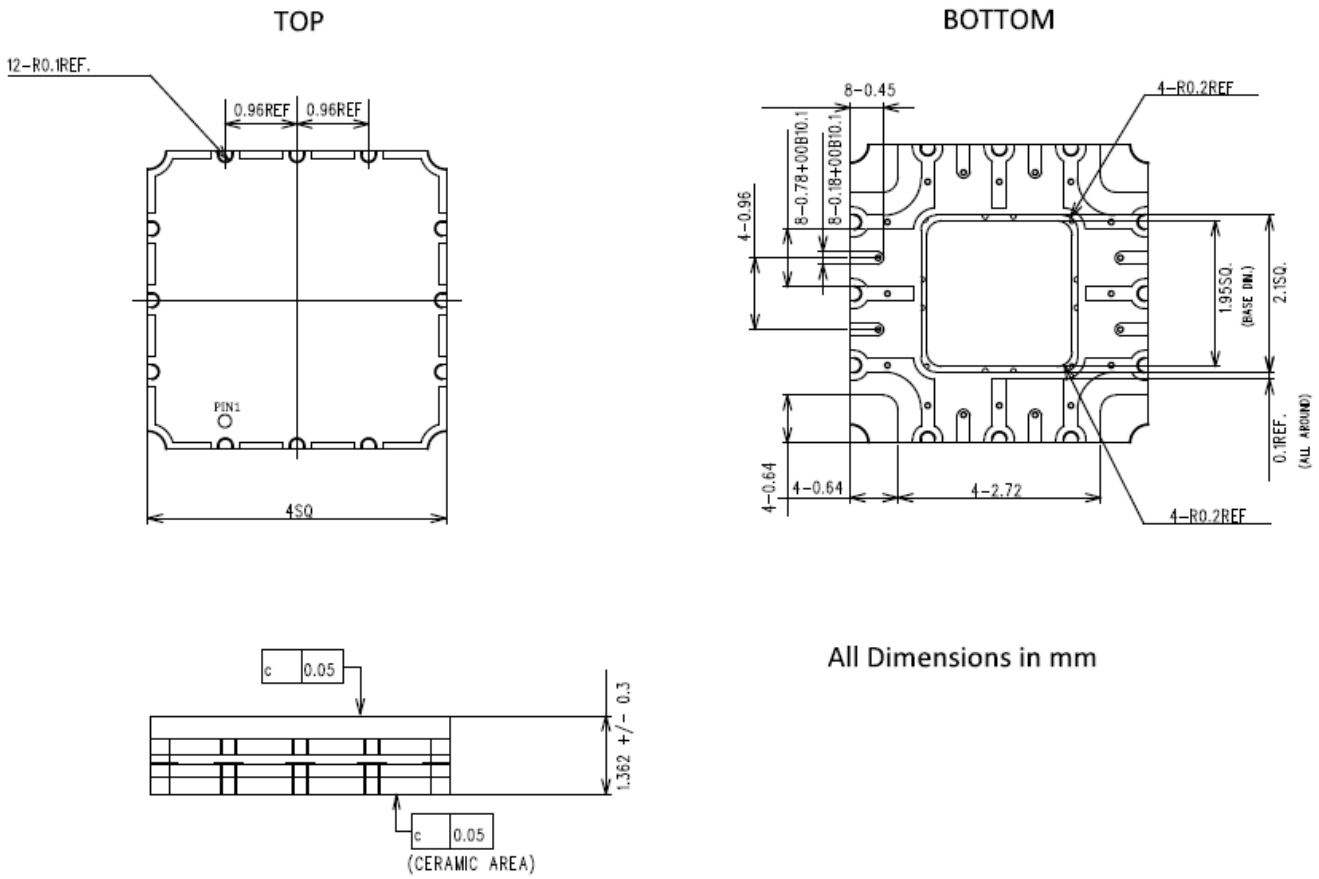

Fig. 2. CQFN24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.1.3	04-2023	Updated Package Drawing
1.1.2	08-2021	Updated RoHS Statement
1.0.2	04-2020	Updated Package information section
1.0.1	04-2020	First release