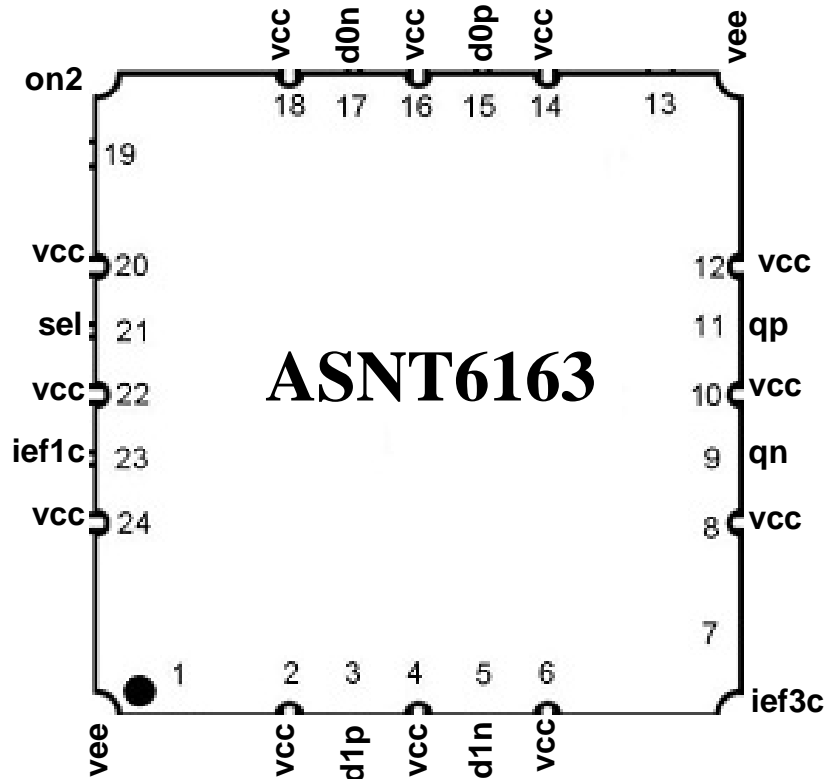# ASNT6163-KHC
## DC-32$GHz$ Analog Signal Selector 1-of-2

- DC to 32$GHz$ broadband operation

- Two differential CML-type input ports and one differential CML-type output port

- Temperature-stabilized differential gain of approximately 0$dB$

- 1$dB$ compression point of 0$dBm$

- DC-to-1G$Hz$ broadband channel selector port

- Optional two-channel mixer/adder setting available

- Low jitter and limited temperature variation over industrial temperature range

- Single +3.6$V$ or -3.6$V$ power supply

- Power consumption: 700$mW$

- Fabricated in SiGe for high performance, yield, and reliability
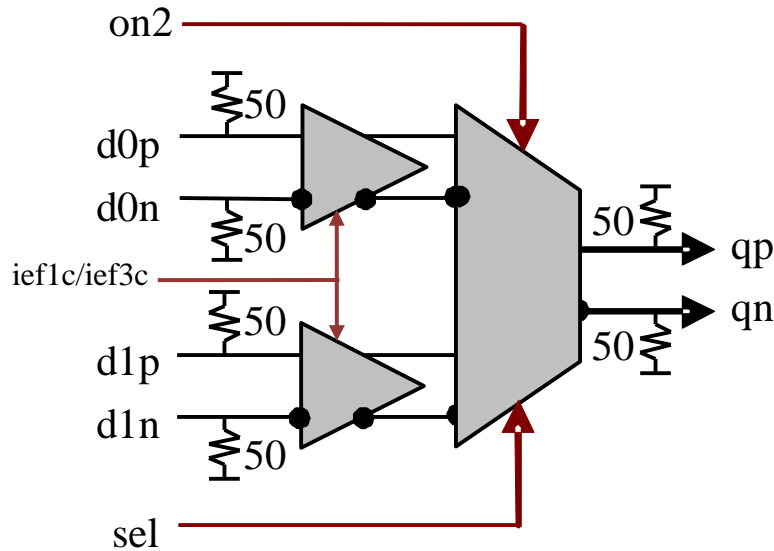
- Custom CQFN 24-pin package

# DESCRIPTION



*Fig. 1. Functional Block Diagram*

The temperature stable ASNT6163-KHC analog signal selector 1-of-2 is intended for use in high-speed systems. The IC shown in Fig. 1 can deliver one of two different broad-band analog differential signals d0p/d0n and d1p/d1n to its differential output qp/qn with a nominal gain of $0dB$. It can also be used as a two-channel analog mixer/adder of signals d0p/d0n and d1p/d1n. Two low-speed analog current controls lef1c and lef3c are available for bandwidth and peaking adjustments.

The active input selection is performed through the external high-speed single-ended port sel that can be referenced to either vcc or vee. When the low-speed single-ended control port on2 is set to vcc, it switches the circuit into mixer/adder mode with both inputs active at the same time.

The part's I/O's support the CML logic interface with on chip $50Ohm$ termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically.

# POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = $0.0V$ = ground and vee = $-3.6V$), or positive supply (vcc = $+3.6V$ and vee = $0.0V$ = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with $50Ohm$ termination to ground.

Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 0.0V = ground.**

# ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

*Table 1. Absolute Maximum Ratings*

| Parameter | Min | Max | Units |
|-----------|-----|-----|-------|
| Supply Voltage (vee) | | -4.0 | *V* |
| Power supply current | | 320 | *mA* |
| Input Voltage | vcc-1.2 | vcc+0.4 | *V* |
| RF Input Voltage Swing (SE) | | 0.6 | *V* |
| Case Temperature | | +90 | *ºC* |
| Storage Temperature | -40 | +100 | *ºC* |
| Operational Humidity | 10 | 98 | *%* |
| Storage Humidity | 10 | 98 | *%* |

# TERMINAL FUNCTION

| TERMINAL | | | DESCRIPTION |
|----------|----|----|-------------|
| Name | No. | Type | |
| **High-speed Signals** | | | |
| d0p | 15 | CML - type | Differential high speed data inputs with internal SE 50*Ohm* termination to vcc |
| d0n | 17 | | |
| d1p | 3 | CML - type | |
| d1n | 5 | | |
| qp | 11 | CML - type | Differential high speed data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc |
| qn | 9 | | |
| **Control Signals** | | | |
| sel | 21 | SE | High-speed high-impedance input (active: high, d1 is connected to q default: low, d0 is connected to q;) |
| ief1c | 23 | Analog Control | Analog current control with internal 64*KOhm* termination to vcc and 72*KOhm* termination to vee. |
| ief3c | 7 | | |
| on2 | 19 | CMOS | Low-speed high-impedance input (active: high, mixer/adder mode; default: low, 1-of-2 selector mode;) |
| **Supply and Termination Voltages** | | | |
| Name | Description | | Pin Number |
| vcc | Positive power supply rail | | 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24 |
| vee | Negative power supply rail | | 1, 13 |

# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| vee | -3.4 | -3.6 | -3.8 | V | ±5.5% |
| vcc | | 0.0 | | V | External ground |
| Ivee | | 200 | | mA | In Selector Mode |
| | | 280 | | mA | In Mixer/Adder Mode |
| Power consumption | | 700 | | mW | In Selector Mode |
| | | 1000 | | mW | In Mixer/Adder Mode |
| Junction temperature | -25 | 50 | 125 | °C | |
| **Input Analog (d0p/d0n, d1p/d1n)** | | | | | |
| Bandwidth | DC | | 32 | GHz | -3dB |
| Common mode level | | vcc | | mV | AC-coupled |
| Voltage swing, pk-pk | 0 | | 400 | mV | Single-ended, with unused input not connected or AC terminated |
| | 0 | | 800 | mV | Differential |
| S11 | | -35 | | dB | at 3GHz |
| | | -16 | | dB | at 10GHz |
| | | -11 | | dB | at 20GHz |
| | | -9 | | dB | at 25GHz |
| **Current Control Signals (ief1c/ief3c)** | | | | | |
| Control range | vee | | vcc | V | |
| Default voltage level | | vee+1.9 | | V | at ±3.6V supply |
| **Output Analog (qp/qn)** | | | | | |
| Bandwidth | DC | | 32 | GHz | -3dB |
| Common mode level | | vcc-0.55 | | V | With external 50Ohm DC termination |
| Small Signal Differential Gain | -1.5 | 0.0 | +1.5 | dB | up to 25GHz |
| Output referred 1dB Compression Point | | 1 | | dBm | Single-Ended, 20GHz |
| THD | | 0.5 | | % | at 1GHz |
| | | 0.6 | | % | at 10GHz |
| | | 1.9 | | % | at 25GHz |
| | | 2.5 | | % | at 35GHz |
| **Low-Speed Control (on2)** | | | | | |
| High logic level | | vcc | | V | Mixer/Adder Mode |
| Low logic level | | vee | | V | 1-of-2 Selector Mode |
| **High-Speed Control (sel)** | | | | | |
| Bandwidth | | 1 | | GHz | |
| High logic level | | vcc | | V | Input d1p/d1n is active |
| Low logic level | | vee | | V | Input d0p/d0n is active |
| Input current | | | 20 | uA | sink or source |

# PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFN package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation.  ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.
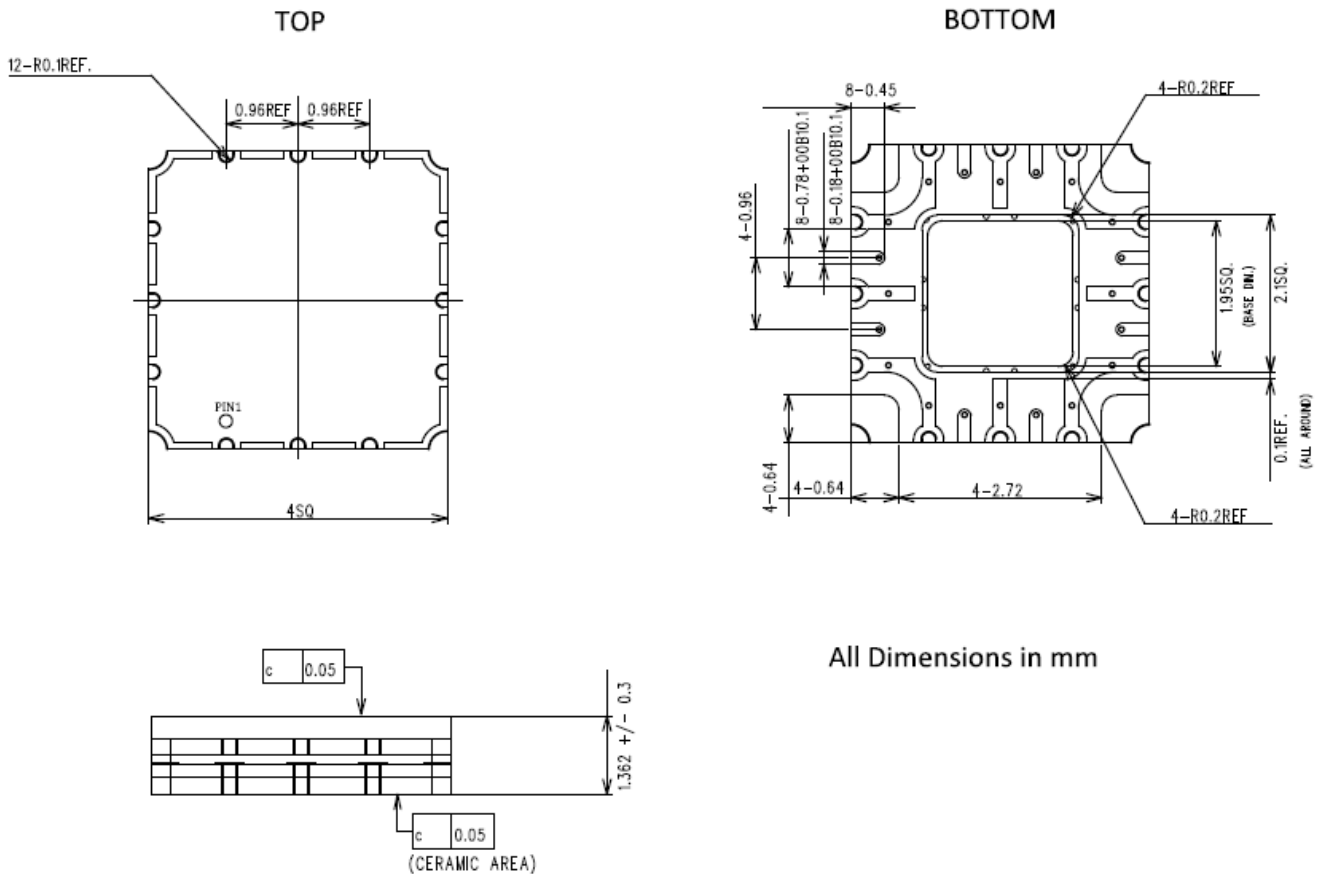


*Fig. 2. CQFN 24-Pin Package Drawing (All Dimensions in mm)*

The part's identification label is ASNT6163-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

# REVISION HISTORY

| Revision | Date | Changes |
|----------|---------|--------------------------|
| 1.2.2 | 08-2023 | Updated Maximum Ratings |
| 1.1.2 | 04-2023 | Updated Package Drawing |
| 1.0.2 | 06-2021 | First release |
| 0.0.2 | 12-2019 | Preliminary release |