ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
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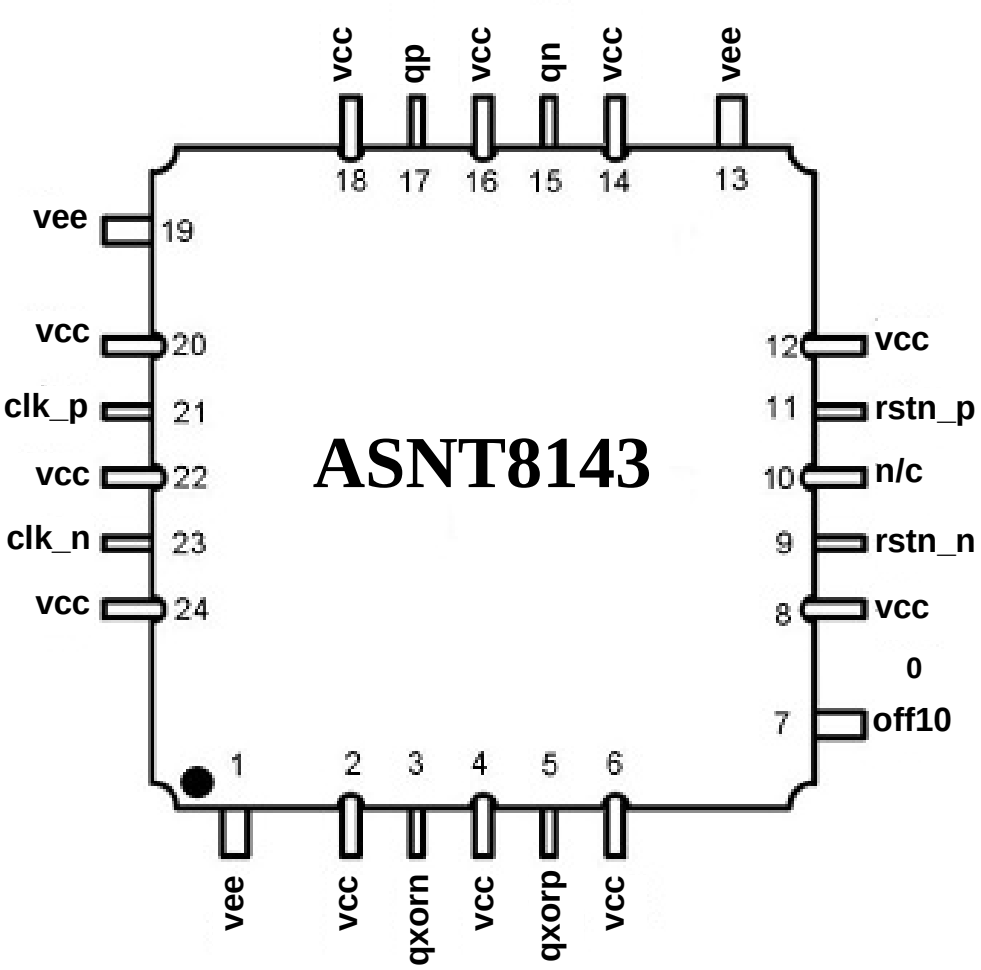
ASNT8143-KMC
Generator of DC-to-24*Gb/s* PRBS with Selectable Polynomials

- Full-length (2^9-1) or (2^{10}-1) pseudo-random binary sequence (PRBS) generator
- Selectable power of the Polynomial
- DC to 24*Gb/s* output data rate
- Additional output delayed by half of the sequence period
- Asynchronous reset signal for elimination of the “all zeros” initial state
- Fully differential CML input interface
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 805*mW*
- Custom CQFP 24-pin package



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DESCRIPTION

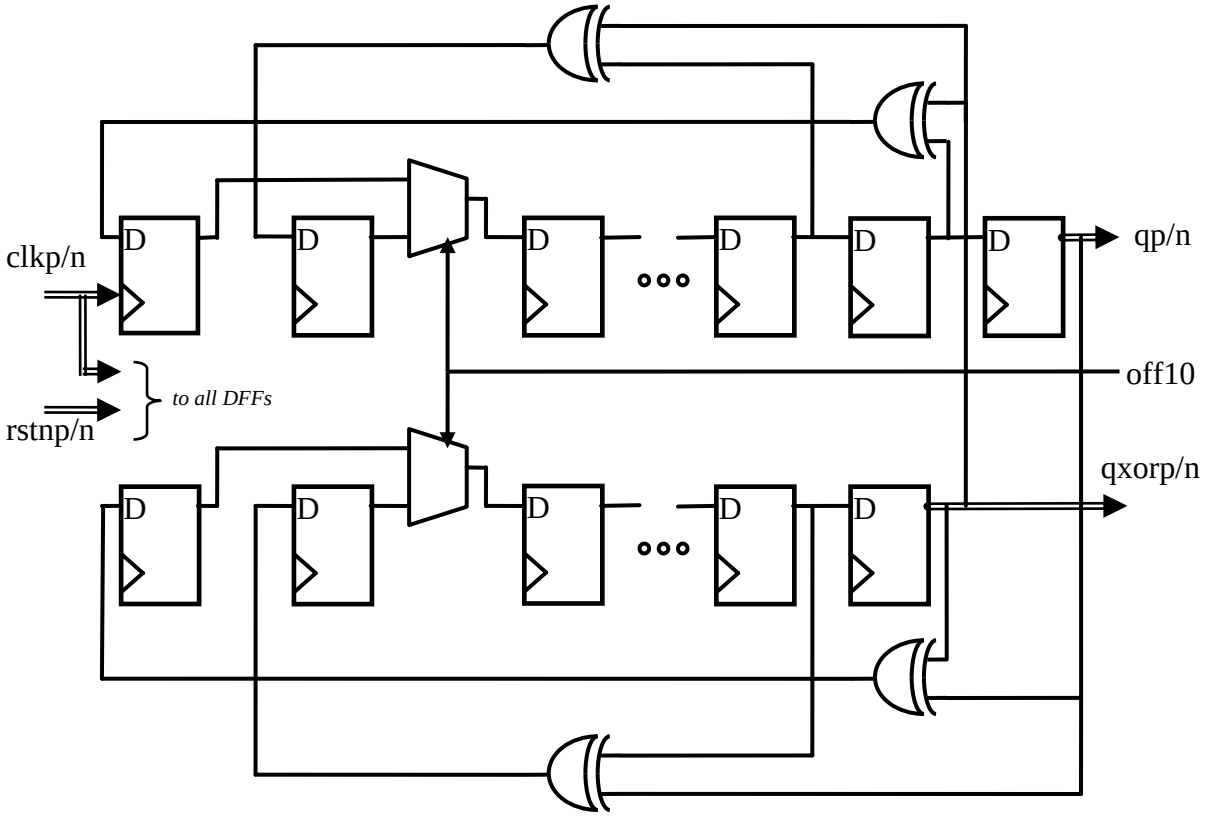

Fig. 1. Functional Block Diagram

The ASNT8143-KMC SiGe IC shown in Fig. 1 provides a selectable full 511-bit or 1023-bit long pseudo-random binary sequence (PRBS) signal according to either a $(x^9 + x^4 + 1)$, or a $(x^{10} + x^7 + 1)$ polynomial respectively, where x^D represents a delay of D clock cycles. This is implemented as a linear feedback shift register (LSFR) in which the outputs of either the ninth and fourth, or tenth and seventh flip-flops are combined together by an XOR function, and provided as an input to the first flip-flop of the register. The polynomial is selected through the external control signal off10.

The LSFR-based PRBS generator produces binary states, excluding the "all zeros" state that is illegal for the XOR-based configuration. To eliminate this state that locks the LSFR and prevents PRBS generation, an asynchronous external active-low preset signal rstnp/rstnn is implemented in the circuit. When the preset is asserted, LSFR is set to the All-"1" state that is enough for activation of the PRBS generation. When the preset is released, the chip delivers one consecutive bit of the PRBS signal to output pins qp/qn per each rising edge of clock clkp/clkn, starting from the state mentioned above.

An additional copy of the same PRBS signal delayed by half of the sequence period is delivered to pins qxorp/qxorn, and can be used to double the frequency of the output signal using an external multiplexer (e.g. ASNT5150 part) or XOR (e.g. ASNT5140 part) as shown in Fig. 2.

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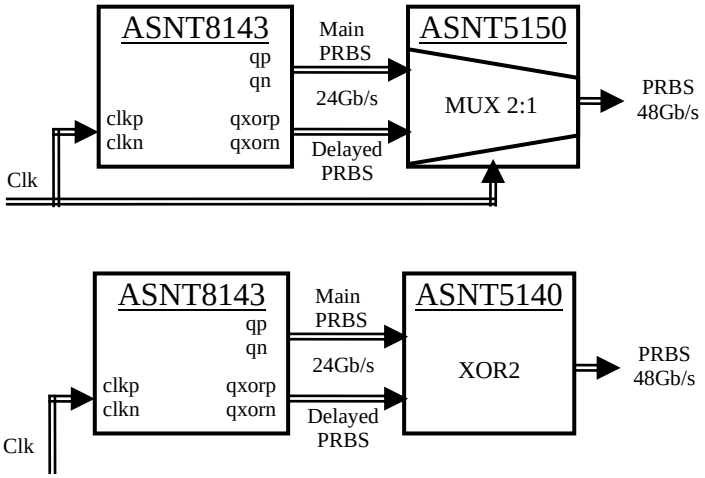

Fig. 2. PRBS Frequency Doubling

The simulated eyes for both signals are shown in Fig. 3.

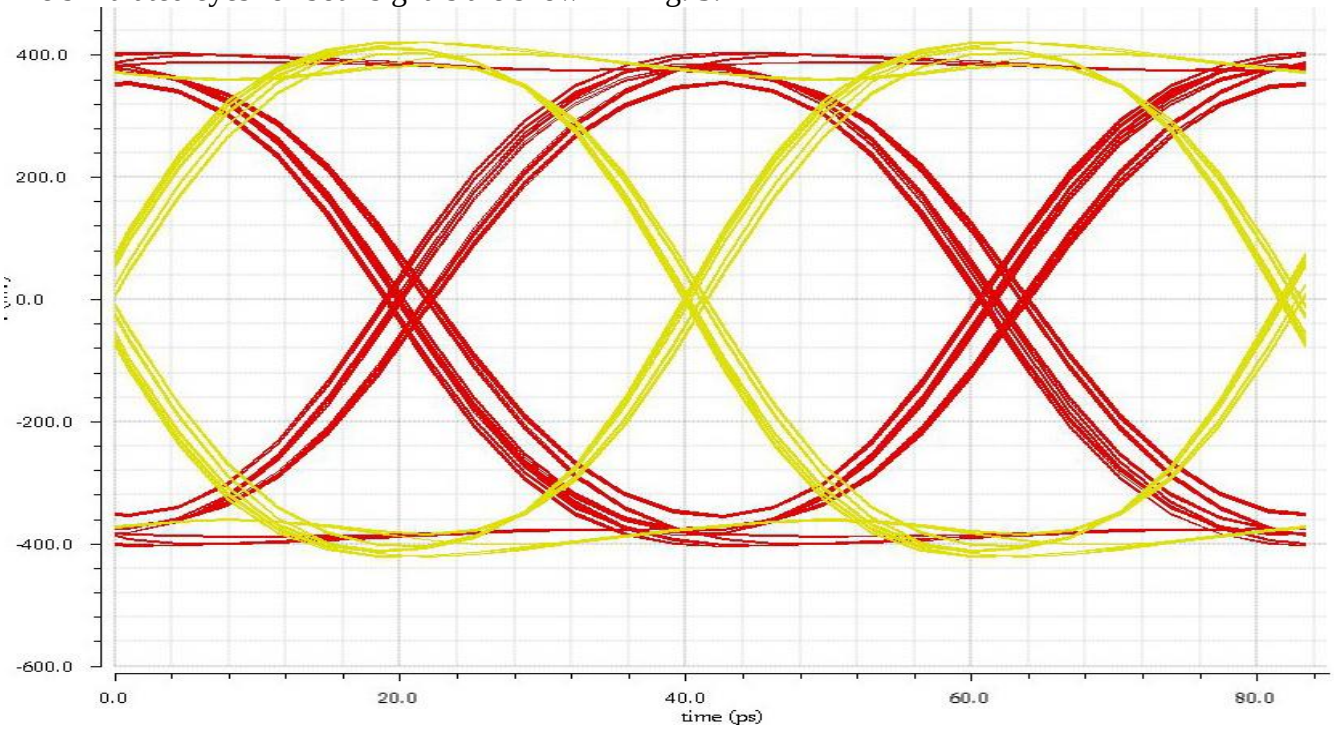

Fig. 3. 24Gbps PRBS Output Eye Diagram (Simulation, Slow Corner, 125°C)

All I/O stages are back terminated to vcc with on-chip 50*Ohms* resistors and may be used in either DC or AC coupling modes (see also POWER SUPPLY CONFIGURATION). In the first mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the second mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

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POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power supply current		350	*mA*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
rstn_p	11	CML input	Differential high-speed asynchronous reset (active low) inputs with internal SE 50*Ohms* termination to VCC
rstn_n	9		
clk_p	21	CML input	Differential clock input signals with internal 50*Ohms* termination to VCC
clk_n	23		
qp	17	CML output	Differential data outputs. Require external SE 50*Ohms* termination to VCC
qn	15		
qxorp	5	CML output	Differential delayed sequence data outputs. Require external SE 50*Ohms* termination to VCC
qxorn	3		
Control Signal			
off10	7	CMOS input	3.3V CMOS input with internal 1*MOhms* pull-up to VCC

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
Supply and Termination Voltages			
Name	**Description**		**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)		1, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee	218	244	277	*mA*	
Power consumption		805		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Clock (clkp/clkn)					
Frequency	DC		24	*GHz*	
Voltage swing, pk-pk	0.15		0.8	*V*	Single ended, unused input not connected or AC terminated
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Data (qp/qn, qxorp/qxorn)					
Voltage swing, pk-pk	280	440		*mV*	Single-ended
CM Voltage Level	vcc-0.8		vcc	*V*	
Output Jitter		2.5		*ps*	Peak-to-peak
Reset Signal (rstnp/rstnn)					
Frequency	DC		15	*GHz*	
Rise time			20	*%*	of the clock period
Recovery time	36			*ps*	
Voltage swing, pk-pk	0.05		0.8	*V*	Differential p-p
CM Voltage Level	vcc-0.8		vcc	*V*	
PRBS Select Signal (off15)					
High voltage level	vcc-0.4		vcc	*V*	
Low voltage level	vee		vee+0.4	*V*	Do not apply voltages below vee!

PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFP package shown in Fig. 4. The package's leads will be trimmed to a length of 1.0*mm*. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8143-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

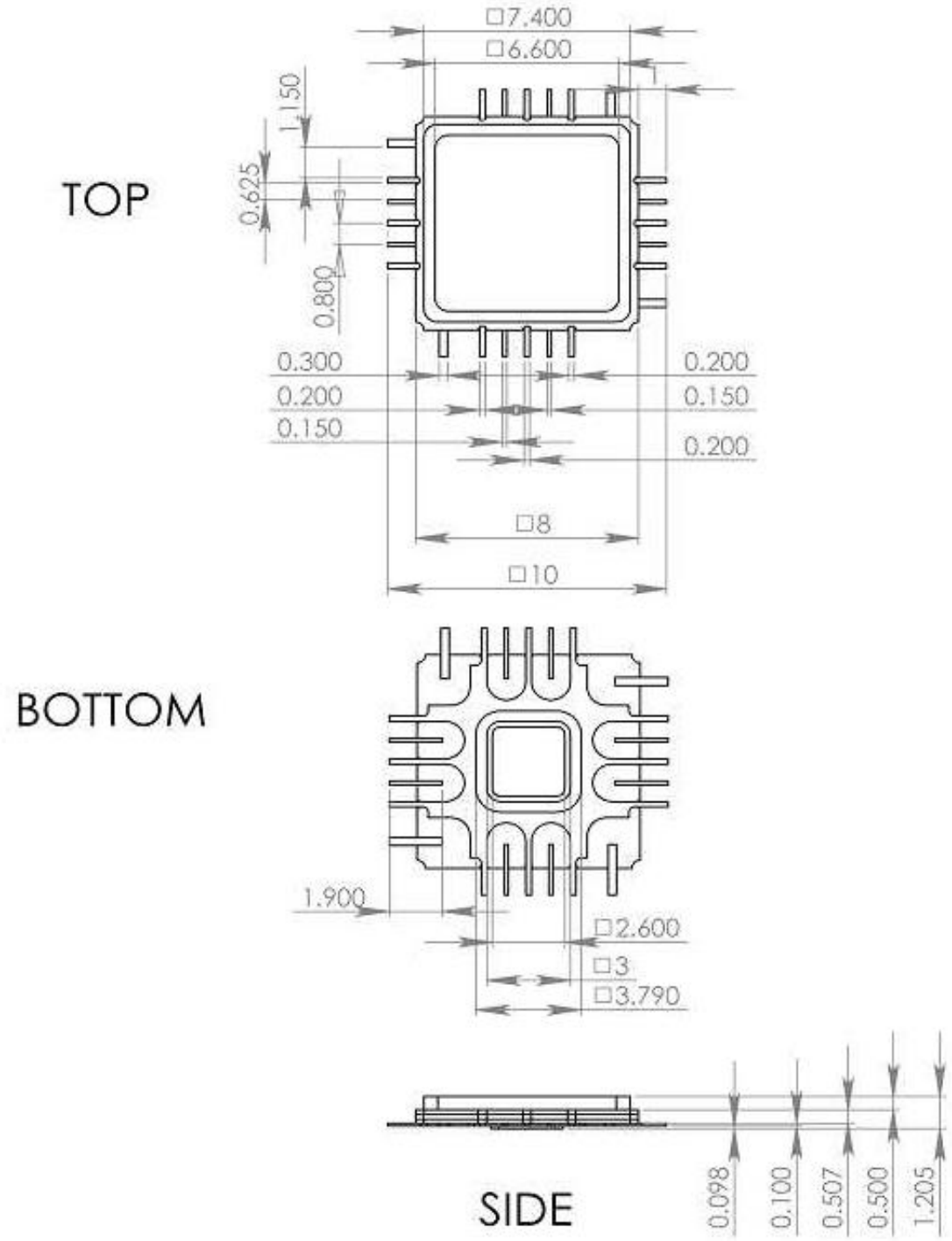

Fig. 4. CQFP 24-Pin Package Drawing (All Dimensions in mm)

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This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.1.2	11-2024	Updated Package Information
1.0.2	02-2020	Initial release
0.0.2	08-2019	Updated Letterhead
0.0.1	12-2018	Preliminary release