ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Dr., Ste #112, Torrance, CA 90505

Office: (310) 530-9400 Fax: (310) 530-9402
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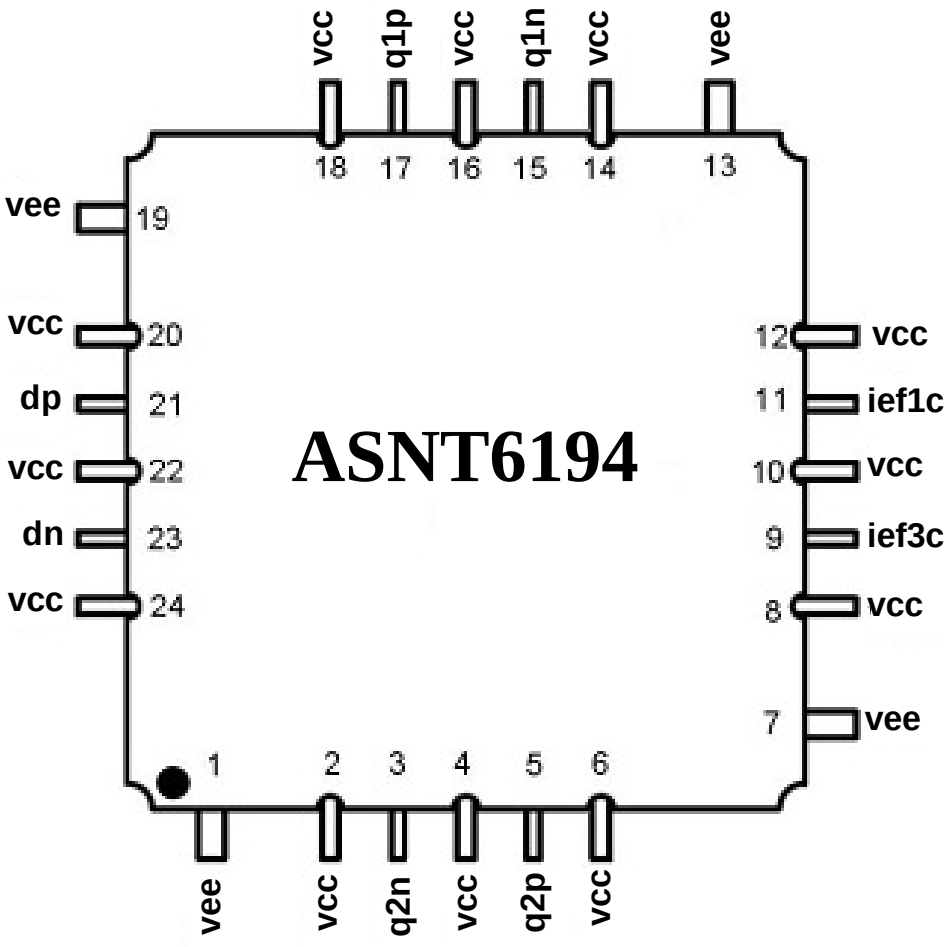
ASNT6194-KMC
DC-32*GHz* 1-to-2 Analog Signal Splitter

- DC to 32*GHz* broadband linear signal splitter
- One differential CML-type input port and two phase-matched differential CML-type output ports
- Differential input linearity range up to 1.4*V* p-p
- Differential gain of approximately 0*dB*
- Adjustable currents for bandwidth and peaking control
- Low jitter and limited temperature variation over industrial temperature range
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 760*mW* typical
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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DESCRIPTION

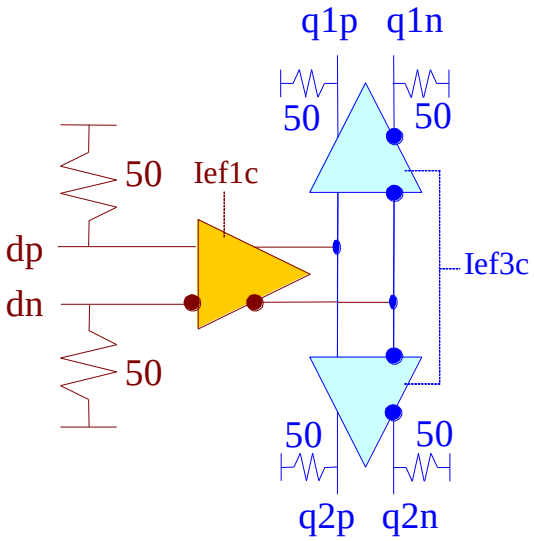

Fig. 1. Functional Block Diagram

The temperature stable ASNT6194-KMC 1-to-2 analog signal splitter is intended for use in high-speed interleaved ADCs or similar systems. The IC shown in Fig. 1 can receive a broad-band analog signal at its differential input dp/dn and effectively distribute it to two separate phase matched differential outputs q1p/q1n, q2p/q2n with a nominal gain of 0*dB*. Two low-speed analog current controls Ief1c and Ief3c are available for bandwidth and peaking adjustments. Both controls are very similar and change peaking of the part's frequency response at high frequencies (above 20*GHz*). Ief1c has a higher impact on the frequency response and also improves linearity at low control voltages. A relatively flat frequency response can be achieved at lower control voltages but it may be not the best setting for the signal eye. Typical S21 plot is shown in Fig. 2.

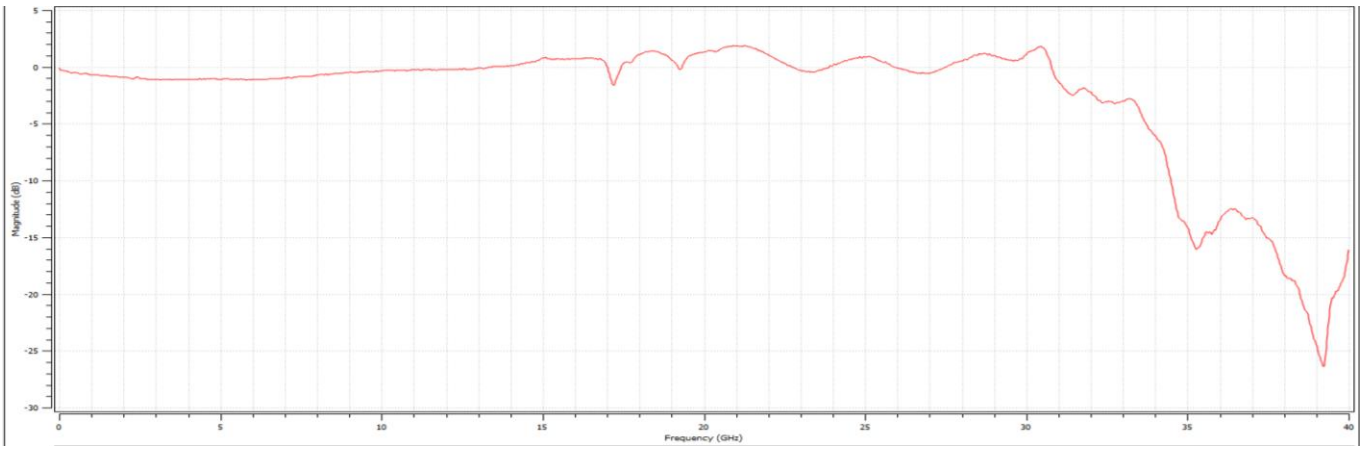

Fig. 2. Typical S21 Plot

The part's I/O's support the CML logic interface with on chip 50*Ohms* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply

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with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power supply current		300	*mA*
Input Voltage	vcc-1.0	vcc+0.4	*V*
RF Input Voltage Swing (SE)		0.8	*V*
Analog control voltages	vee	vcc	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTION

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
dp	21	CML input	Differential high speed data inputs with internal SE 50*Ohms* termination to vcc
dn	23		
q1p	17	CML output	Differential high speed data outputs with internal SE 50*Ohms* termination to vcc. Require external SE 50*Ohms* termination to vcc
q1n	15		
q2p	5	CML output	
q2n	3		
ief1c	11	Analog Control	Analog current control with internal 64*KOhms* termination to vcc and 72*KOhms* termination to vee.
ief3c	9		
Supply and Termination Voltages			
Name	**Description**		**Pin Number**

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vcc	Positive power supply (+3.3*V* or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)	1, 7, 13, 19

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee	180	230	250	*mA*	
Power consumption	560	760	825	*mW*	
Junction temperature	-25	50	125	*°C*	
Input Analog (dp/dn)					
Bandwidth	DC		32	*GHz*	-3*dB*
Common mode voltage level		vcc		*V*	Internally generated
Single ended voltage swing, pk-pk; unused input not connected or AC terminated			1400	*mV*	THD>41*dBm* at 1*GHz*
			1400	*mV*	THD>37*dBm* at 5*GHz*
			900	*mV*	THD>30*dBm* at 10*GHz*
Input Noise Density		1.5		*nV*/sqrt(*Hz*)	
S11		-35		*dB*	at 3*GHz*
		-16		*dB*	at 10*GHz*
		-11		*dB*	at 20*GHz*
		-9		*dB*	at 25*GHz*
Control Signals (ief1c/ief3c)					
Control range	vee+0.8		vee+1.8	*V*	
Default voltage level		vee+1.75		*V*	at ±3.3*V* supply
Output Analog (q1p/q1n, q2p/q2n)					
Common mode level		vcc-0.55		*V*	With external 50*Ohms* DC termination
Small Signal Differential Gain		0		*dB*	up to 10*GHz*
Gain flatness		±1.5		*dB*	Up to 24*GHz* and with optimal peaking control settings
Output referred 1*dB* Compression Point		1		*dBm*	Single-Ended, 20*GHz*
THD		0.3		*%*	at 1*GHz*, 0.8*V*
THD		0.4		*%*	at 10*GHz*, 0.8*V*
THD		0.9		*%*	at 25*GHz*, 0.8*V*
THD		3.5		*%*	at 35*GHz*, 0.8*V*

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PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFP package shown in Fig. 3. The package's leads will be trimmed to a length of 1.0*mm*. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

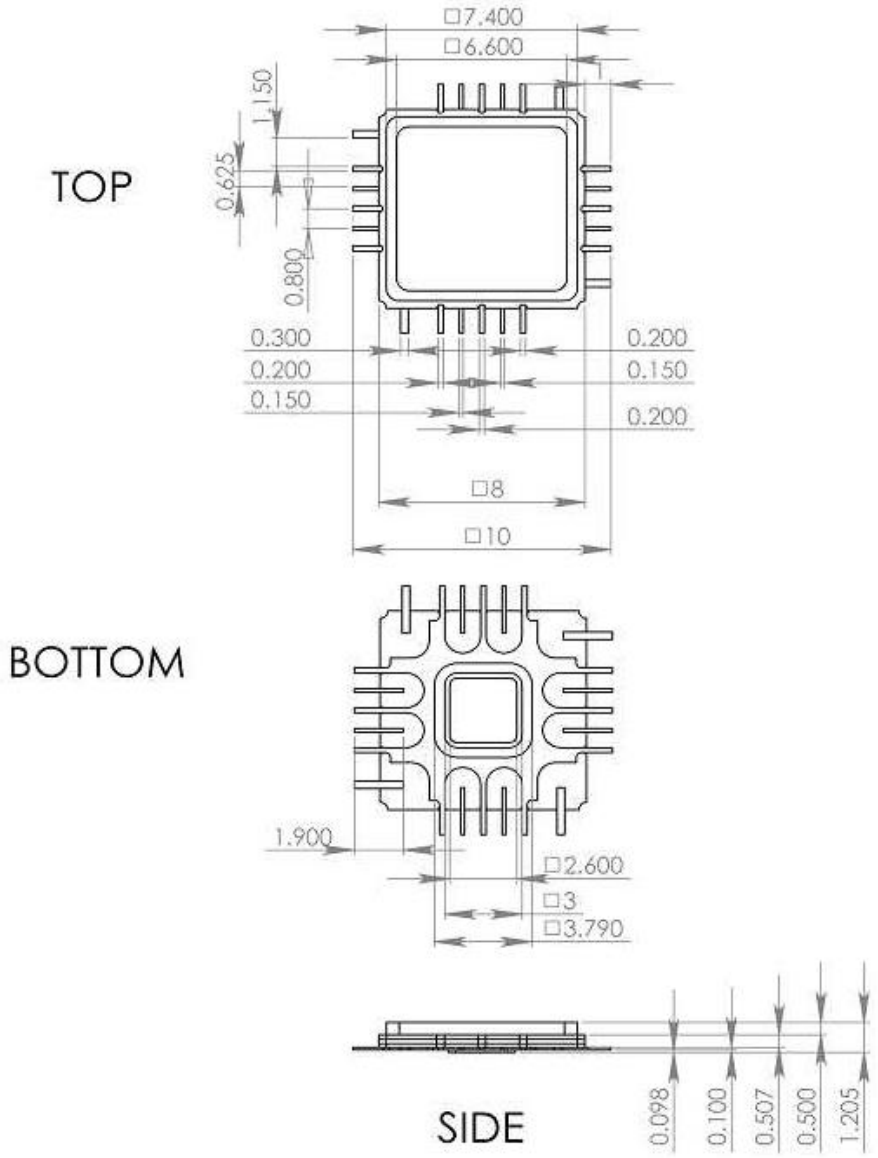

Fig. 3. CQFP 24-Pin Package Drawing (All Dimensions in mm)

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The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6194-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.7.2	11-2024	Updated Package Information
1.6.2	12-2021	Corrected Terminal Function table
1.5.2	06-2021	Corrected THD and input swing values Updated package information section
1.4.2	11-2019	Corrected input swing Corrected Absolute Maximum input swing
1.3.2	11-2019	Corrected range of analog controls Added description of analog controls Added maximum values of analog control voltages
1.2.2	10-2019	Added Gain Flatness specification
1.1.2	08-2019	Corrected pinout diagram
1.0.2	08-2019	First release Corrected title Corrected maximum speed S21 plot inserted Corrected current and power consumption Corrected Terminal Functions table
0.0.2	01-2019	Corrected header
0.0.1	01-2019	Preliminary release