ADSANTEC
Ultra High-Speed Mixed Signal ASICs
Advanced Science And Novel Technology Company, Inc.
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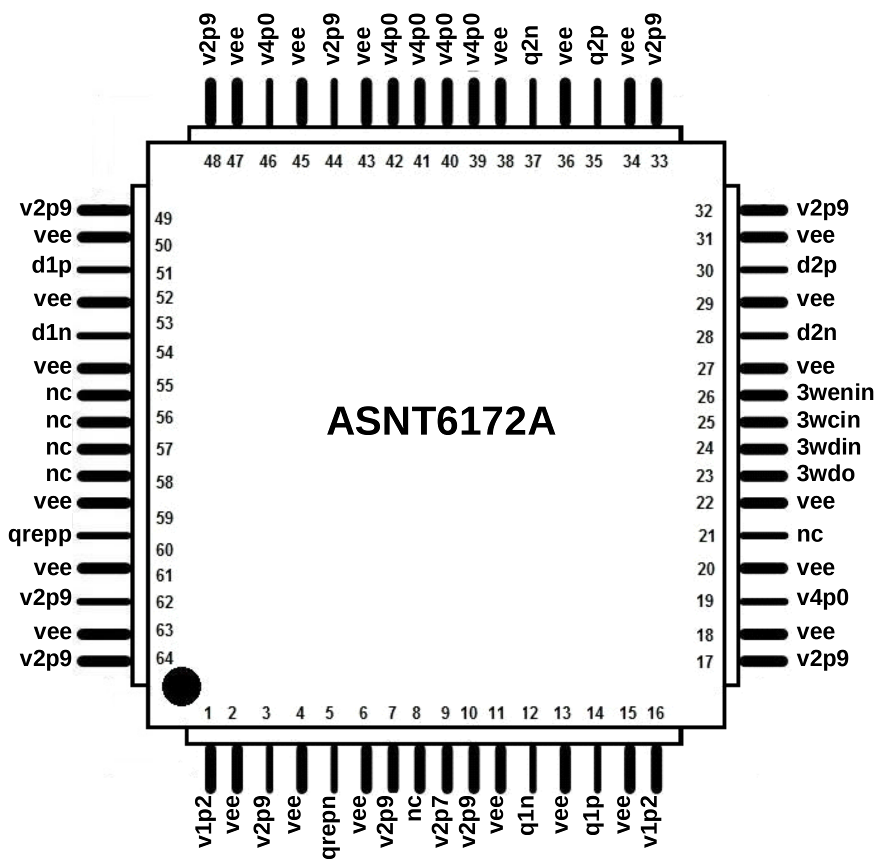
ASNT6172A-KMO
Asynchronous FIR Filter and 2x2 Analog Switch

- Dual FIR filter with 9 fully controlled taps for each input analog signal
- Fully differential CML-type analog input interfaces
- Two independent fully differential CML-type analog outputs
- Operates as an analog non-blocking 2x2 switch with a possibility to mix weighted input signals
- High bandwidth DC-28*Gbps* / 20*GHz*
- Total gain up to 6*dB*
- Dual-port 3-wire SPI for tap weight and sign adjustment
- Additional frequency response and gain adjustment through the SPI
- Independent power supplies for analog and digital sections
- Power consumption: <1.25*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 64-pin package



DESCRIPTION

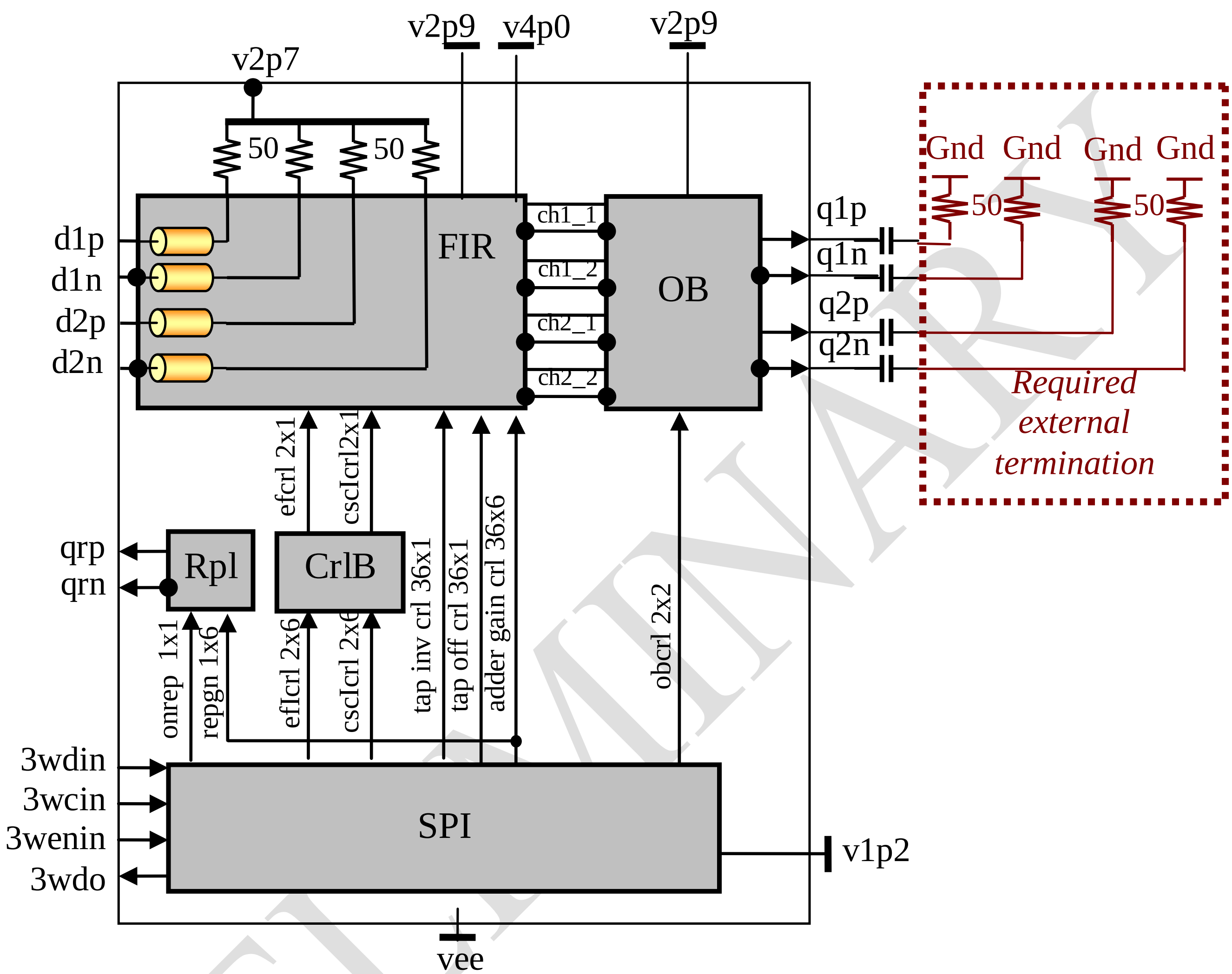


Fig. 1. Functional Block Diagram

The IC shown in Fig. 1 is a two-channel differential analog 9-tap FIR filter. It receives two high-speed analog signals through its differential input ports d1p/d1n and d2p/d2n. Each channel of FIR has 9 dual taps. Each tap provides two copies of its input signal with controlled polarities. The signals are then processed by analog adders with controlled weight coefficients to perform the pre-emphasis operation. The resulting 4 analog signals (the first and the second signals from the first and the second channels) are sent to the output buffer block that converts them into two output analog signals delivered to linear differential ports out1p/out1n and out2p/out2n. The first output port presents either individual first signal from any channel, or a sum of both first signals. It can be also completely disabled. The second output port presents the second signals from both channels with the same operational modes. Both ports operate in CML-type mode and require external 50*Ohm* terminations.

All chip functions are controlled by internal digital signals delivered through a 3-wire serial-to-parallel interface (SPI) that operates in combination with an internal control block CrlB.

The chip includes a 1-tap replica Rpl that can be independently enabled and used for initial gain calibration as described below.

FIR

The FIR consists of two identical channels. At the input of each channel there is a differential transmission line that includes 10 identical sections connected in series to provide ten equal delays. The connection nodes of the sections serve as inputs for 9 taps. The ends of the last section have internal 50*Ohm* terminations to a separate internally generated power supply v2p7. The last section is required for achievement of matching conditions for all taps.

Each tap includes a pair of dual buffers (buf1 and buf2) which allows for generation of two copies of the tap's input signal with polarities individually selected by 1-bit binary signals chX_inv1 and chX_inv2, where "0" corresponds to a direct output signal and "1" corresponds to an inverted output signal. Dual buffers in each tap can be individually disabled by special 1-bit binary signals chX_off1="0" or chX_off2="0". The buffers of different taps have slightly different gains and internal peaking in order to compensate for transmission line losses.

The 9 pairs of delayed copies of the differential input signal with set polarities are then processed by two 2-stage adders in order to create two linear sums of weighted tap signals. The first stage of each adder consists of three 3-to-1 adders and combines 9 input signals into 3 intermediate signals. The second stage combines those intermediate signals into 1 output signal. Identical 3-to-1 analog adders with digital controls of each input's weight are used in both stages. The control circuitry of the 3-to-1 adder is designed in such a way that the combined weight of all 3 inputs does not exceed the maximum weight of one tap. The control circuitry receives three 6-bit binary signals: the first weight chX_gncYZ1, the second weight chX_gncYZ2, and the maximum possible weight chX_gnmxY, and converts them into another three 6-bit binary signals that control the actual weights of all three inputs. Here X is the channel number 1 or 2; Z is the 2-stage adder number 1 or 2; and Y is the 3-to-1 adder number 1, 2, 3, or 0, where the adders 1, 2, and 3 represent the first stage and the adder 0 represents the second stage. The corresponding algorithm is detailed in Table 1.

Table 1. Wight Control Algorithm

Input number	Control signal	Formula	Condition
1	chX_crlYZ1	chX_gncYZ1	if chX_gncYZ1≤ chX_gnmxY
		chX_gnmxY	if chX_gncYZ1> chX_gnmxY
2	chX_crlYZ2	chX_gncYZ2	if R1=(chX_gnmxY- chX_gncYZ1)>0 and ichX_gncYZ2≤ R1
		R1	if R1>0 and chX_gncYZ2>R1
		0	if R1 ≤0
3	chX_crlYZ3	R1-chX_gncYZ2	if R1>0 and R2=R1-chX_gncYZ2>0
		0	if R1≤0 or R2≤0

The maximum weight can be adjusted depending on the fabrication process corner. The required value of the maximum weight is defined during initial calibration. The calibration is performed using a replica block Rpl that is described below.

Each tap can be enabled/disabled and its weight and polarity are defined by internal binary signals set through SPI that is also described below.

OB

The output buffer (OB) takes two pairs of analog signals from the two FIR channels (ch1_out1, ch1_out2, ch2_out1, and ch2_out2) and delivers them to the two output ports q1p/q1n and q2p/q2n as defined by 2-bit binary control signals obcrl1<1:0> and obcrl2<1:0> according to Table 2. Here X is the channel number 1 or 2.

Table 2. Output Buffer Operational Modes

obcrlX<1>	obcrlX<0>	qX
0	0	Output disabled
0	1	ch1_outX
1	0	ch2_outX
1	1	0.5*(ch1_outX)+0.5*(ch2_outX)

CrlB

The control block (CrlB) converts binary signals from SPI into analog voltages that control internal peaking and linearity parameters of FIR channels. The peaking can be adjusted by 6-bit binary signals chX_ief<5:0> where higher values corresponding to higher bandwidth with associated high-frequency peaking of the channel's frequency response. The linearity can be adjusted by 6-bit binary signals chX_icsc<5:0> where higher values correspond to higher linearity at low weights.

Rpl

The tap replica (Rpl) is used for initial tap gain calibration to ensure the optimal maximum data signal swing at the outputs of the first stages of both adders.

Rpl is an exact copy of Tap1. In the optimal state, it should generate a predefined DC voltage difference between its outputs qrp and qrn. This difference should be adjusted to the value specified in ELECTRICAL CHARACTERISTICS using the 6-bit binary signal ch1_gnmx1. Rpl is used for initial calibration only and can be completely disabled by the binary signal onrep="0".

SPI

The 3-wire SPI operates in slave mode and accepts three CMOS signals: 3wenin (SSn), 3wcin (SCLK), and 3wdin (MOSI) as described in ELECTRICAL CHARACTERISTICS. Additional CMOS data output 3wdout (MISO) is provided for control purposes.

SPI converts 40 input serial bytes into 115 parallel binary control signals. The SPI byte description is presented in Table 3.

Table 3. SPI Control Bytes

SPI Section	**Byte Number**	**Bit Number**							
		7 (MSB for Left)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (MSB for Right)**
Left	1	onrep	X	ch1_gnmx1					
	2	obcrl1		ch1_gnmx0					
	3	ch1_off1(1)	ch1_inv1(1)	ch1_gnc111					
	4	ch1_off1(2)	ch1_ inv1(2)	ch1_ gnc112					
	5	ch1_off1(3)	ch1_ inv1(3)	ch1_gnc121					
	6	ch1_off1(4)	ch1_ inv1(4)	ch1_ gnc122					
	7	ch1_off1(5)	ch1_ inv1(5)	ch1_gnc211					
	8	ch1_off1(6)	ch1_ inv1(6)	ch1_ gnc212					
	9	ch1_off1(7)	ch1_ inv1(7)	ch1_gnc221					
	10	ch1_off1(8)	ch1_ inv1(8)	ch1_ gnc222					
	11	ch1_off1(9)	ch1_ inv1(9)	ch1_gnc311					
	12	ch1_off2(1)	ch1_ inv2(1)	ch1_ gnc312					
	13	ch1_off2(2)	ch1_ inv2(2)	ch1_gnc321					
	14	ch1_off2(3)	ch1_ inv2(3)	ch1_ gnc322					
	15	ch1_off2(4)	ch1_ inv2(4)	ch1_gnc011					
	16	ch1_off2(5)	ch1_ inv2(5)	ch1_ gnc012					
	17	ch1_off2(6)	ch1_ inv2(6)	ch1_gnc021					
	18	ch1_off2(7)	ch1_ inv2(7)	ch1_ gnc022					
	19	ch1_off2(8)	ch1_ inv2(8)	ch1_ef1 (DAC)					
	20	ch1_off2(9)	ch1_ inv2(9)	ch1_csc (DAC)					
	21	X	X	ch1_ef2 (DAC)					
Right	22	ch2_ef2 (DAC) (reversed bit order)						X	X
	23	ch2_csc (DAC) (reversed bit order)						ch2_ inv2(9)	ch2_off2(9)
	24	ch2_ef1 (DAC) (reversed bit order)						ch2_ inv2(8)	ch2_off2(8)
	25	ch2_ gnc022 (reversed bit order)						ch2_ inv2(7)	ch2_off2(7)
	26	ch2_gnc021 (reversed bit order)						ch2_ inv2(6)	ch2_off2(6)
	27	ch2_ gnc012 (reversed bit order)						ch2_ inv2(5)	ch2_off2(5)
	28	ch2_gnc011 (reversed bit order)						ch2_ inv2(4)	ch2_off2(4)
	29	ch2_ gnc322 (reversed bit order)						ch2_ inv2(3)	ch2_off2(3)
	30	ch2_gnc321 (reversed bit order)						ch2_ inv2(2)	ch2_off2(2)
	31	ch2_ gnc312 (reversed bit order)						ch2_ inv2(1)	ch2_off2(1)
	32	ch2_gnc311 (reversed bit order)						ch2_ inv1(9)	ch2_off1(9)
	33	ch2_ gnc222 (reversed bit order)						ch2_ inv1(8)	ch2_off1(8)
	34	ch2_gnc221 (reversed bit order)						ch2_ inv1(7)	ch2_off1(7)
	35	ch2_ gnc212 (reversed bit order)						ch2_ inv1(6)	ch2_off1(6)
	36	ch2_gnc211 (reversed bit order)						ch2_ inv1(5)	ch2_off1(5)
	37	ch2_ gnc122 (reversed bit order)						ch2_ inv1(4)	ch2_off1(4)
	38	ch2_gnc121 (reversed bit order)						ch2_ inv1(3)	ch2_off1(3)
	39	ch2_ gnc112 (reversed bit order)						ch2_ inv1(2)	ch2_off1(2)
	40	ch2_gnc111 (reversed bit order)						ch2_inv1(1)	ch2_off1(1)
	41	ch2_gnmx0 (reversed bit order)						obcrl2 (reversed bit order)	
	42	ch2_gnmx1 (reversed bit order)						X	X

The bytes are delivered starting from 1 to 40 and bits within a byte are delivered starting from MSB. Bit#7 is the MSB of a byte as shown in Fig. 2. Internal registers are updated at a rising edge of 3wenin.

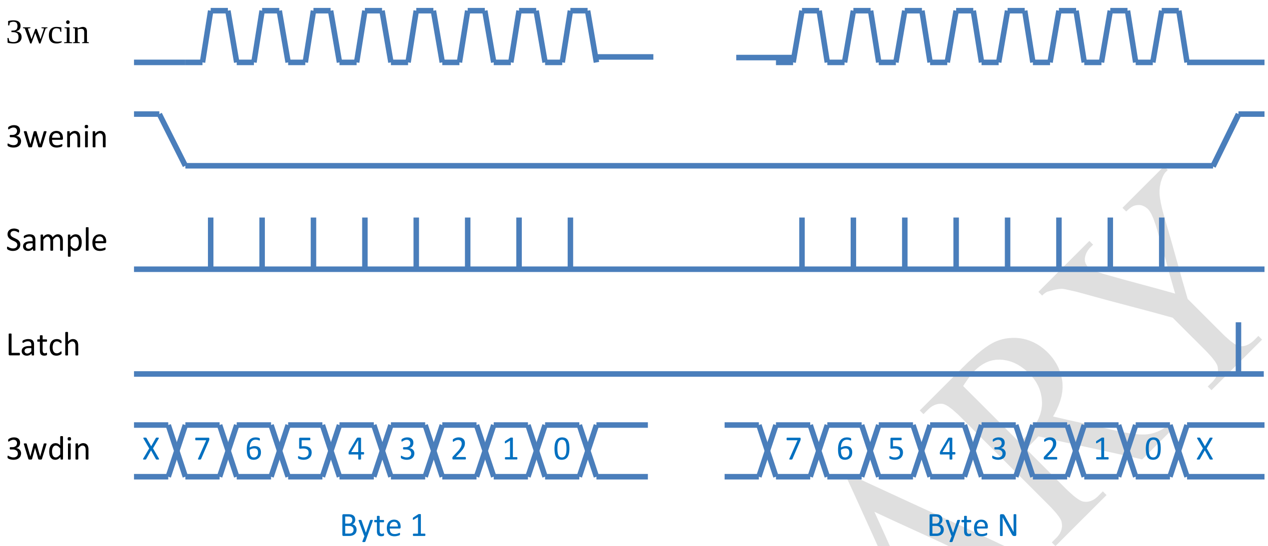


Fig. 2. SPI Operation

POWER SUPPLY CONFIGURATION

The IC requires three positive external power supplies. The first supply v2p9 is used for the data output terminations and to power all high-speed circuitry and reference sources. The second supply v4p0 powers the internal analog adder circuitry. The digital supply v1p2 is used for the internal CMOS circuits of the SPI.

All supplies are positive in relation to the internal common node vee=0.0*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (v4p0)		+4.4	*V*
Supply Voltage (v2p9, v2p7)		+3.6	*V*
Supply Voltage (v1p2)		+1.5	*V*
RF Input Voltage Swing (SE)		0.5	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			Description
Name	**No.**	**Type**	
High-Speed I/Os			
d1p	51	CML-type input	Differential high-speed data inputs with internal SE 50*Ohm* terminations to v2p9
d1n	53		
d2p	30	CML-type input	
d2n	28		
q1p	14	CML-type output	Differential high-speed data outputs with internal SE 50*Ohm* terminations to v2p9; require external SE 50*Ohm* terminations to v2p9.
q1n	12		
q2p	35	CML-type output	
q2n	37		
Low-Speed I/Os			
3wenin	26	1.2*V* CMOS input	Enable input signal SSn for 3-wire interface
3wcin	25		Clock input signal SCLK for 3-wire interface
3wdin	24		Data input signal MOSI for 3-wire interface
3wdout	23	1.2*V* CMOS output	Data output signal MISO for 3-wire interface
Analog Control Voltages			
v2p7	9	Internal voltage generator output	Internal voltage source of v2p9-0.2*V*
Analog Control Nodes (for DMM measurements only!)			
qrepp	60	Analog DC output	Replica differential data outputs
qrepn	5		

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vee	External ground	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 50, 52, 54, 59, 61, 63
v2p9	Positive power supply	3, 7, 10, 17, 32, 33, 44, 48, 49, 62, 64
v4p0	Positive power supply	19, 39, 40, 41, 42, 46
v1p2	Positive power supply	1, 16
nc	not connected pins	8, 21, 55, 56, 57, 58

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
v2p9		2.9		*V*	Analog supply
v4p0		4.0		*V*	Analog supply
vdd		1.2		*V*	CMOS digital supply
vee		0.0		*V*	External ground
*I*v2p9		400		*mA*	All taps enabled, maximum peaking
		175		*mA*	3 equivalent taps in each channel
*I*v4p0		180	215	*mA*	Depending on bandwidth control settings
Power consumption		1.25	2.1	*W*	
Junction temperature	-25	50	125	*°C*	
FIR Parameters					
No. of Taps		2x2x9			
Delay between Taps		13.5		*ps*	
Voltage gain		6		*dB*	From chip input to chip output
High Speed Input Data (d1p/d1n, d2p/d2n)					
Data Rate	DC		28	*Gb/s*	
Swing in linear mode		110		*mV*	Differential or SE, p-p
S11		TBD		*dB*	
CM Voltage Level		v2p7-0.2		*V*	Must match for both inputs
Analog Output Data (q1p/q1n, q2p/q2n)					
Bandwidth	DC		20	*GHz*	
Swing		220		*mV*	At each SE output
S22		TBD		*dB*	
CM Voltage Level		2.5		*V*	
DC Control Voltages					
qrp-qrn		220		*mV*	With optimal ch1_gnmx1
3-Wire Interface Ports					
Clock frequency			6	*MHz*	
Low logic level		0		*V*	
High logic level		1.2		*V*	

PACKAGE INFORMATION

The chip die is housed in a custom, 64-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vee plain, which is ground for a positive supply.

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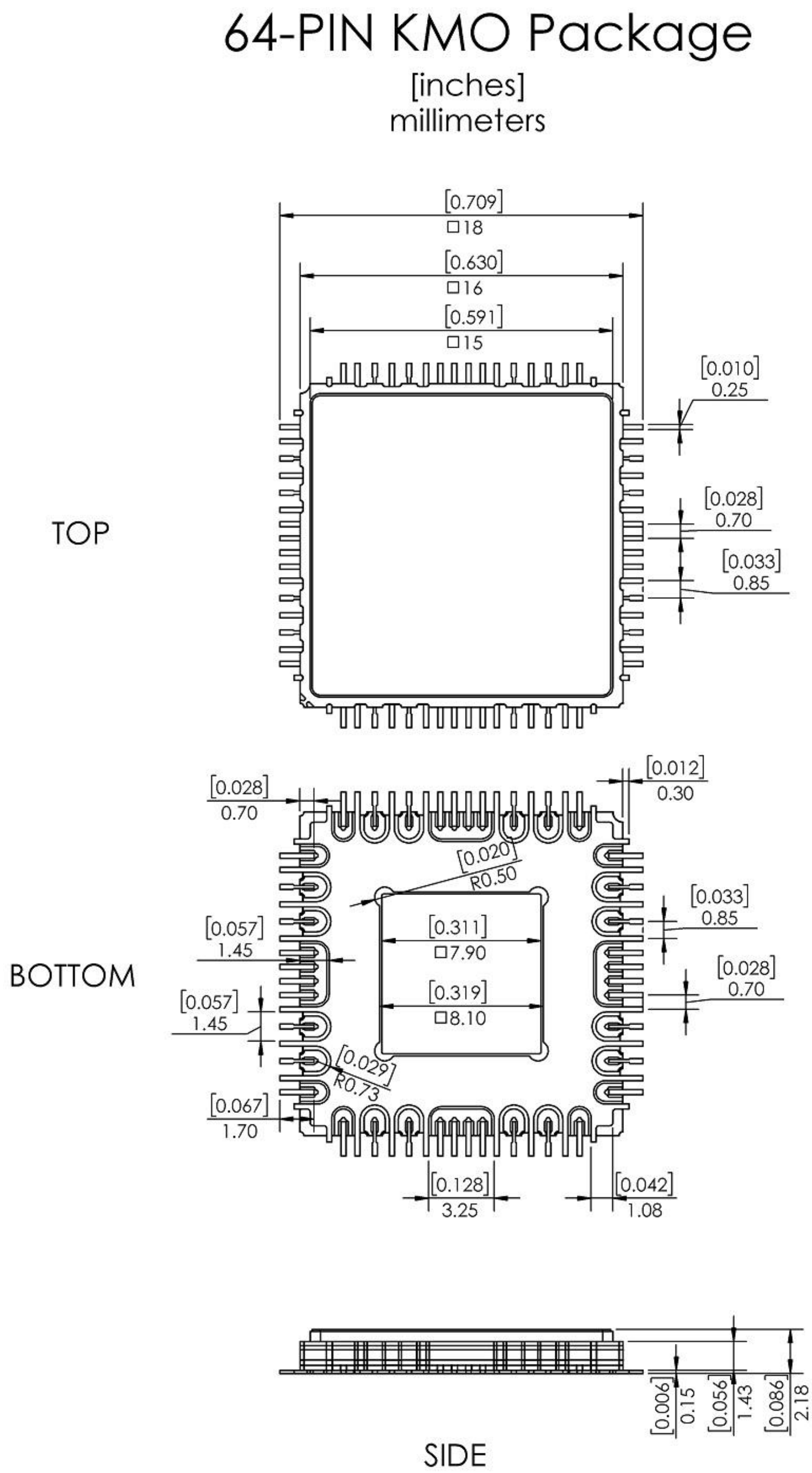

Fig. 3. CQFP 64-Pin Package Drawing (All Dimensions in mm)

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The part's identification label is ASNT6172A-KMO. The first 9 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
0.2.2	12-2020	Corrected pin out drawing Corrected Terminal Functions table Corrected SPI byte table Updated package information
0.1.2	01-2020	Updated Package Information
0.0.1	08-2019	Preliminary release