Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

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ASNT2113_EV
High-Speed Burst-Mode CDR Filter

- Recoverable clock frequency range is from 6*GHz* to 30*GHz*
- Input data up to 30*Gbps*
- Short synchronization time
- 50% duty cycle of output clock
- Adjustable phase of output clock
- Single negative -3.3*V* supply
- Low output clock phase noise

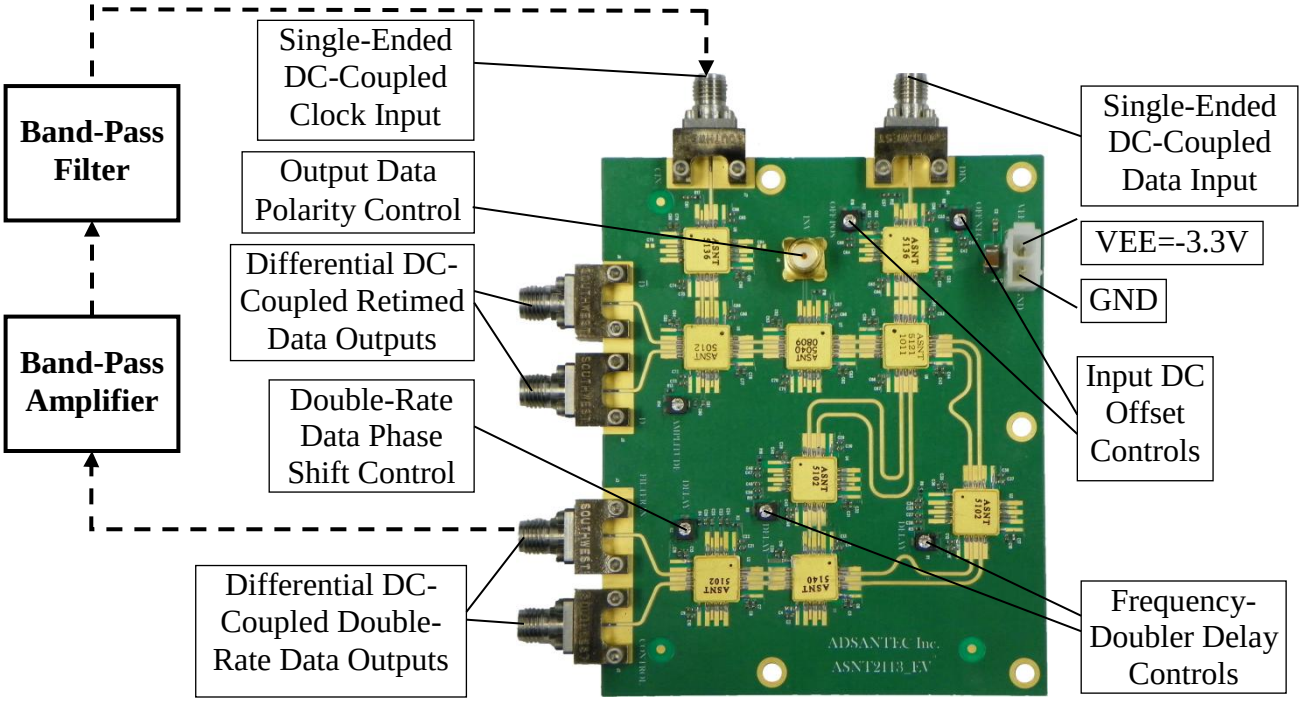

Fig. 1. PCB Layout

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DESCRIPTION

The ASNT2113_EV Burst-Mode CDR Filter shown in Fig. 1 is a narrow-band CDR for testing, prototyping, and communication applications. It is designed to work with an external narrow band-pass amplifier, and filter to recover the clock frequency. There are two single-ended inputs: the input data signal, and the recovered clock which is fed back to the board through an external band-pass Amplifier and Filter. There are two differential outputs: the multiplied double-rate data, and the retimed input data. All inputs and outputs are DC-coupled CML-type signals. High-speed Southwest connectors (MFG PN: 1092-03A-5) are installed for all inputs and outputs. The polarity of the retimed output signal can be reversed through an SMA connector. Phase shifters can be controlled manually via on-board potentiometers. Power is supplied through a two-pin MOLEX connector P/N: 39-28-1023.

Functional Block Diagram

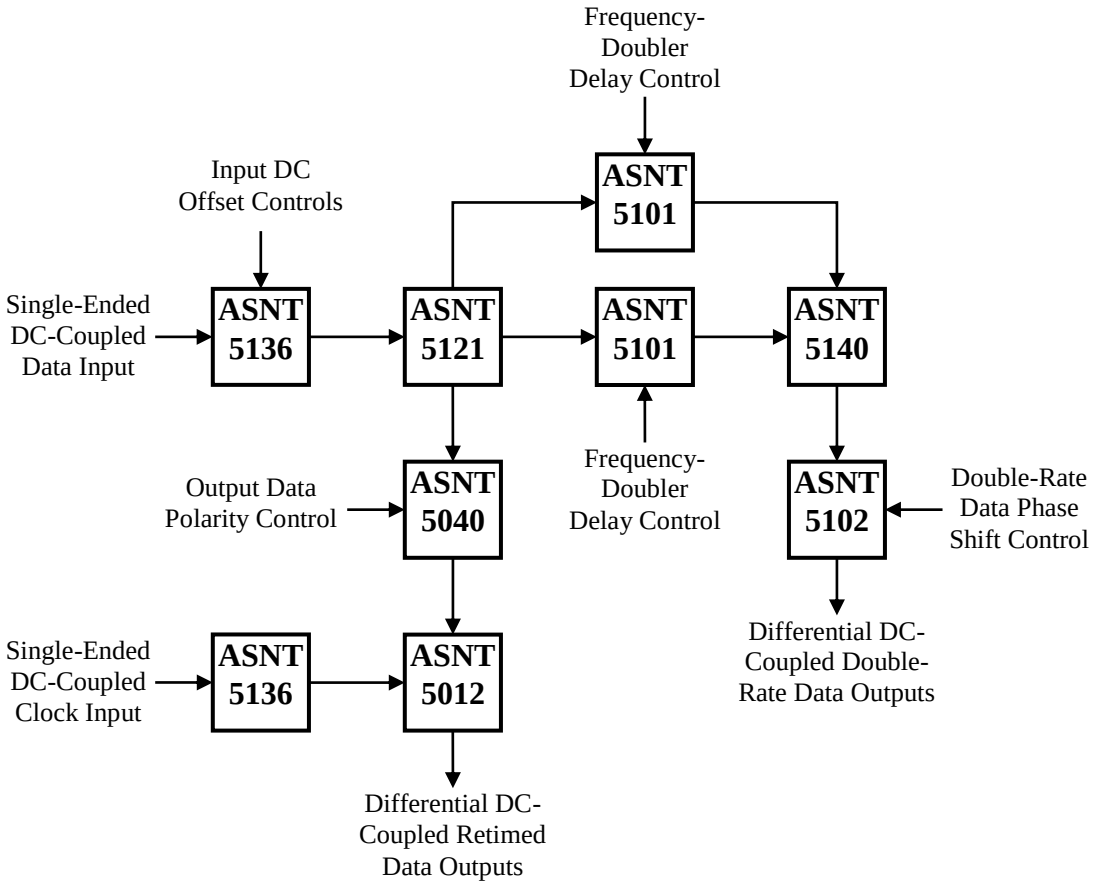

Fig. 2. Functional Block Diagram

The input data signal is amplified and split into three paths via ASNT5136 and ASNT5121. The data signal's delay is then adjusted by two phase shifters ASNT5101 to double its frequency in the XOR gate ASNT5140. An additional phase shifter ASNT5102 is placed after the XOR gate. Then, the output signal is amplified and band-pass filtered off the board to isolate the highest harmonic component. The isolated

harmonic is used as the recovered clock to retime the input data signal in the D-Type Flip-Flop ASNT5012. The synchronization time of this system is less than 2*ns*.

Frequency-Doubler Delay Controls

The variable phase shift of two ASNT5101 may be adjusted from 0*ps* to 80*ps* by tuning their adjacent potentiometers. The optimal relative delay of two ASNT5101 phase shifters guarantees correct operation of the ASNT5140 XOR frequency-doubler.

Double-Rate Data Phase Shift Control

The variable phase shift of the output ASNT5102 may be adjusted from 0*ps* to 80*ps* by tuning its adjacent potentiometer. This may be necessary to guarantee optimal retiming of the input data in the ASNT5012 D-Type Flip-Flop.

Output Data Polarity Control

The polarity of the retimed output data may be reversed by applying -1*V* to the Output Data Polarity Control SMA connector.

Input DC Offset Control

The DC offset (common mode) of the single-ended input signal may be adjusted by tuning two potentiometers adjacent to ASNT5136. This allows shifting the internal threshold between the rails of the input signal.

Applications

The ASNT2113_EV can be used as a high-speed CDR with short synchronization times, which is ideal for high-speed testing. If the differential double-rate data output is used as a single-ended signal, the second output can also be filtered to synchronize other devices or as an oscilloscope trigger.

POWER SUPPLY CONFIGURATION

The part operates with a negative supply (vcc = 0.0*V*=ground)

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

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Table 1. Absolute Maximum Ratings.

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.7	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		1680		*mA*	
Power consumption		5540		*mW*	
Synchronization time		2		*ns*	< 2*ns*
Frequency-doubler delay range	0		80	*ps*	
Junction temperature	-25	50	125	*°C*	
Input Data (DIN)					
Bandwidth	6		30	*Gbps*	
Input common mode	N/A – see comments				**Must be AC-Coupled**
Swing	10	200	500	*mV*	Single-Ended, p-p
Input Clock (CIN)					
Bandwidth	6		30	*GHz*	
Input Common Mode	N/A – see comments				**Must be AC-Coupled**
Swing	10	200	500	*mV*	SE, p-p
Output Double-Rate Data					
Bandwidth	6		30	*GHz*	
Phase shift	0		80	*ps*	
Output swing		600		*mV*	Single-Ended, p-p
Output Retimed Data (D/D_bar)					
Bandwidth	DC		30	*Gbps*	
Logic “1” level		gnd		*V*	With external 50*Ohm*
Logic “0” level		-0.4		*V*	DC termination
Polarity switch control		-1		*V*	DC control voltage

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REVISION HISTORY

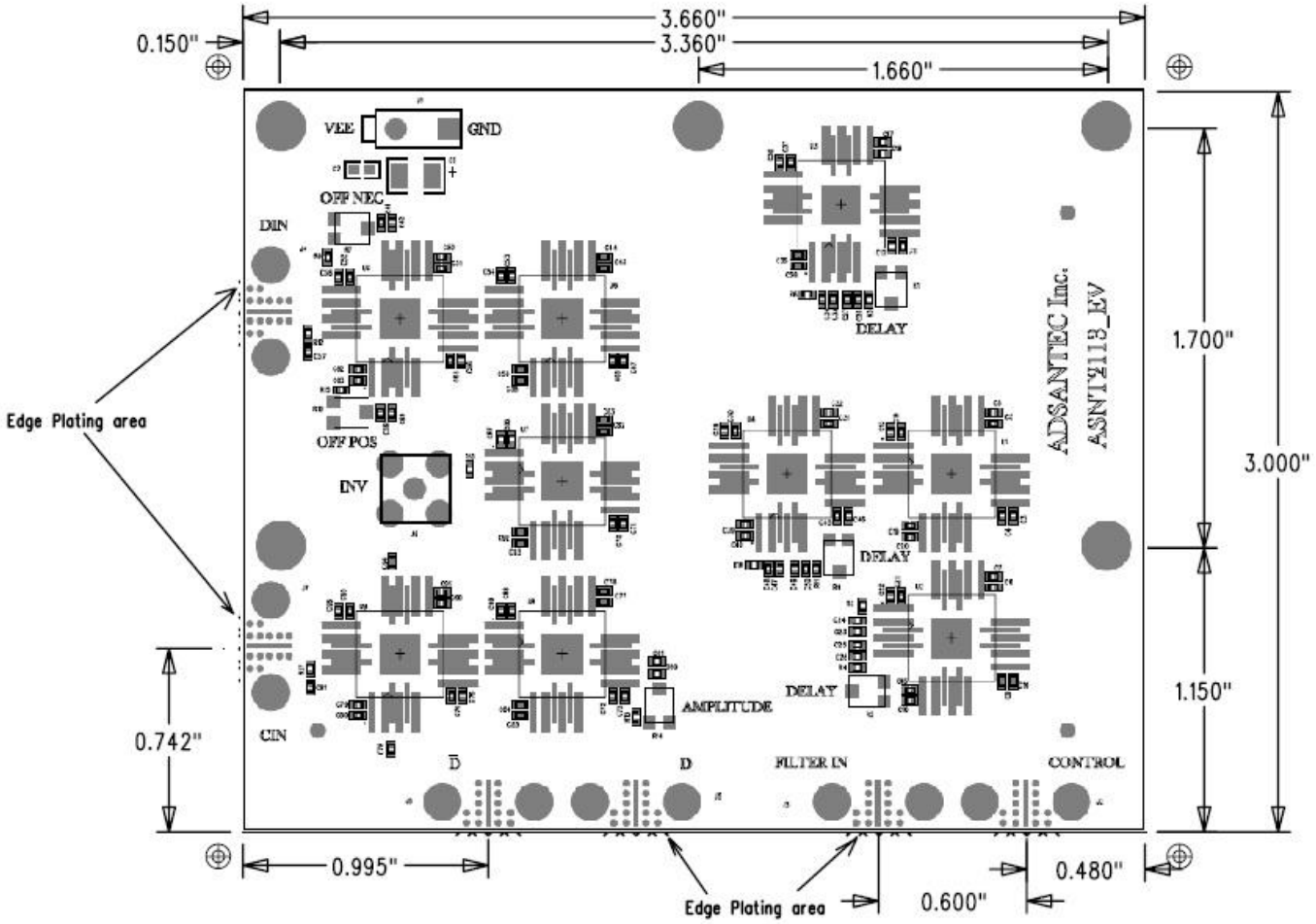

Fig. 3. Board dimensions diagram

REVISION HISTORY

Revision	Date	Changes
1.2.2	05-2023	Added Board Dimensions Section Added Board Dimensions diagram
1.1.2	07-2019	Updated Letterhead
1.1.1	04-2019	Added P/N of connectors to board description
1.0.1	09-2017	Initial Release