ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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ASNT_PRBS40_1
4*Gbps* -44*Gbps* 2^7-1 PRBS Generator with Sync Output

- Broadband frequency range from 4*Gbps* – 44*Gbps*
- Adjustable clock duty cycle for MUX
- 2-512 divide differential sync output
- Static divide-by-four differential output
- AC coupled single-ended Clock Input
- Minimal insertion jitter
- Fast rise and fall times
- 50% duty cycle sync output on all divide ratios
- Single +3.3*V* supply

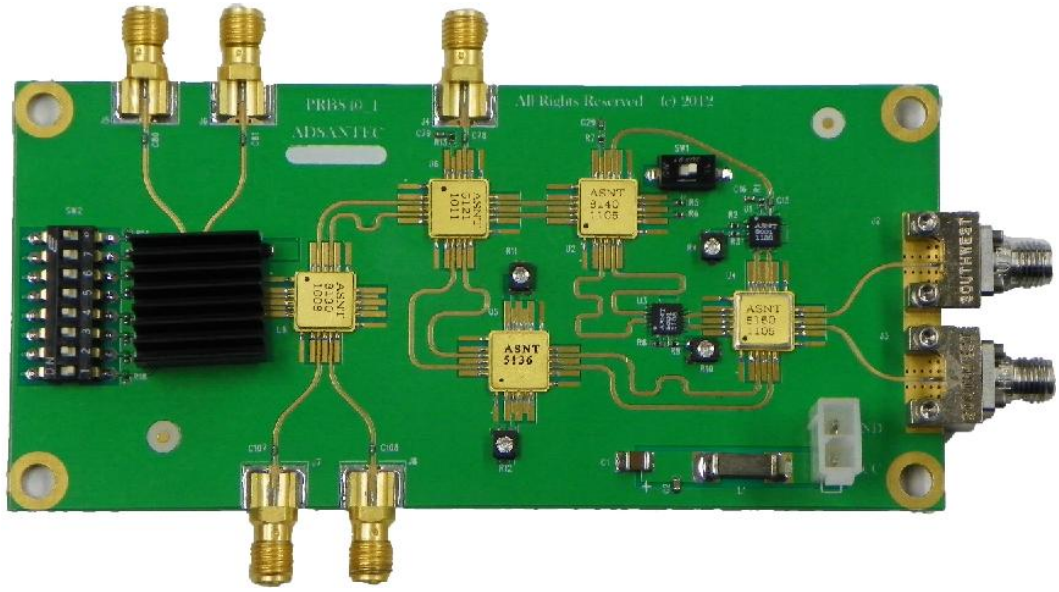

Fig. 1. ASNT_PRBS40_1 evaluation board

DESCRIPTION

The ASNT_PRBS40_1 is a broadband 2^7-1 PRBS generator intended for test, prototyping, microwave, and communication applications. A single-ended clock from 2*GHz* to 22*GHz* is used. This single-ended Clock Input feeds a static differential Divide by 4 Output, an adjustable differential divide-by-2 to 512 Sync Output, a differential clock that supplies the multiplexer responsible for doubling the data rate up to 44*Gbps*, and a differential clock that triggers the PRBS 2^7-1. The Clock Input, Sync Output, and Divide by 4 Output are AC coupled on board. The PRBS Output is DC coupled operating with a common mode level above ground.

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The ASNT_PRBS40_1 board contains five Emerson SMA connectors MFG PN: 142-0761-881, two Southwest 2.92mm (K-type) edge mount female connectors MFG PN: 1092-03A-5, 50*Ohms* transmission lines to the device, and power supply decoupling networks on the evaluation board. Power is supplied through a two-pin MOLEX connector P/N: 39-28-1023.

On board trim potentiometers allow adjustment of the clock's duty cycle that feeds the multiplexer. They also adjust the phase shift delay for both data paths fed into the multiplexer. This adjustment capability ensures the best operating sampling point for the desired waveform output. An on board PRBS reset switch is included to preset the generator to avoid the all zero state lock-up.

FUNCTIONAL BLOCK DIAGRAM

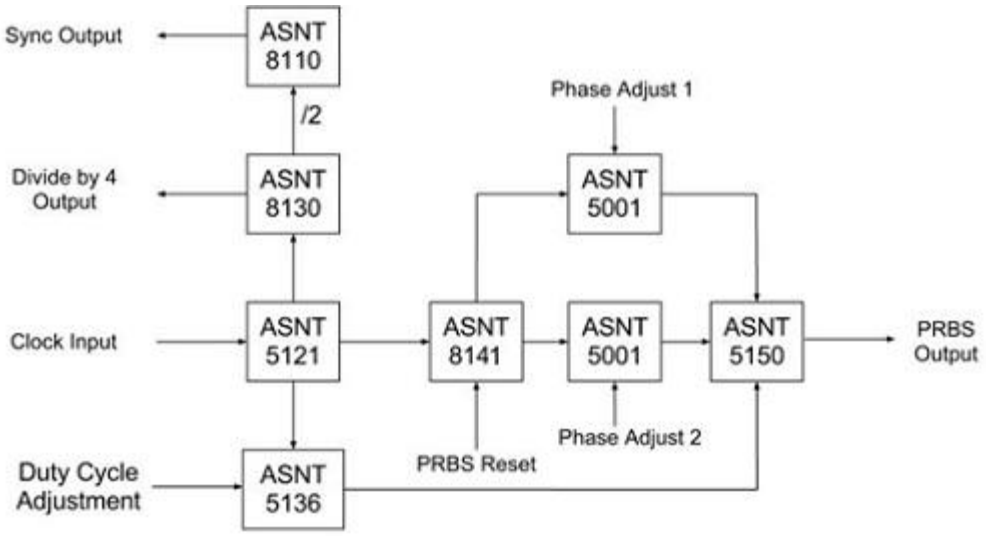

Fig. 2. Functional Block Diagram

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Sync Output

Using the Sync Output to trigger an oscilloscope will display an eye diagram at divide-by-32, and a PRBS waveform output for 254, or 508. It contains eight switches that represent 8 bits. The LSB starts at SW8, and the MSB ends at SW1. The binary value of zero gives a decimal n value of 512. Increasing binary values increases the decimal value n.

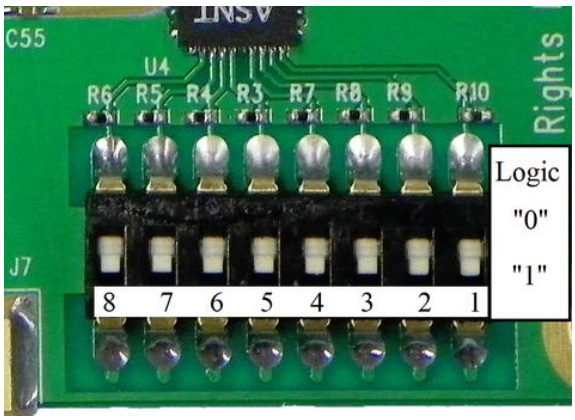

Fig. 3. DIP switch settings

Table 1. Divide ratio

DIP SW # 8 7 6 5 4 3 2 1	n Divide Ratio	
1 0 0 0 0 0 0 0	2	
0 1 0 0 0 0 0 0	4	
0 0 0 0 1 0 0 0	32	Eye diagram
.		
1 1 1 1 1 1 1 0	254	pattern
0 1 1 1 1 1 1 1	508	pattern
0 0 0 0 0 0 0 0	512	

TERMINAL FUNCTIONS

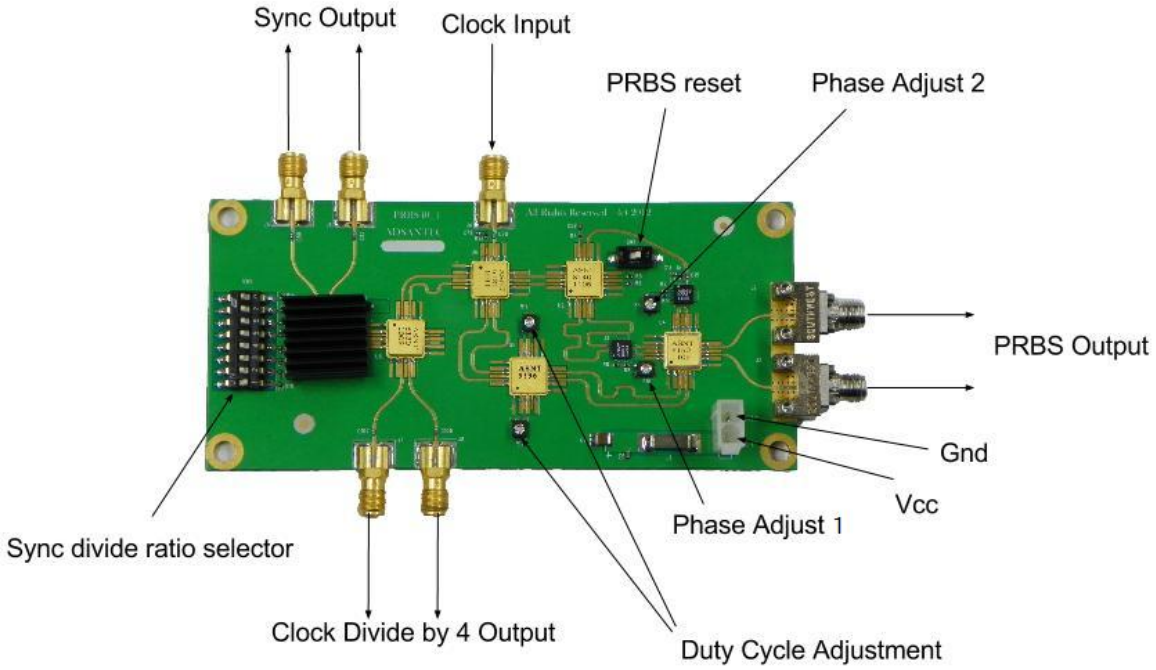

Fig. 4. Terminal Functions Diagram

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OPERATION

1. Measure 50*Ohms* on all SMA connectors referenced to VCC.
2. Set the PRBS Reset switch to the OFF position.
3. Set the power supply to 0.0V, and current limit it to 2.2*A*.
4. Connect the power supply to the board, and slowly increase to +3.3*V*.
5. Apply a DC coupled single-ended clock to the Clock Input.

   (**NOTE**: The Clock Input is AC coupled on board.)
6. Connect the PRBS Output to a 50*Ohms* terminated oscilloscope single-ended, or differentially using DC blocks.

   (**NOTE**: If using a single-ended output only, apply an AC coupled 50*Ohms* termination to the unused output.)
7. Connect Sync Output to trigger single-ended, or differentially. These outputs are AC coupled on board.

   (**NOTE**: If using a single-ended output only, apply 50*Ohms* termination to the unused output.)
8. Toggle the PRBS Reset switch to turn on the PRBS pattern. (Turn it ON then OFF)
9. Use a divide-by-32 ratio for the Sync Output to view the eye pattern on the oscilloscope.
10. It is crucial that both Duty Cycle Adjustments are tuned to achieve the best output performance. When observing the waveform on the oscilloscope, adjust both controls until the best symmetry is achieved. Do not adjust the Phase Adjust control until both Duty Cycle Adjustments are at a position where symmetry on the waveform is at its best.
11. When the Duty Cycle Adjustments are done proceed to change both Phase Adjusts to correct the phase of the data relative to each other and to the clock to achieve the best eye waveform output.
12. The potentiometers are 1-turn, and may be turned in one direction continuously without damage to the ASIC.

    (**NOTE**: If the clock input rate is changed, repeat steps 8, 10 and 11.)

11. **Fig. 5** below provides a diagram with an example of how this board can be connected.

    (**NOTE**: The connections described below only represent one way of interfacing to the evaluation board. While the use of DC blocks will be required on the depicted outputs, there are many ways of connecting the board depending on the use case involved.)

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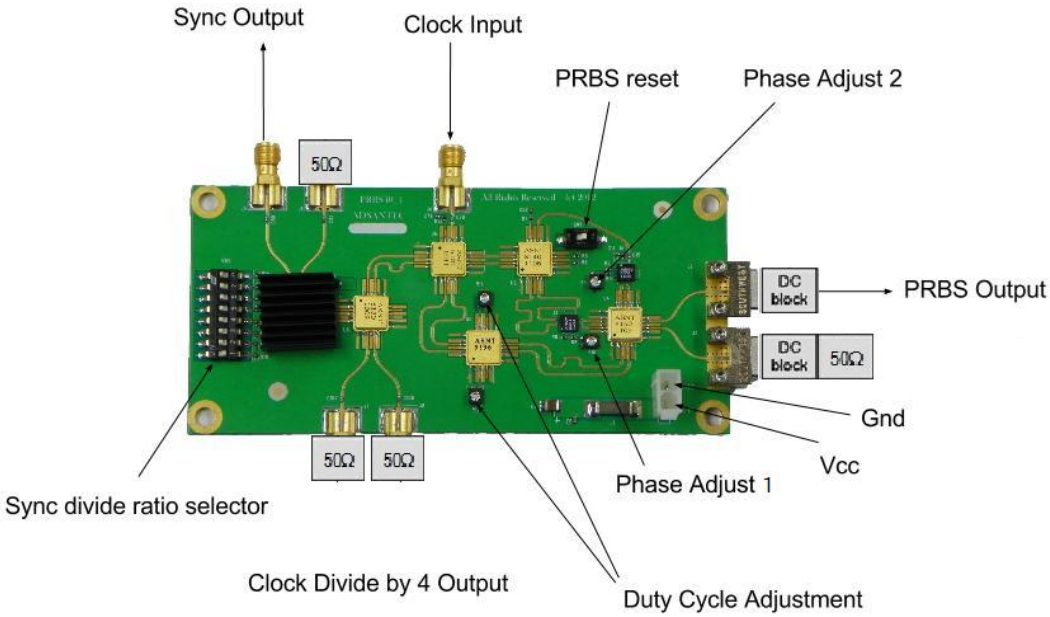

Fig. 5. Recommended Board Configuration Diagram

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ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Comments
vee		0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	
I_{VCC}		2.07		*A*	
Power		6.8		*W*	
Operating Temperature	-25	50	85	*°C*	
Clock Input					
Frequency	2		22	*GHz*	
Single-Ended Swing	50	400	1000	*mV*	Peak-to-Peak
Duty Cycle	40%	50%	60%		Range of input tolerance
Sync Output					
Frequency	0.0039		12	*GHz*	
Single-Ended Swing	570	600	630	*mV*	Peak-to-Peak
Rise/Fall Times	15	17	19	*ps*	20% to 80%
Duty Cycle	45%	50%	55%		For clock signal
PRBS Output					
Data rate	4		44	*Gbps*	
Single-Ended Voltage Level	380	400	420	*mV*	Peak-to-Peak
Common Mode Level	vcc - (Single-Ended Swing)/2			*V*	
Duty Cycle	40%	50%	60%		
Rise/Fall Time	6	8	10	*ps*	20% to 80%

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BOARD DIMENSIONS

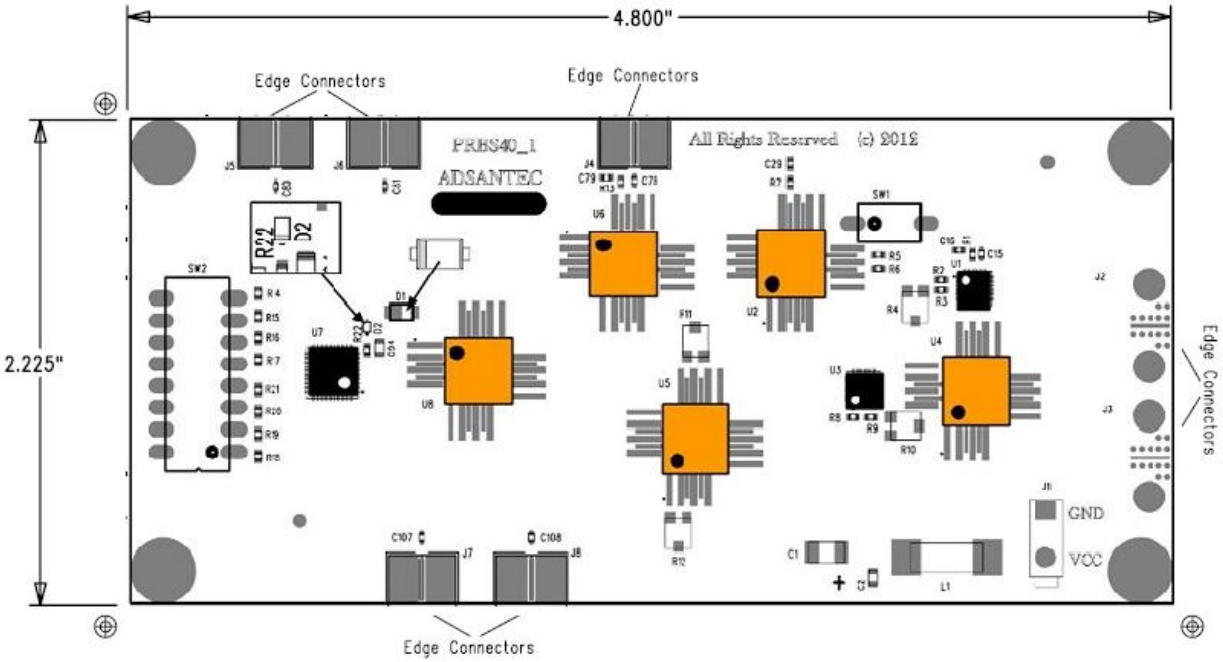

Fig. 6. Board dimensions diagram

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REVISION HISTORY

Revision	Date	Changes
2.0.2	05-2023	Corrected Figure numbering Added Board Dimensions Section Added Fig. 6 Board Dimensions diagram
1.9.2	03-2022	Added Fig. 5. Recommended Board Configuration Diagram
1.8.2	06-2021	Updated for use with the ASNT8110-PQB divider
1.7.2	07-2019	Updated Letterhead
1.7.1	04-2019	Added P/N of connectors to board description
1.6.1	03-2015	Updated block diagram
1.5.1	03-2015	Updated current limit
1.4.1	07-2013	Updated minimum output date rate
1.3.1	05-2013	Revised title Revised description Renamed overview to terminal functions Revised operation Revised electrical characteristics
1.2.1	07-2012	Updated operation procedures
1.1.1	06-2012	Updated electrical characteristics Added overview
1.0.1	06-2012	Initial release