ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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ASNT_PRBS34A REV 2
Selectable PRBS9/PRBS10 Generator with USB Control
Operation Manual

Fig. 1 ASNT_PRBS34A REV 2 Board

- Broadband frequency range from 2*Gbps* – 32*Gbps*
- On board data rate multiplexer to reduce the input clock frequency
- Adjustable phase-shift for multiplexer' clock
- 1-2^{16} (any combination) divide ratio for sync output
- Differential CML inputs and outputs
- Minimal insertion jitter
- Fast rise and fall times
- 50% duty cycle sync output on any divide ratio
- Software controlled via USB 2.0 interface
- Single +5.0V supply

DESCRIPTION

The ASNT_PRBS34A REV 2 is a broadband 2^9-1 or 2^{10}-1 PRBS generator intended for test, prototyping, microwave, and communication applications. A single-ended or differential clock from 1*GHz* to 16*GHz* can be used to drive the generator. A dual 1/256 divider block with differential Sync Output divides the input clock allowing a PRBS9 and PRBS10 pattern view on an oscilloscope by using a divide ratio 511 or 1023. The PRBS9/PRBS10 data output is multiplexed to double the data rate, giving a maximum data rate of 32*Gbps*. An on-board DAC module, software controlled via USB interface allows to phase adjust the multiplexer clock input for all input clock frequencies in a specified range to ensure the best output is achieved. The built-in PRBS generator reset switch presets PRBS generator to avoid the all zero-state lock-up.

FUNCTIONAL BLOCK DIAGRAM

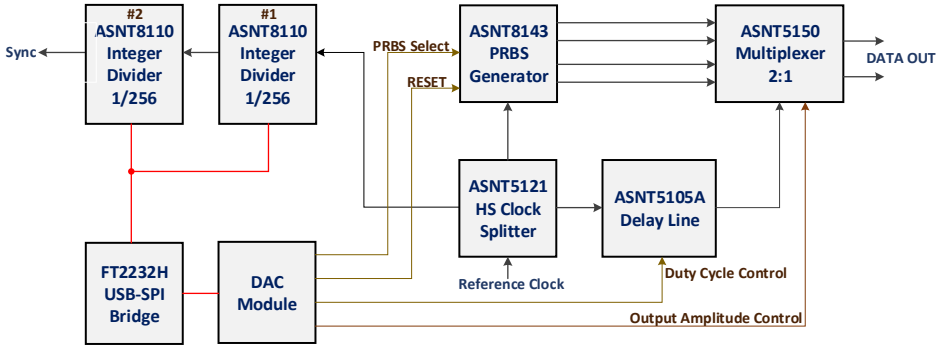

Fig. 2 Functional Block Diagram

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TERMINAL FUNCTIONS

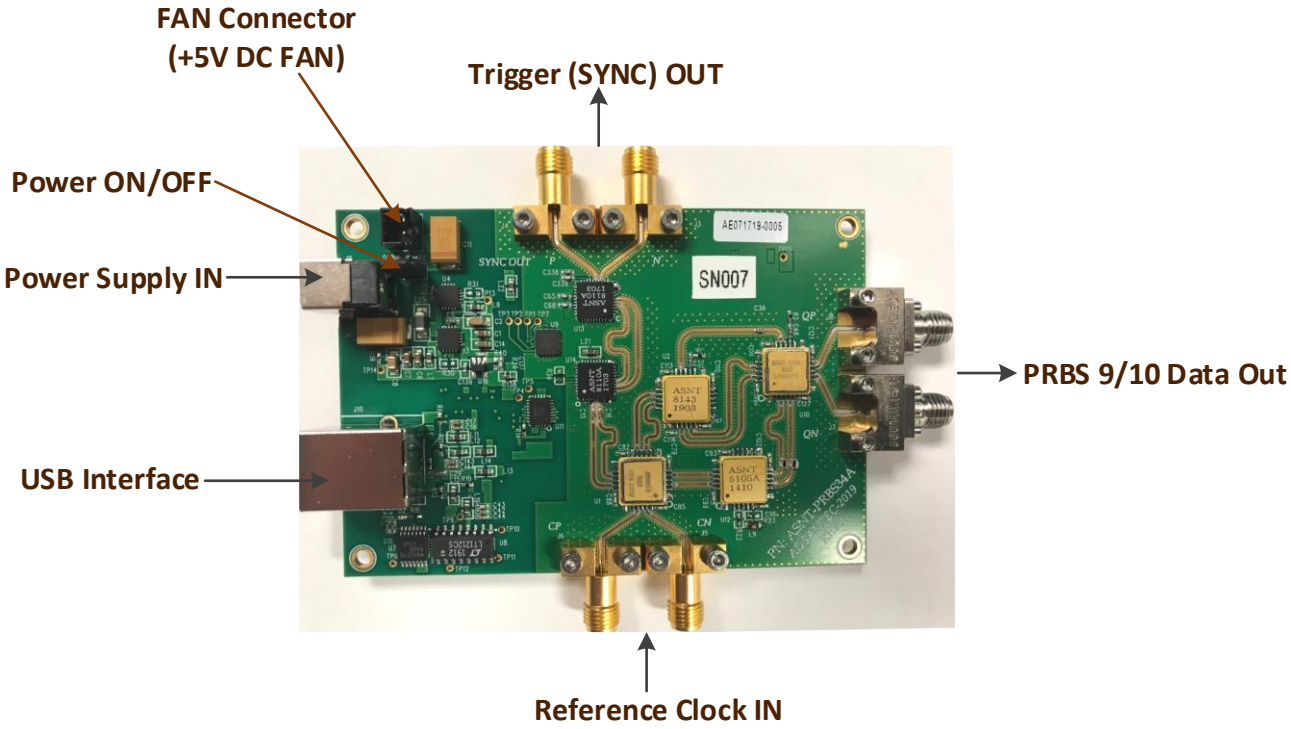

Fig. 3. Terminal Functions Diagram

OPERATION

1. Measure 50*Ohms* on all SMA connectors referenced to **vcc**.
2. Connect the power supply (provided) to the board.
3. Use a fan (not provided) to air cool the board during operation (**Required**).

   The 5V/up to 0.2A FAN can be directly connected to the board (Terminal Functions section).

   Digi-Key part number of the mating connector: H2083-ND; Mating jumper cables: Red – H2BXG-10112-R4-ND; Black - H2BXG-10112-B4-ND
3. Apply an **AC coupled** single-ended/differential clock signal to the Reference Clock Input.
4. Connect the PRBS Output to a 50*Ohms* terminated **AC-coupled** oscilloscope single-ended/differentially.
5. Connect the Sync (Trigger) Output **AC-coupled** to oscilloscope trigger

   Note: If using a single-ended input/output only, apply an AC coupled 50*Ohms* termination to the unused input/output. This will reduce any noise presence.
6. Start the provided software and choose either a PRBS9 or a PRBS10 Pattern.
7. Follow the software operating instructions provided in the GUI interface section.

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GUI Interface

The provided GUI interface allows full PC control of the ASNT_PRBS34A REV 2 output signal parameters, including the output sync signal division ratio. After starting the software by engaging the provided **.exe** file the GUI window will appear as it's depicted in the picture below.

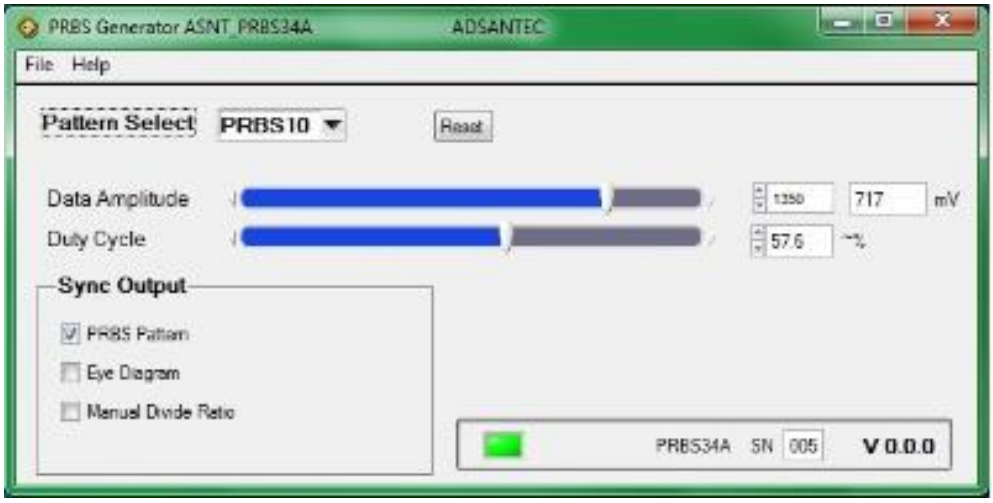

Fig. 4. ASNTPRBS34A REV 2 GUI Interface

The software automatically connects to a powered and USB-connected ASNT_PRBS34A REV 2 board. When connected, the USB connection indicator changes the color from red to green and indicates the serial number of the board under test (in the provided example it's **SN 005**). The device is connected and ready for configuration. If necessary, reset the generator to avoid the all zero-state lock-up at the start up by clicking the **Reset button** (upper center). The user can choose the type of Sync output signal depending on the particular testing need by checking the appropriate box in the **Sync Output** section. The PRBS pattern type selection is realized by choosing the appropriate pattern in the **Pattern Select** dropdown menu. The interface also supports precision output data amplitude adjustment (**Data Amplitude**) and multiplexer clock input phase adjustment to ensure the best possible data output signal under full range of input clock frequencies (**Duty Cycle**).

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ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Comments
Power Supply		5.0		*V*	Provided
Ivcc		2.1		*A*	
Power		10.5		*W*	
Operating Temperature	-25	30	60	*°C*	
Clock Input					
Frequency	1		16	*GHz*	
Single-Ended Swing	50	400	1000	*mV*	Peak-to-Peak
Common mode level	vcc -0.8	vcc -0.2	vcc	*V*	
Duty Cycle	40%	50%	60%		Range of input tolerance
Sync Output					
Frequency	0.0003		16	*GHz*	
Single-Ended Swing	570	600	630	*mV*	Peak-to-Peak
Common-Mode Level	vcc - (Single-Ended Swing)/2				
Rise/Fall Times	15	17	19	*ps*	20% to 80%
Duty Cycle	45%	50%	55%		
PRBS Output					
Data rate	2		32	*Gbps*	
Single-Ended Voltage Level		400		*mV*	Peak-to-Peak
Common Mode Level	vcc - (Single-Ended Swing)/2			*V*	
Duty Cycle	40%	50%	60%		
Rise/Fall Time		20		*ps*	20% to 80%

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BOARD DIMENSIONS

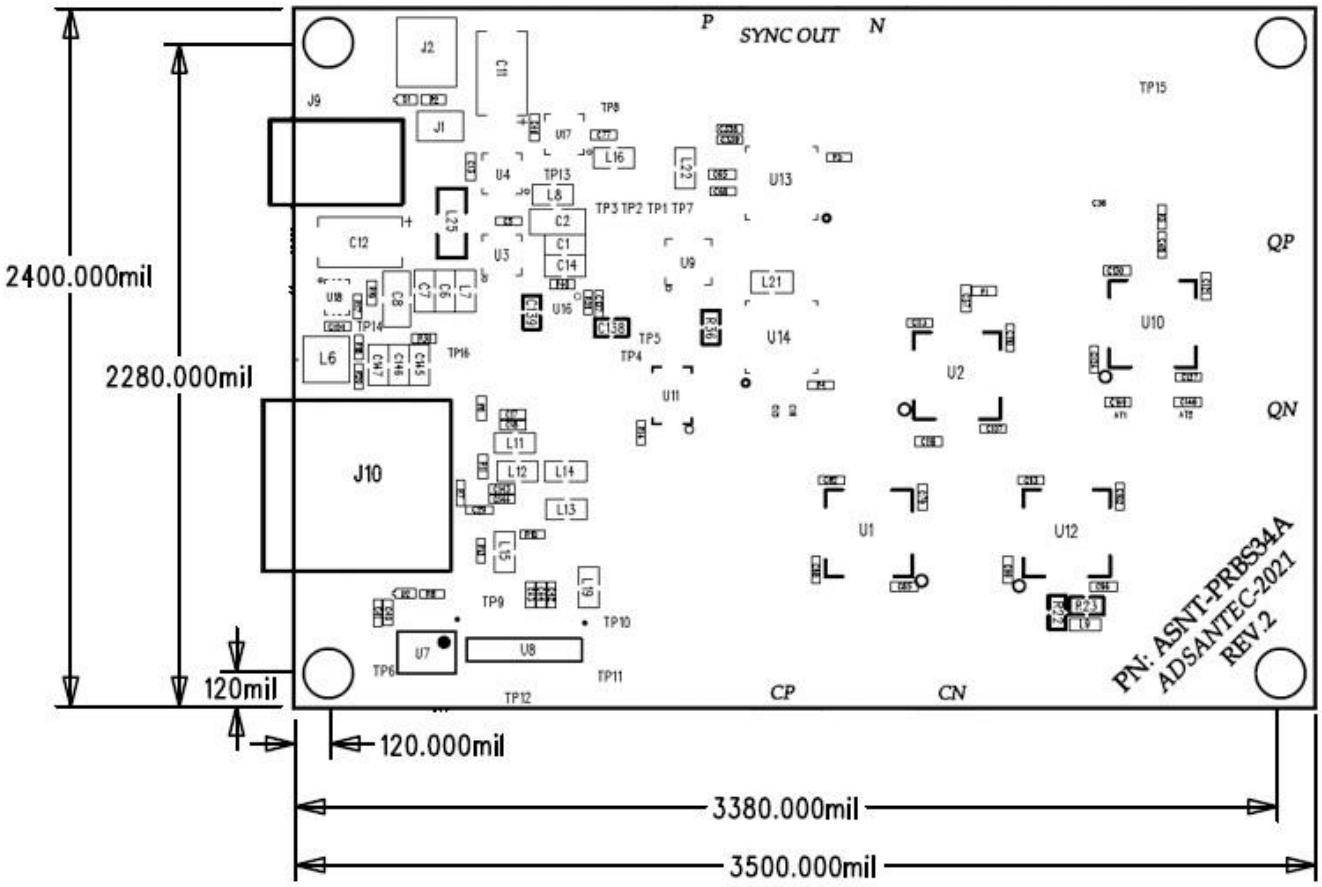

Fig. 5 Board Dimensions Diagram

REVISION HISTORY

Revision	Date	Changes
1.2.2	09-2025	Added revision number
1.1.2	05-2023	Added Board Dimensions Section Added Fig. 5 Board Dimensions Diagram
1.0.2	11-2021	Initial release