ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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ASNT_PRBS20B_1
20*Mbps*-18*Gbps* PRBS7/15 Generator Featuring Jitter Insertion, Selectable Sync, and Output Amplitude Control

- Broadband frequency range from 20*Mbps* – 18.0*Gbps*
- Minimal insertion jitter
- Fast rise and fall times
- Two PRBS data output, jitter insertion capability, and output amplitude control from 0*V* to 1*V* peak to peak.
- Up to 155*ps* delay variation on each output
- Differential clock output
- 50% duty cycle for sync output on all divide ratios
- Sync output and Clock input are AC coupled on board
- Single positive 3.3*V* supply

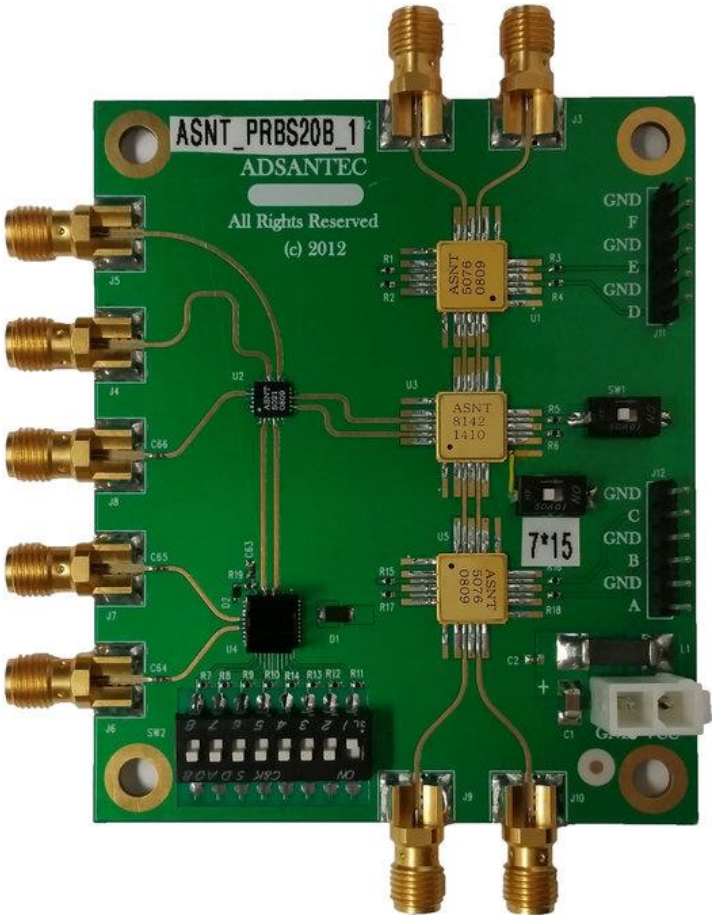

Fig. 1. ASNT_PRBS20B_1 evaluation board

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DESCRIPTION

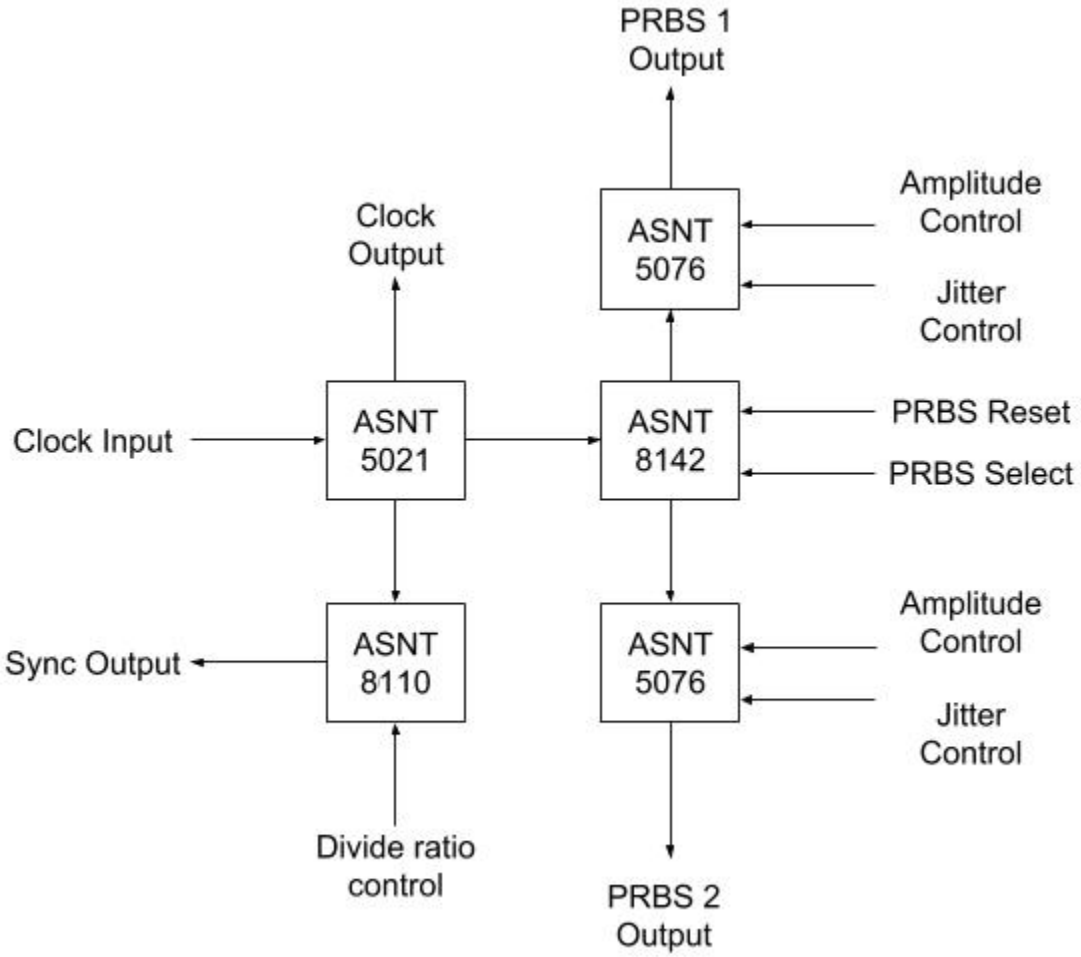

Fig. 2. Functional Block Diagram

The ASNT_PRBS20B_1 is a broadband 2^7-1 or 2^{15}-1 PRBS generator intended for test, prototyping, microwave, and communication applications. The amplitude, and phase are adjustable on both differential outputs. There is jitter/phase shift insertion onto either differential output with a bandwidth up to 500 *kHz*. Output amplitude on both PRBS outputs varies from 0*V* to 1*V* single-ended peak to peak. A single-ended clock from 10*MHz* to 18*GHz* with an amplitude as low as 50*mV* peak to peak may be applied to the clock input. A buffered differential clock output is provided. A differential Sync Output divides an input clock from 1 to 256. When using an oscilloscope, the Sync Output triggers the oscilloscope. The system is capable of triggering for an eye diagram for PRBS7/PRBS15, or a PRBS7 pattern with divide ratios 127 or 254, and it uses an on-board PRBS reset switch to preset the generator avoiding the all zero state lock-up. An on-board Pattern Select switch selects either PRBS7, or PRBS15.

The ASNT_PRBS20B_1 board contains nine Emerson SMA connectors MFG PN: 142-0761-881, 50*Ohms* transmission lines to the device, and power supply decoupling networks on the evaluation board. Power is supplied through a two-pin MOLEX connector P/N: 39-28-1023.

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SYNC OUTPUT

The Sync Output can be configured to output any divide ratio from 1 to 256 from the clock input. It contains eight switches that represent 8 bits. The LSB starts at SW8, and the MSB ends at SW1. The binary value of zero gives a decimal n value of 256. Increasing binary values increases the decimal value n.

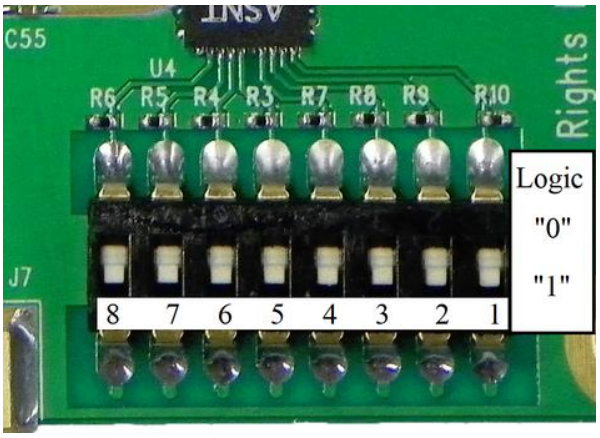

Fig. 3. DIP switch settings

DIP SW # 8 7 6 5 4 3 2 1	n Divide Ratio	
1 0 0 0 0 0 0 0	1	
0 1 0 0 0 0 0 0	2	
1 1 0 0 0 0 0 0	3	
0 0 0 0 1 0 0 0	16	Eye diagram
. .		
1 1 1 1 1 1 1 0	127	pattern
0 1 1 1 1 1 1 1	254	pattern
0 0 0 0 0 0 0 0	256	

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed nor implied. All min and max voltage limits are in reference to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.6	*V*
Power Consumption		8	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

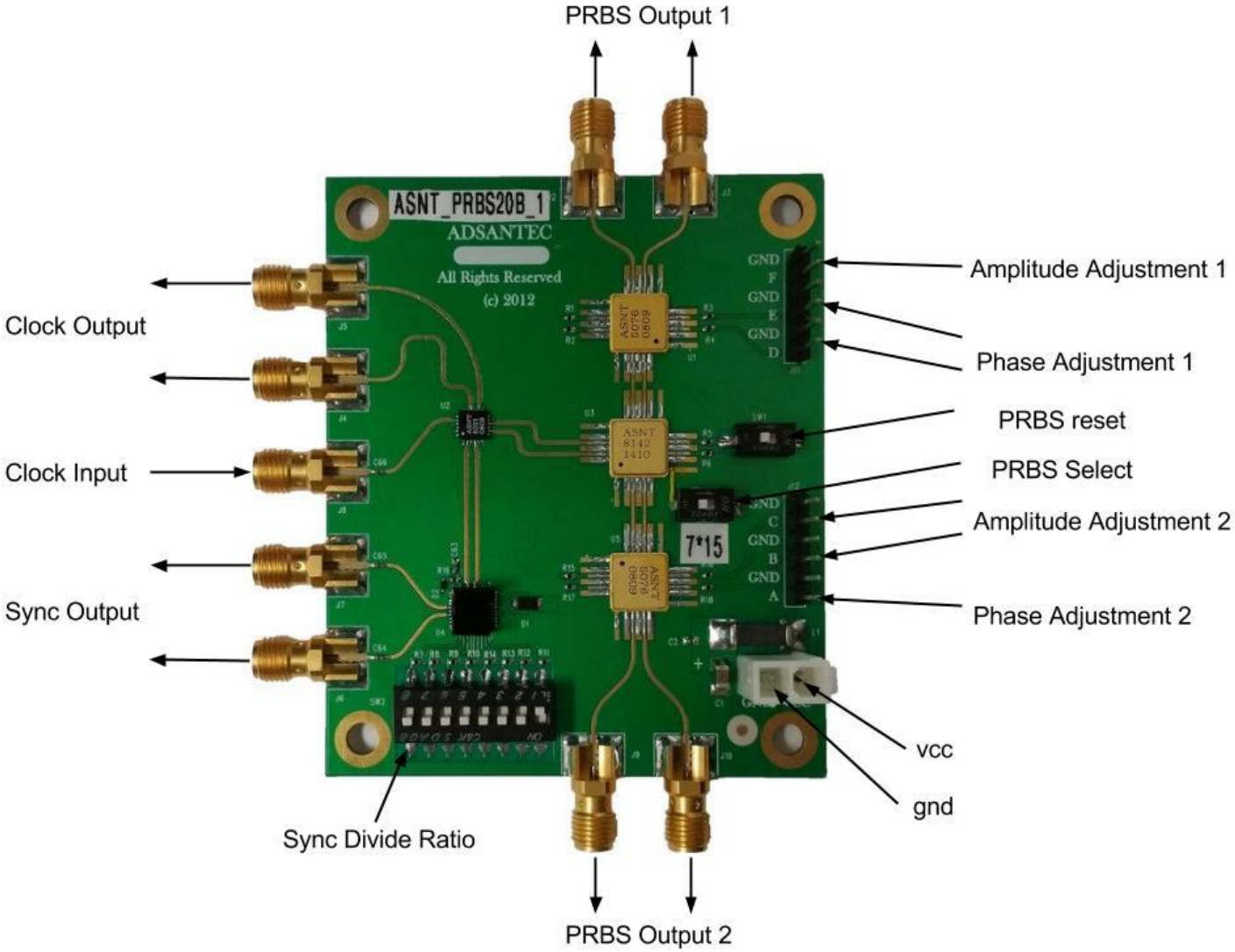

Fig. 4. Terminal functions diagram

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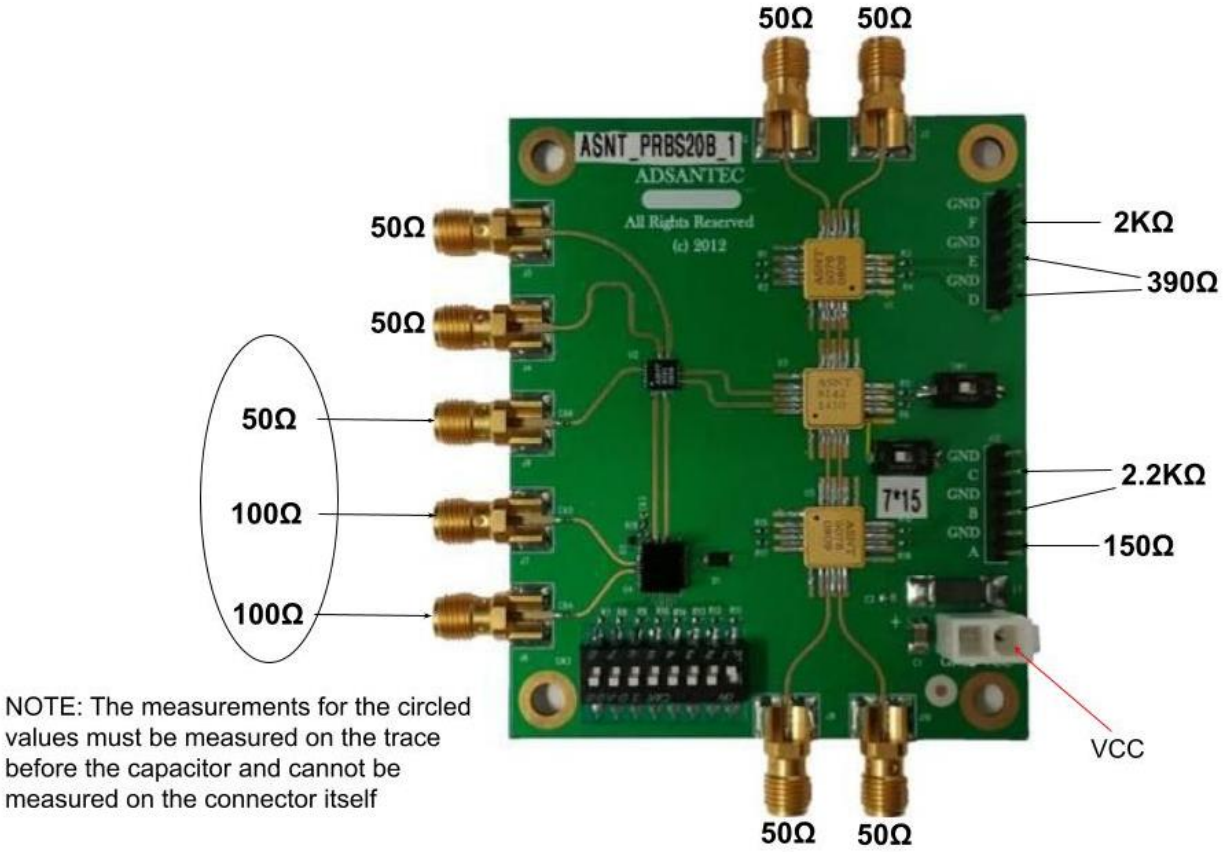

Fig. 5. Ohmic Measurements diagram

OPERATION

1. Measure ALL I/O's on board according to **Fig. 5** in relation to vcc.

   (**NOTE**: A deviance of up to 10% in these values is within specification.)
2. Connect the board to a power supply set to 0.0*V* with a current limit of 2.3*A*.
3. Slowly increase the power supply to + 3.3*V*. The nominal current is 2.2*A*.
4. Apply a DC coupled clock to the Clock Input up to 18*GHz* with a peak-to-peak amplitude from 50*mV* to 1*V*.
5. (**NOTE**: Clock input and sync outputs are AC coupled on-board.)
6. Connect the PRBS outputs AC coupled to a 50*Ohms* terminated oscilloscope as well as one sync output. Place 50*Ohms* AC coupled terminations on all unused input/outputs.
7. Set the PRBS Select switch to the ON position to select PRBS15, or OFF to select PRBS7.
8. Turn the PRBS reset switch to the ON position, and then back to the OFF position to reset the PRBS generator.

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9. To add jitter, or change the phase on the PRBS 1 output, apply a 2.1*V* to 3.3*V* to header pin E and float (do not connect) pin D to decrease phase shift. Apply 2.1*V* to 3.3*V* to header pin D and float (do not connect) header pin E to increase phase shift.

10. To change the amplitude on the PRBS 1 output, apply a positive voltage ranging from 2.5V to 3.3V to header pin F. The amplitude control for the PRBS 1 output is single-ended only.

11. To change the amplitude on the PRBS 2 output, apply a voltage ranging from 2.5*V* to 3.3*V* to header pin B and float (do not connect) pin C to increase amplitude. Apply a voltage ranging from 2.5*V* to 3.3*V* to header pin C and float (do not connect) header pin B to decrease amplitude.

12. To add jitter, or change the phase on the PRBS 2 output, apply a positive voltage ranging from 2.1V to 3.3V to header pin A. The delay control for the PRBS 2 output is single-ended only.

13. **Fig. 6** on the following page provides an example of how this board can be connected.

    (**NOTE:** The connections described below only represent one way of interfacing to the evaluation board. While the use of DC blocks will be required on the depicted outputs, there are many ways of connecting the board depending on the use case involved.)

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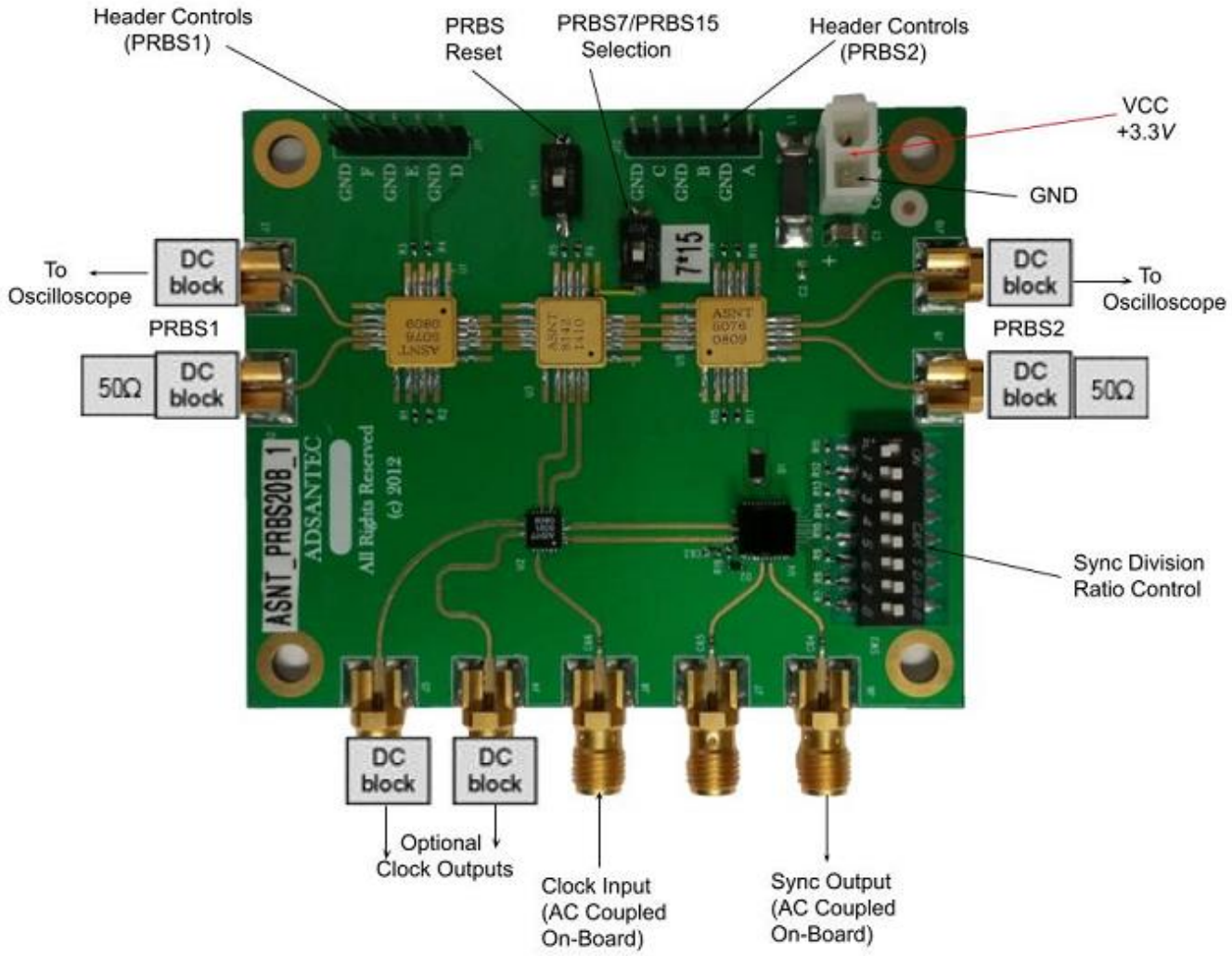

Fig. 6. Recommended Board Configuration Diagram

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
vee		0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	
I_{VCC}	1.7	2.2	2.5	*A*	
Power		7.2		*W*	
Operating Temperature	-25	50	85	*°C*	
Clock Input					
Frequency	0.02		18	*GHz*	
Single-Ended Swing	50	400	1000	mV_{PP}	
Clock Output					
Frequency	0.02		18	*GHz*	
Single-Ended Swing	570	600	630	mV_{PP}	
Common Mode Level	vcc -0.35	vcc -0.3	vcc -0.25		
Additive Jitter			5	*ps*	Peak-to-Peak
Duty Cycle	45	50	55	%	For Clock Signal
Sync Output					
Frequency	0.01		18	*GHz*	
Single-Ended Swing	570	600	630	mV_{PP}	
Rise/Fall Times	15	17	19	*ps*	20%-80%
Duty Cycle	45%	50%	55%		For clock signal
PRBS_1 Output					
Single-Ended Voltage Level	475	500	525	mV_{PP}	
Common Mode Level	vcc -0.3	vcc -0.25	vcc -0.2	*V*	When the amplitude adjustment pin F is not connected
Duty Cycle	45	50	55	%	

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ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
PRBS_2 Output					
Single-Ended Voltage Level	475	500	525	mV_{PP}	
Common Mode Level	vcc -0.3	vcc -0.25	vcc -0.2	*V*	When the amplitude adjustment pins B and C are not connected
Duty Cycle	45%	50%	55%		
Amplitude Control					
Differential Swing	-2.85		2.85	mV_{PP}	
Common Mode Level	vcc -0.5	vcc -0.25	vcc	*V*	
Amplitude Variation	0	500	1000	*V*	
Bandwidth	0.0		100	*kHz*	
Jitter Control					
Differential Swing	-3.8		3.8	mV_{PP}	
Common Mode Level	vcc -0.5	vcc -0.25	vcc	*V*	
Phase Shift Control	0		155	*ps*	
Shift Stability	-12		12	*ps*	0-125°C
Bandwidth	0.0		500	*kHz*	

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BOARD DIMENSIONS

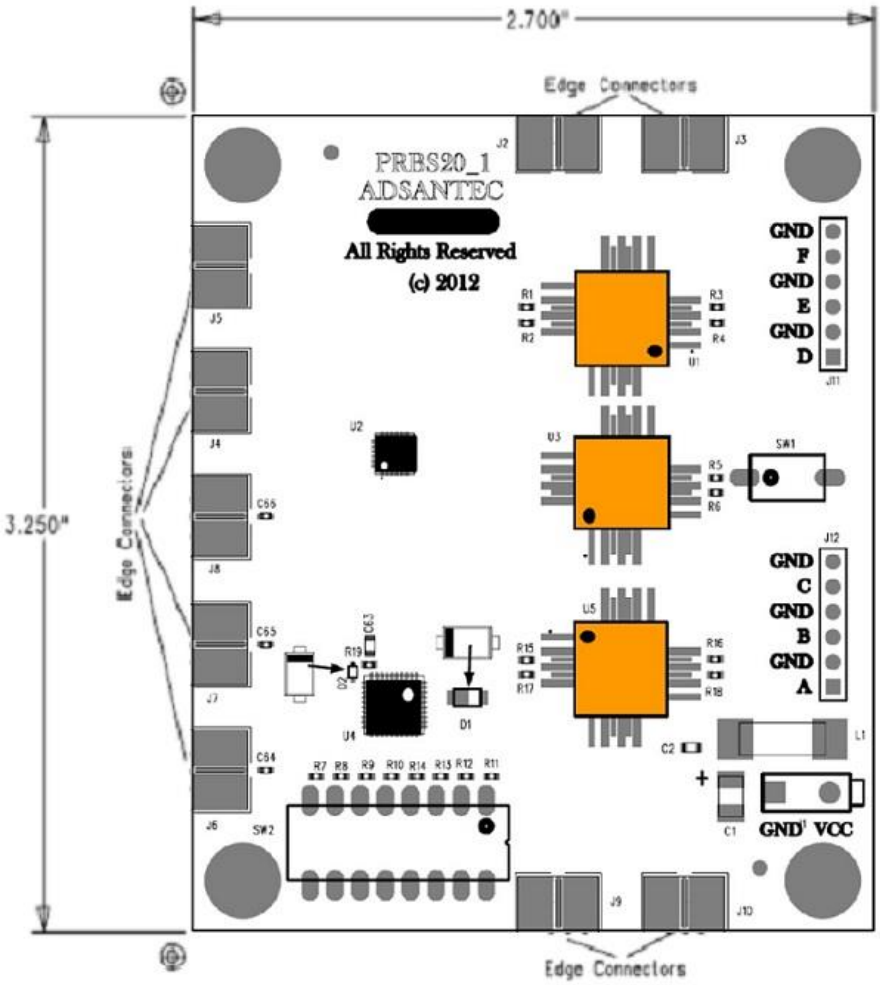

Fig. 7. Board dimensions diagram

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REVISION HISTORY

Revision	Date	Changes
2.0.2	03-2025	Added Fig. 6 Diagram and ohmic measurement clarifications
1.9.2	05-2023	Corrected Figure numbering Added Board Dimensions Section Added Fig. 7 Board Dimensions diagram
1.8.2	03-2022	Added Fig. 6
1.7.2	08-2021	Updated the Operation section Updated Electrical Characteristics table
1.6.2	02-2021	Updated for Use with ASNT8110 Divider
1.5.2	08-2020	Updated Ohmic Values, Sensitivity and Electrical Characteristics
1.4.2	02-2020	Corrected Header Control Voltage Values
1.3.2	07-2019	Updated Letterhead
1.3.1	04-2019	Added P/N and connector description to board description
1.2.1	08-2015	Correction Operation #2. Current limit increased to 2.2A from 2A
1.1.1	04-2015	Changed page 1 picture and terminal function picture Changed Ivcc current and power Corrected Operation #6
1.0.1	04-2015	Initial Release