ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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ASNT_502
2*kHz*-46*GHz* Clock Divide-by-8/2-to-1024

- Broadband frequency range from 2*kHz* – 46*GHz*
- Minimal insertion jitter
- Fast rise/fall times
- 50% duty cycle for all divide ratios
- Selectable divide output up to 1024
- Second divide by 8 output
- Positive +3.3*V* supply

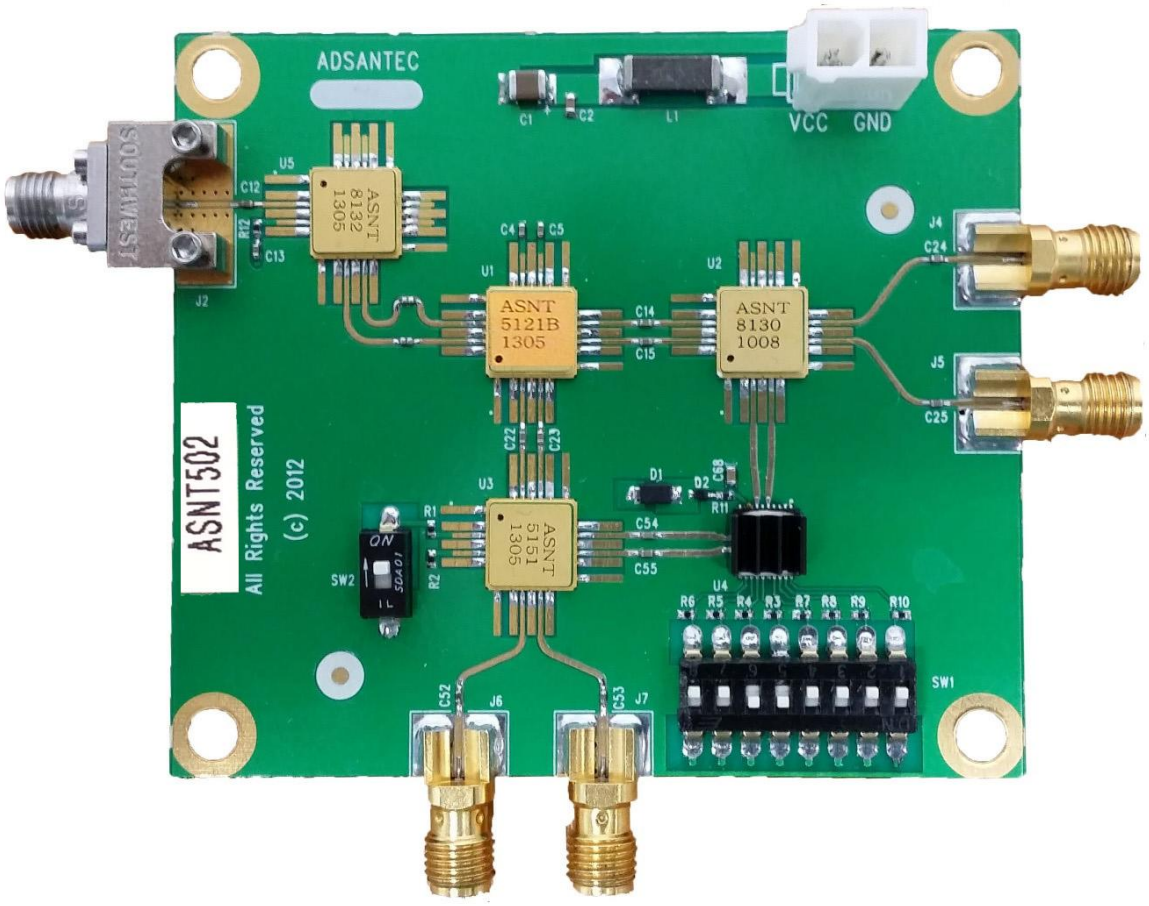

Fig. 1. ASNT_502 evaluation board

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DESCRIPTION

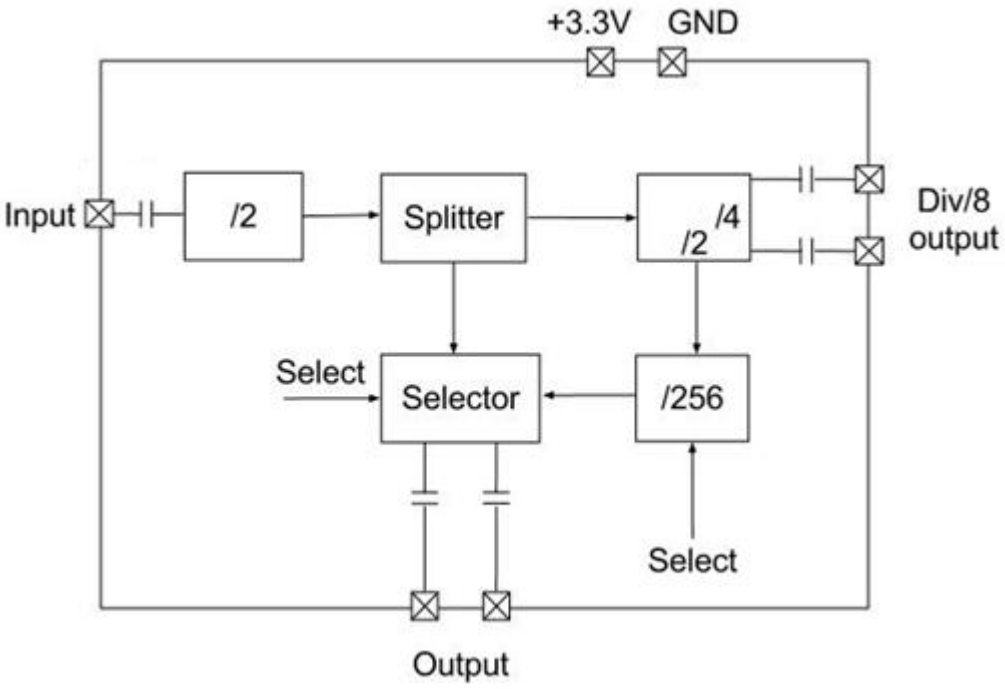

Fig. 2 Functional Block Diagram

The ASNT_502 system on board functions as a multi-purpose divider for test, microwave, and communication applications. The selectable divide output can be operated single-ended or differentially. A secondary fixed divide-by-8 output can also be used single-ended or differentially. The high-speed clock input is AC coupled with a K-type Southwest connector MFG PN: 1092-03A-5. The clock outputs are AC coupled with Emerson SMA connectors MFG PN: 142-0761-881. Power is supplied through a two pin MOLEX connector P/N: 39-28-1023.

APPLICATIONS

The ASNT_502 divider can be used as a prescaler to extend the useful frequency range for triggering. The second fixed divide-by-8 output can be used to synchronize other devices. The divider can also be used as a prescaler for PLL's or frequency counters.

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DIVIDE RATIO CONTROL

The divide by (2-to-1024) output has been configured to divide the input frequency ratio from 2 to 1024. The following equation {Div/ output n = 4m}, where m is an integer from 1 to 256 which provides all possible divide ratios. The divide ratio control contains 8 switches which represent 8 bits. The LSB starts at SW8 and the MSB ends at SW1. The binary value of zero gives a decimal m value of 256. Ascending binary values increase the decimal value m. Table 1 shows values of m with their corresponding binary representation.

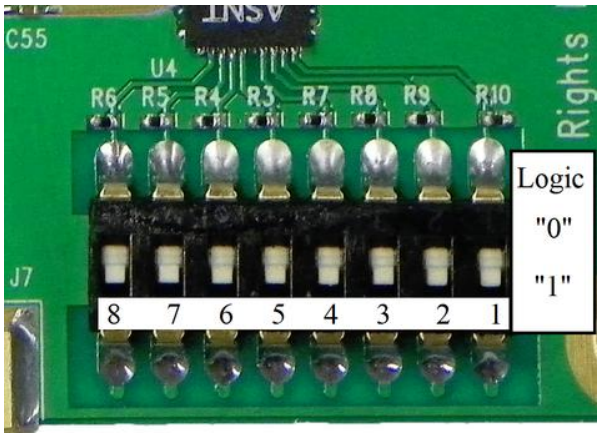

Fig. 3. DIP switch settings

Table 1. Binary Values for Divide Ratio

DIP SW #	m	n
8 7 6 5 4 3 2 1	**Switch Ratio**	**Divide Ratio**
1 0 0 0 0 0 0 0	1	4
0 1 0 0 0 0 0 0	2	8
1 1 0 0 0 0 0 0	3	12
0 0 1 0 0 0 0 0	4	16
. . .		
1 0 0 1 1 0 0 0	25	100
.		
.		
.		
0 1 0 1 1 1 1 1	250	1000
. . .		
1 1 1 1 1 1 1 1	255	1020
0 0 0 0 0 0 0 0	256	1024

DIVIDE-BY-2 SWITCH

Switching the divide-by-2 switch to the position shown below (Div/2) will override any divide ratio that is currently set on the divide ratio control and output a divide-by-2. Switching the divide-by-2 switch to the position below (Div/4-1024) will turn on the divide ratio control.

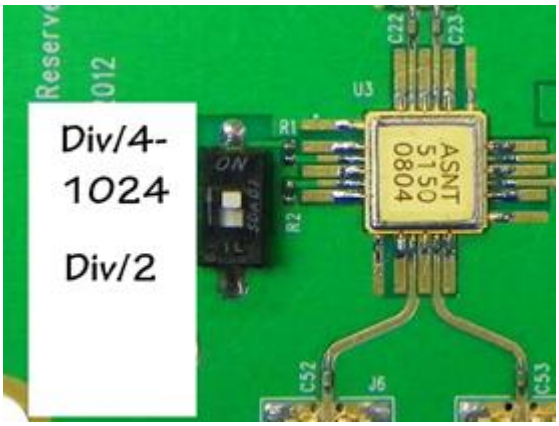

Fig. 4. Divide switch settings

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		+3.6	*V*
Power Consumption		4.7	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

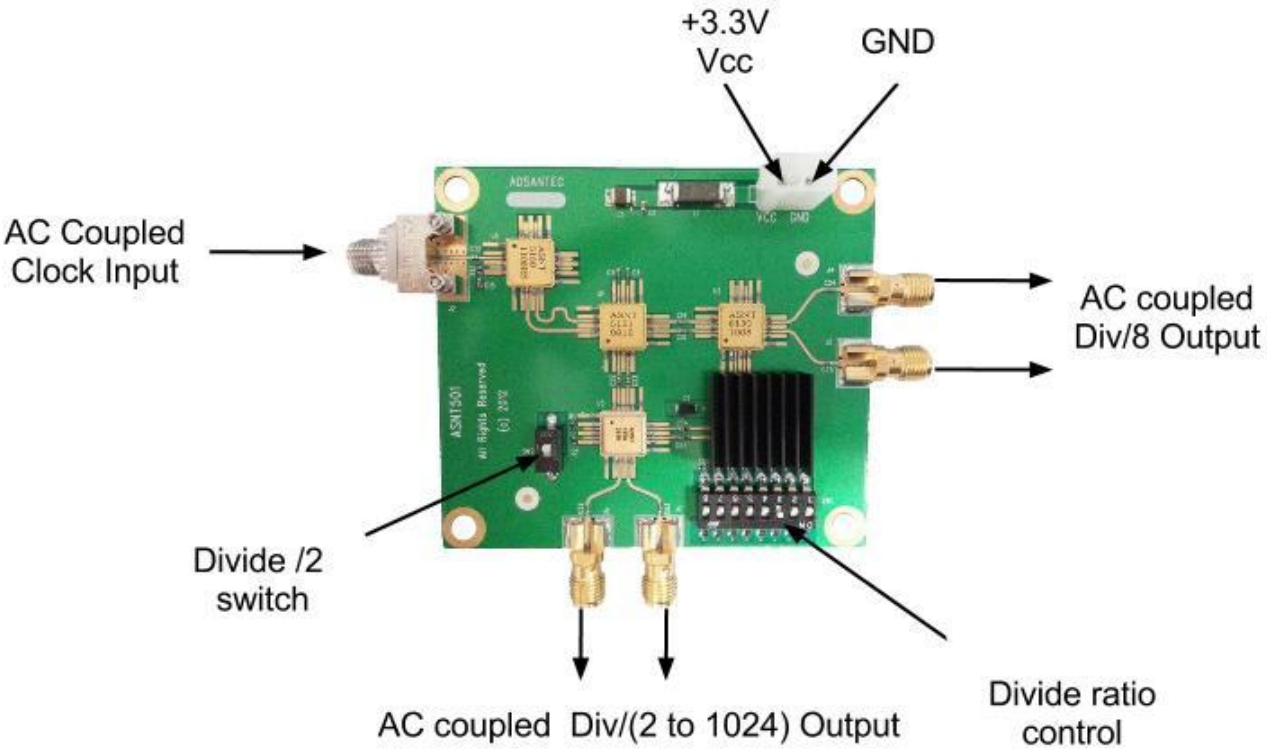

Fig. 5. Terminal Functions Diagram

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
V_{EE}		0		*V*	External ground
V_{CC}	3.1	3.3	3.5	*V*	
I_{VCC}		1300		*mA*	
Power		4.3		*W*	
Operating Temperature	-25	50	85	*°C*	
Clock Input					
Frequency	2.0E-6		46	*GHz*	
Single-ended Swing	200	400	1000	mV_{PP}	
Common Mode Level	V_{CC}-0.8	V_{CC}-0.2	V_{CC}	*V*	
Duty Cycle	40	50	60	*%*	Range of input tolerance
Output (Div/8)					
Frequency	2.0E-6		5.75	*GHz*	
Single-ended Swing	380	400	420	mV_{PP}	
Rise/Fall Time	10	12	14	*ps*	20% to 80%
Additive Jitter		<1		*ps*	Peak-to-Peak
Duty Cycle	45	50	55	*%*	For clock signal
Output (2-to-1024)					
Frequency	2.0E-6		23	*GHz*	
Single-ended Swing	380	400	420	mV_{PP}	
Rise/Fall Time	10	12	14	*ps*	20% to 80%
Additive Jitter		<1		*ps*	Peak-to-Peak
Duty Cycle	45	50	55	%	For clock signal

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BOARD DIMENSIONS

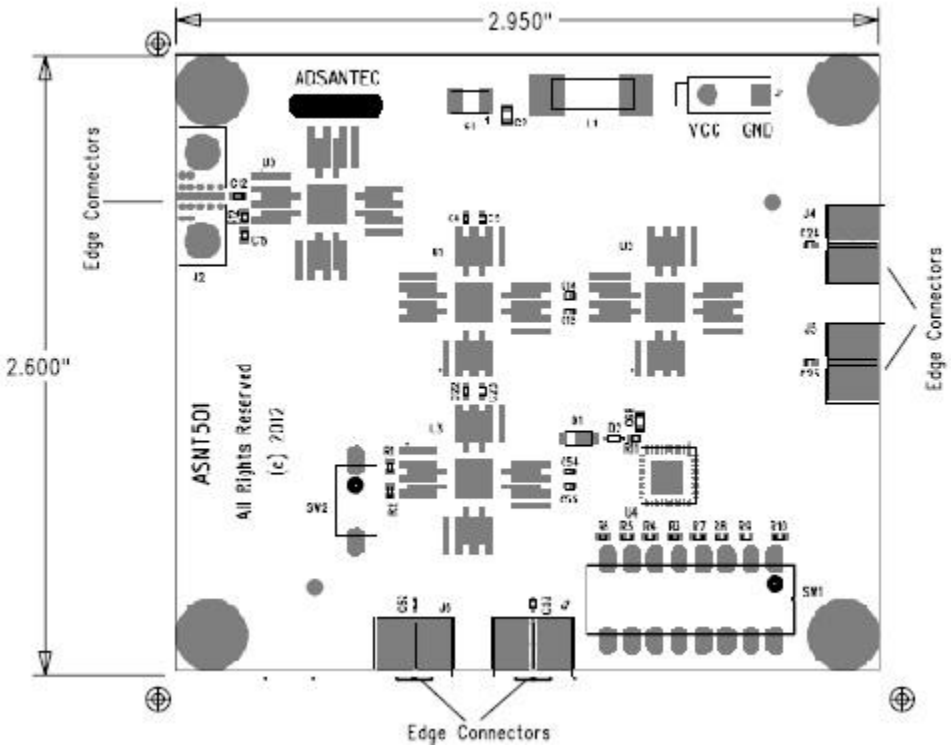

Fig. 6. Board dimensions diagram

REVISION HISTORY

Revision	Date	Changes
1.5.2	05-2023	Corrected Figure numbering Added Board Dimensions Section Added Board Dimensions diagram
1.4.2	01-2021	Updated for use with ASNT8110
1.3.2	07-2019	Updated Letterhead
1.3.1	04-2019	Added P/N of connectors to board description
1.2.1	11-2018	Updated frequency of operation
1.1.1	09-2015	Update current and power consumption Updated Board Picture and Divide-by-2 Switch Picture
1.0.1	08-2014	Initial release