ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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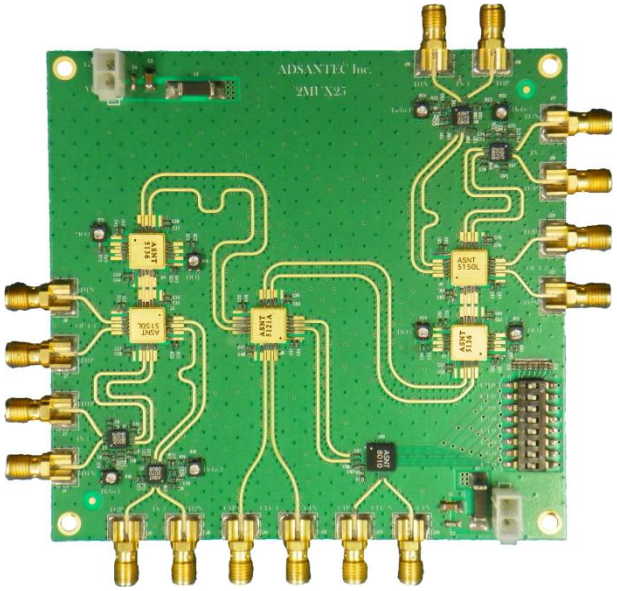
ASNT_2MUX25
DC-44*Gbps* Dual Channel Data Rate Doubler with Sync Output



- Broadband frequency input range from DC to 22*Gbps*
- Individual on board adjustable data path delays to ensure optimal timing at the multiplexer inputs
- Easy two-way duty cycle adjustment for the multiplexer clock inputs
- Synchronization signal with the frequency divided by any number from 1 to 256 and 50% duty cycle for viewing data bits or full eye diagram
- Differential inputs and outputs
- Minimal insertion jitter
- Fast rise and fall times
- One negative power supply at -3.3*V* and one positive power supply at +3.0*V*

DESCRIPTION

The ASNT_2MUX25 system on board integrates two identical 2:1 multiplexer blocks. Each MUX is used to double the incoming data rate by multiplexing two of the four input data channels. All four digital inputs have an operating frequency range from DC up to 22*Gbps*, resulting in the possibility to generate two differential output data streams with a rate up to 44*Gbps*.

Input data can be applied single-ended/differentially, and AC/DC coupled to the inputs of each MUX. Two independent delay lines can correct the phase relationship between both data signals. On-board potentiometers allow for the individual adjustment of each data channel.

The clock input signal with a frequency from DC to 22*GHz* can be applied single-ended/differentially, and AC/DC coupled. Amplifiers are used in both clock paths to optimize the duty cycle of the two multiplexed output data signals.

The board also incorporates a programmable 1 to 256 divider (optional), operating up to 17*GHz* that can be used to generate a synchronization signal for monitoring the output data signals. The divider output is fully differential and supports the CML interface.

The multiplexer circuitry operates from a negative -3.3*V* power supply and consumes about 2.2*A*. A separate +3.0*V* power supply with a current consumption of about 800*mA* is required for the divider operation (if installed).

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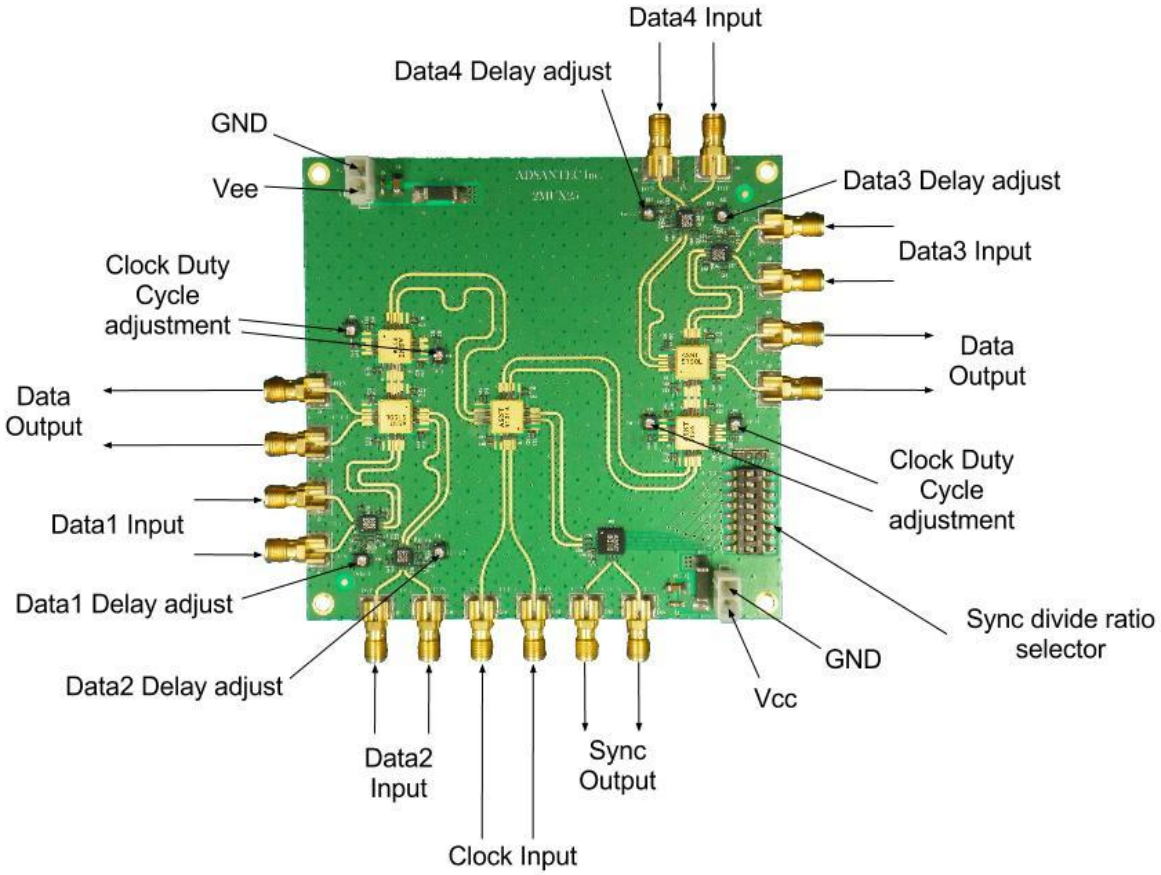
The board contains sixteen Emerson SMA connectors MFG PN: 142-0761-881, 50*Ohm* transmission lines to the device, and power supply decoupling networks.

Sync Output

The Sync Output can be configured to deliver any divide ratio from 1 to 256 in respect to the clock input frequency. Eight switches that represent an 8-bit binary code can set this ratio. The LSB starts at SW8 and the MSB ends at SW1. The decimal value of zero gives a divide value of 256. The decimal value of 1 gives a divide ratio of one, a value of 2 gives a ratio of two, a value of 3 gives a ratio of three, and so forth as shown in Table 1.



Operation

Apply a single-ended/differential, and AC/DC coupled clock with a frequency up to 22*GHz* to Clock Input. The allowed amplitude range is from 50*mV* to 1.0*V* peak to peak. In case of DC coupling, a common mode voltage level from -0.8*V* to 0.0*V* is required.

Apply two single-ended/differential, and AC/DC coupled data streams with a rate up to 22*Gbps* to Data1 Input and Data2 Input. The allowed amplitude range is from 50*mV* to 1.0*V* peak to peak. In case of DC coupling, a common mode voltage level of vcc – (single-ended swing/2) is required.

Connect Data Output to a 50*Ohm* oscilloscope input either single-ended (terminate the unused port to 50*Ohm*) or differentially. DC blocks are not required for those outputs.

Connect the Sync Output to the oscilloscope's trigger input single-ended (or differentially if possible). Terminate the unused Sync Output connector with 50*Ohm* through a DC block. **Note:** Failure to use a DC block with the termination may destroy the part.

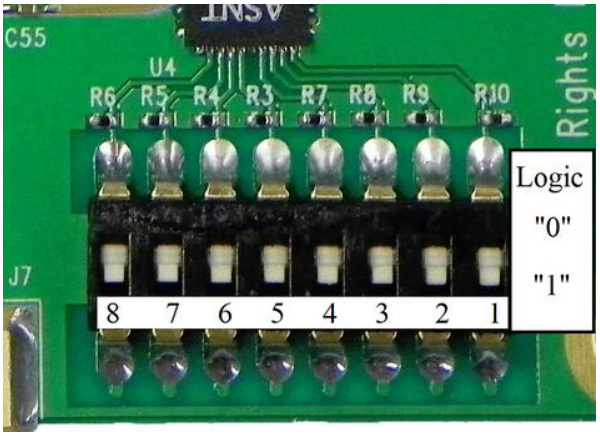
Terminate all other unused connectors with 50*Ohm* loads. DC blocks are not required for these outputs.

Set both power supplies to 0.0*V*. Connect the two power supplies to the two MOLEX connectors on board, where one supply is negative, and one is positive. The positive supply is required only if the programmable divider is installed. Set the current limit on the negative supply to 2.5*A* and increase the voltage to -3.3*V*. If a positive supply is used, set the current limit to 800*mA* and slowly increase the voltage to +3.0*V*.

Using a screwdriver, adjust Data1 Delay and/or Data2 Delay potentiometers to align the waveforms on the oscilloscope until the best waveform is achieved. Adjust one of the Clock Duty Cycle adjustment controls to achieve the desired duty cycle.

SYNC OUTPUT

The Sync Output can be configured to output any divide ratio from 1 to 256 from the clock input. It contains eight switches that represent 8 bits. The LSB starts at SW8 and the MSB ends at SW1. The binary value of zero gives a decimal n value of 256. Increasing binary values increases the decimal value n.



DIP SW #	n Divide Ratio	
8 7 6 5 4 3 2 1		
1 0 0 0 0 0 0 0	1	
0 1 0 0 0 0 0 0	2	
1 1 0 0 0 0 0 0	3	
0 0 1 0 0 0 0 0	4	
0 0 0 0 1 0 0 0	16	Eye diagram
. .		
0 1 1 1 1 1 1 1	127	pattern
1 1 1 1 1 1 1 0	254	pattern
0 0 0 0 0 0 0 0	256	

Table 1. Divider Ratio Controls

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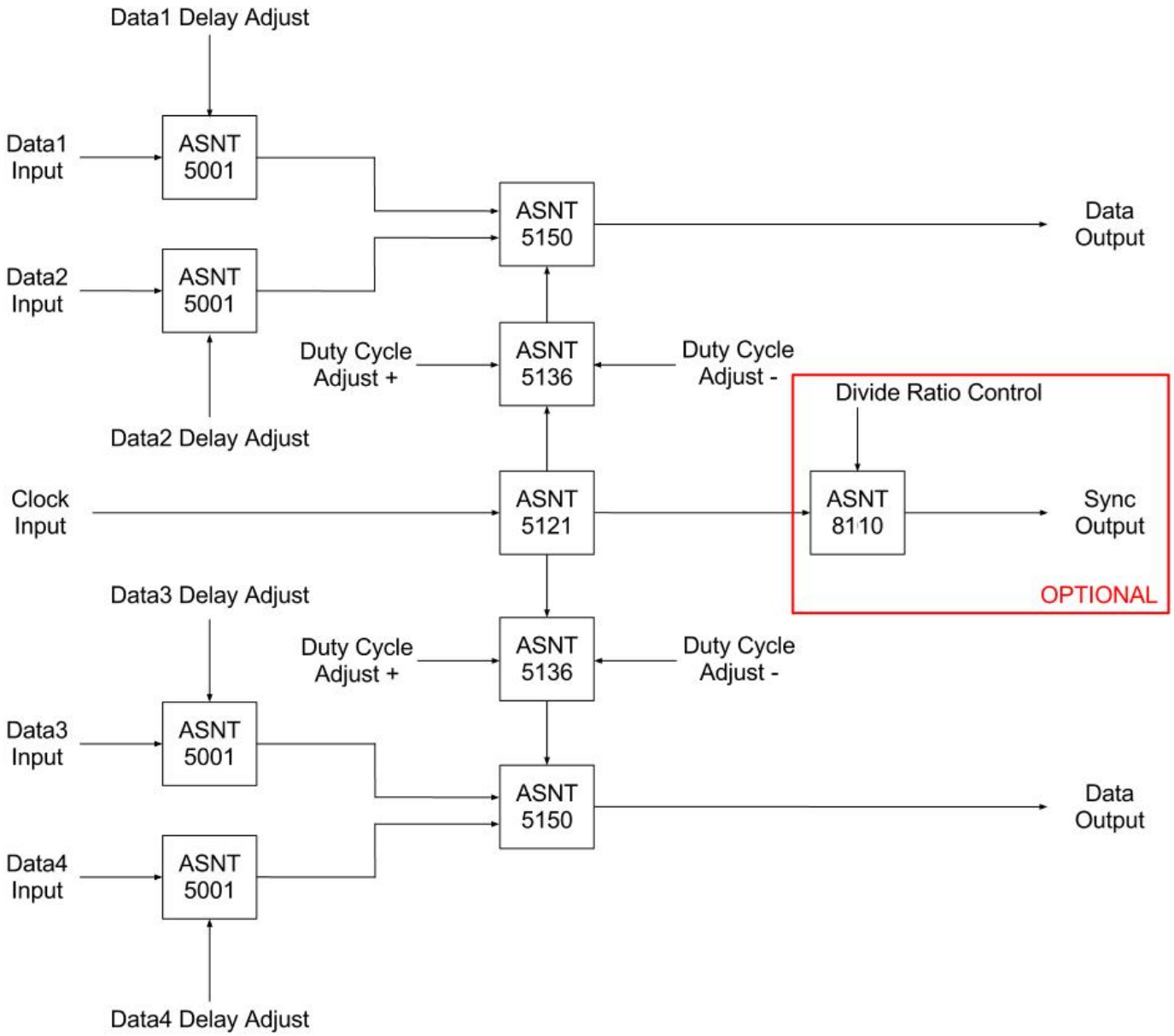
FUNCTIONAL BLOCK DIAGRAM



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REVISION HISTORY

Revision	Date	Changes
1.5.2	06-2021	Updated divider instructions and current draw Added Table 1
1.4.2	01-2021	Updated for use with ASNT8110
1.3.2	07-2019	Updated Letterhead
1.3.1	04-2019	Added connector description and P/N
1.2.1	05-2013	Revised title Revised description Revised operation
1.1.1	07-2012	Revised formatting
1.1	06-2012	Revised formatting and filename
1.0	05-2012	Initial release