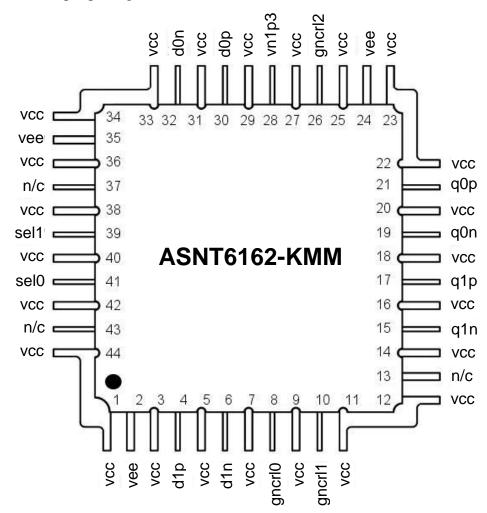
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# ASNT6162-KMM DC-17*GHz* Linear Non-Blocking Cross-Switch 2x2

- DC to 17*GHz* broadband operation
- Two differential CML-type input ports and two differential CML-type output ports
- Temperature-stabilized differential gain of approximately 0dB
- 1dB compression point of 0dBm
- DC-to-1*GHz* broadband channel selector ports
- Low jitter and limited temperature variation over industrial temperature range
- Single +4.5V or -4.5V power supply
- Power consumption: 1260mW
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 44-pin package



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### **DESCRIPTION**

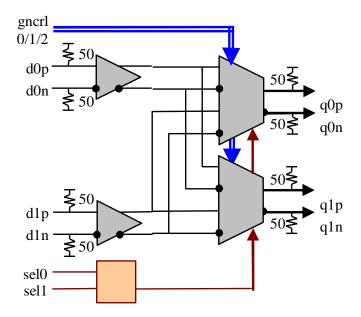


Fig. 1. Functional Block Diagram

The temperature stable ASNT6162-KMM linear non-blocking cross-switch 2x2 is intended for use in high-speed systems. The IC shown in Fig. 1 can deliver two different broad-band analog differential signals d0p/d0n and d1p/d1n to two differential outputs q0p/q0n and q1p/q1n with a nominal gain of 0dB. The gain can be fine-tuned using the 3-pin control port gncrl0/1/2 with accuracy of 0.5dB as shown in Table 1.

gncrl2 Gain, dB **Comments** gncrl1 gncrl0 -1.00 0 0 0 0 -0.5 0 0 1 -0.5 0 1 1 0 default state 1 0 0 0.5 1 0 1 0.5 0 1 1 1.0 1 1 1 1.0

Table 1. Gain Control

The assignment of inputs to outputs is performed through the external high-speed dual port sel1/sel2 that is referenced to vcc. The assignment logic is shown in Table 2.

Table 2. Channel Selection

sel1	sel0	Input connected to q0	Input connected to q1	Comments
0	0	d0	d0	default state
0	1	d1	d0	
1	0	d0	d1	
1	1	d1	d1	



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The part's I/Os support the CML-type interface with on chip 50*Ohm* termination to vcc, and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance. In particular, the specified output common-mode voltage level is guaranteed only in case of external single-ended 50*Ohm* DC termination to vcc.

### POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0V = ground), or a positive supply (vec = 0.0V = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. In any case, the input common mode voltage level is shifted down from vcc by a certain voltage of  $\Delta V_{ICM}$  as specified in ELECTRICAL CHARACTERISTICS. To have the input common mode voltage equal to ground, a floating negative supply scheme detailed in Fig. 2 should be used.

For the best performance, the external 50*Ohm* terminations for the outputs should be connected to **vcc**, but not to ground!

The part features an additional internal supply voltage vn1p3 that is also accessible through the corresponding pin. This pin is recommended to be left not connected but can be also used for adjustment of the output eye by applying an external voltage source within the range specified in ELECTRICAL CHARACTERISTICS. The external supply should be able to both source and sink a current of about 1mA.

Different PCB layouts will be needed for each different power supply combination.

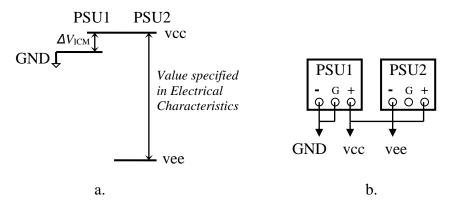


Fig. 2. Floating Negative Supply Scheme: Potential Diagram (a) and Schematic (b)

All the characteristics detailed below assume VCC = 0.0V = ground.

#### ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the Rev. 1.4.2



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absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-5.5	V
Power Consumption		1.5	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	${}^o\!C$
Storage Temperature	-40	+100	${}^o\!C$
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## **TERMINAL FUNCTION**

TERMINAL		AL	DESCRIPTION		
Name	No.	Type	1		
	High-speed Signals				
d0p	30	CML -	Differential high speed dat	ta inputs with internal SE 67 <i>Ohm</i>	
d0n	32	type	termination to vcc and SE 50 <i>Ohm</i> termination to virtual ground		
d1p	4	CML -			
d1n	6	type			
q0p	21	CML -	Differential high speed dat	ta outputs with internal SE 50 <i>Ohm</i>	
q0n	19	type	termination to vcc. Require external SE 50 <i>Ohm</i> termination to vcc		
q1p	17	CML -			
q1n	15	type			
			Control Sign	als	
sel0	41	SE	High-speed input with sele	ectable logic levels, (active: high; default:	
sel1	39	SE			
gncrl0	8	8 CMOS Low-speed input with internal 10 <i>KOhm</i> termination to vcc. For the			
gncrl1	10	CMOS	control logic see Table 1		
gncrl2	26	CMOS	Low-speed input with internal 10 <i>KOhm</i> termination to <b>vee</b> . For the		
	control logic see Table 1				
			<b>Supply and Terminati</b>	on Voltages	
Name	Description			Pin Number	
vcc	Positive power supply rail			1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22,	
				23, 25, 27, 29, 31, 33, 34, 36, 38, 40,	
	Negative power supply rail 42, 44  2, 24, 35				
vee	Negative power supply rail		e power supply rail	2, 24, 35	
vn1p3	Internal supply vcc-1.3V		l supply vcc-1.3V	28	
n/c	Not connected pins		connected pins	13, 37, 43	



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# **ELECTRICAL CHARACTERISTICS**

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
	Ge	eneral Pai	rameters		
vee	-4.7	-4.5	-4.3	V	±4.5%
vcc		0.0		V	External ground
Ivee		280		mA	
Power consumption		1260		mW	
Junction temperature	-25	50	125	$^{\circ}C$	
Input Analog (d0p/d0n, d1p/d1n)					
Bandwidth	DC		17	GHz	-3 <i>dB</i>
Common mode level	vcc-0.6	vcc-0.5	vcc-0.4	mV	
Input Noise Density		1.5		<i>nV</i> /sqrt( <i>Hz</i> )	
S11		-30		dB	at 1 <i>GHz</i>
		-8		dB	at 20 <i>GHz</i>
	Output Ai	nalog (q0 <sub>1</sub>	p/q0n, q1	p/q1n)	
Bandwidth	DC		17	GHz	-3 <i>dB</i>
Common mode level		vcc-0.55		V	With external 50 <i>Ohm</i>
					DC termination to vcc
S22		-27		dB	at 1 <i>GHz</i>
Small Signal Differential Gain	-1.0	0.0	+1.0	dB	
Output referred 1 <i>dB</i>		0		dBm	Single-Ended, 20 <i>GHz</i>
Compression Point					
2 <sup>nd</sup> harmonic		-55		dBc	at 1 <i>GHz</i>
		-35		dBc	at 20GHz
3 <sup>rd</sup> harmonic		-55		dBc	at 1 <i>GHz</i>
		-40		dBc	at 20 <i>GHz</i>
	Low-Spec		ols (gncrl (		
High logic level		VCC		V	
Low logic level	vee		V		
High-Speed Control (sel0, sel1)					
Bandwidth		1		GHz	
High logic level		VCC		V	
Low logic level		vcc-3.3		V	-2.4V default state
Input current			10	иA	sink or source
Additional Internal Supply (vn1p3)					
Nominal voltage value		vcc-1.3		V	when not connected
Adjustment range	vcc-1.6	)	vcc-1.0	V	with external supply
Current			1	mA	source or sink

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# PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the **vcc** plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6162-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

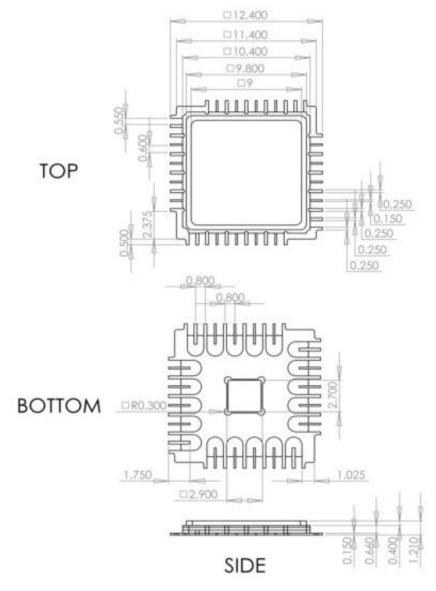


Fig. 3. CQFP 44-Pin Package Drawing (All Dimensions in mm)



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# **REVISION HISTORY**

Revision	Date	Changes		
1.4.2	05-2020	Updated Package Information		
1.3.2	07-2019	Updated Letterhead		
1.3.1	05-2018	Corrected the maximum frequency of operation		
1.2.1	04-2018	Added description of the vn1p3 pin (updated description, Terminal Functions, and Electrical characteristics)		
1.1.1	08-2017	Corrected power supply value		
1.0.1	08-2017	First release Corrected description		
0.2.1	08-2017	Corrected pin out diagram Removed IvIcrl pin and its description Corrected bandwidth		
0.1.1	07-2017	Pin name sel2 was changed to sel0 in description tables and in the block diagram. Channel selection table was corrected.		
0.0.1	08-2016	Preliminary release		