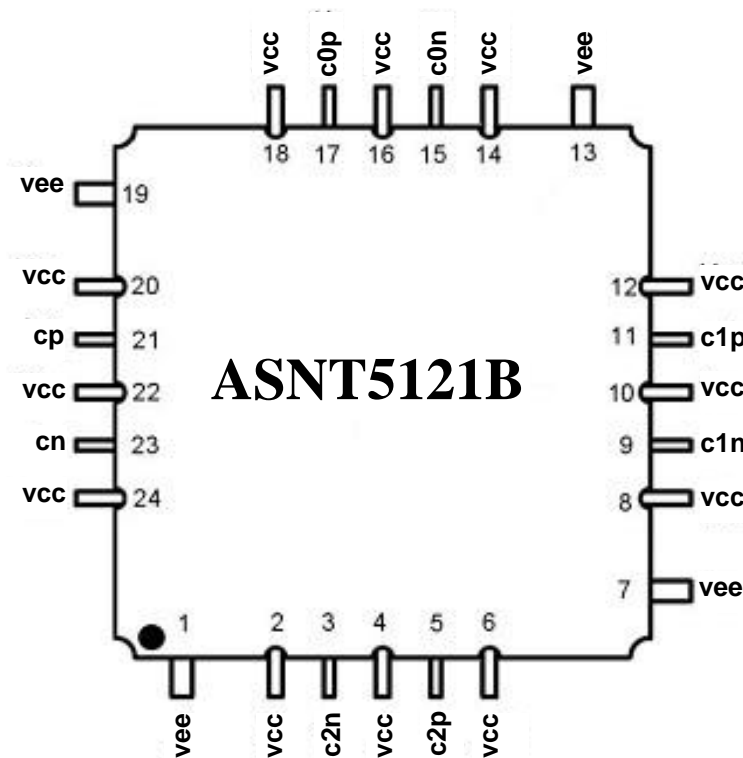




## ASNT5121B-KMC DC-35GHz Clock Distributor 1-to-3

- High-speed broadband Clock Amplifier and Distributor
- Exhibits low jitter and limited temperature variation over industrial temperature range
- One input differential signal port and three differential amplified output signal ports
- Matched phase delays for all outputs
- Fully differential CML input interfaces
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 760mW
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package





## DESCRIPTION

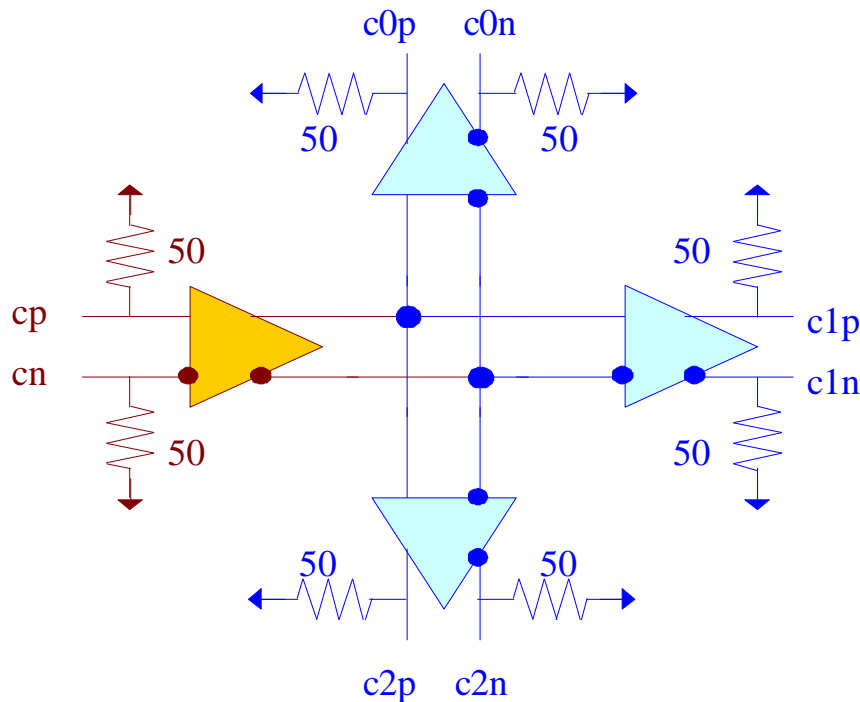


Fig. 1. Functional Block Diagram

The temperature stable ASNT5121B-KMC SiGe IC provides active broadband clock signal splitting, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can process a broadband high-speed clock input signal cp/cn and deliver three broadband high-speed clock phase matched output signals c0p/c0n, c1p/c1n, c2p/c2n.

The part's I/O's support the CML logic interface with on chip 50Ohms termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

## POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0V = ground and vee = -3.3V), or positive supply (vcc = +3.3V and vee = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50Ohms termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 0.0V and vee = -3.3V.**



## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.83	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
<b>High-Speed I/Os</b>			
cp	21	CML input	Differential high speed data/clock inputs with internal SE 50Ohms termination to vcc
cn	23		
c0p	17	CML output	Differential high speed data/clock outputs with internal SE 50Ohms termination to vcc. Require external SE 50Ohms termination to vcc
c0n	15		
c1p	11	CML output	Differential high speed data/clock outputs with internal SE 50Ohms termination to vcc. Require external SE 50Ohms termination to vcc
c1n	9		
c2p	5	CML output	Differential high speed data/clock outputs with internal SE 50Ohms termination to vcc. Require external SE 50Ohms termination to vcc
c2n	3		
<b>Supply and Termination Voltages</b>			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0V or -3.3V)		1, 7, 13, 19



## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I <sub>vee</sub>		230		mA	
Power consumption		760		mW	
Junction temperature	-40	25	125	°C	
<b>HS Input Clock (cp/cn)</b>					
Frequency	DC		35	GHz	
Swing	0.05		1.0	V	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
<b>HS Output Clock (c0p/c0n, c1p/c1n, c2p/c2n)</b>					
Frequency	DC		35	GHz	
Logic "1" level		vcc		V	
Logic "0" level		vcc-0.4		V	With external 50Ohms DC termination
Rise/Fall times	6	8	10	ps	20%-80%
Output Jitter		200		fs	Peak-to-peak
Duty cycle	45	50	55	%	For clock signal

## PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package's leads will be trimmed to a length of 1.0mm. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
  - 3.9.1 Solderability
  - 3.2.2 Solder Purity Maintenance
  - 3.9.2 Solderability Maintenance
  - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5121B-KMC. The first 9 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous



substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

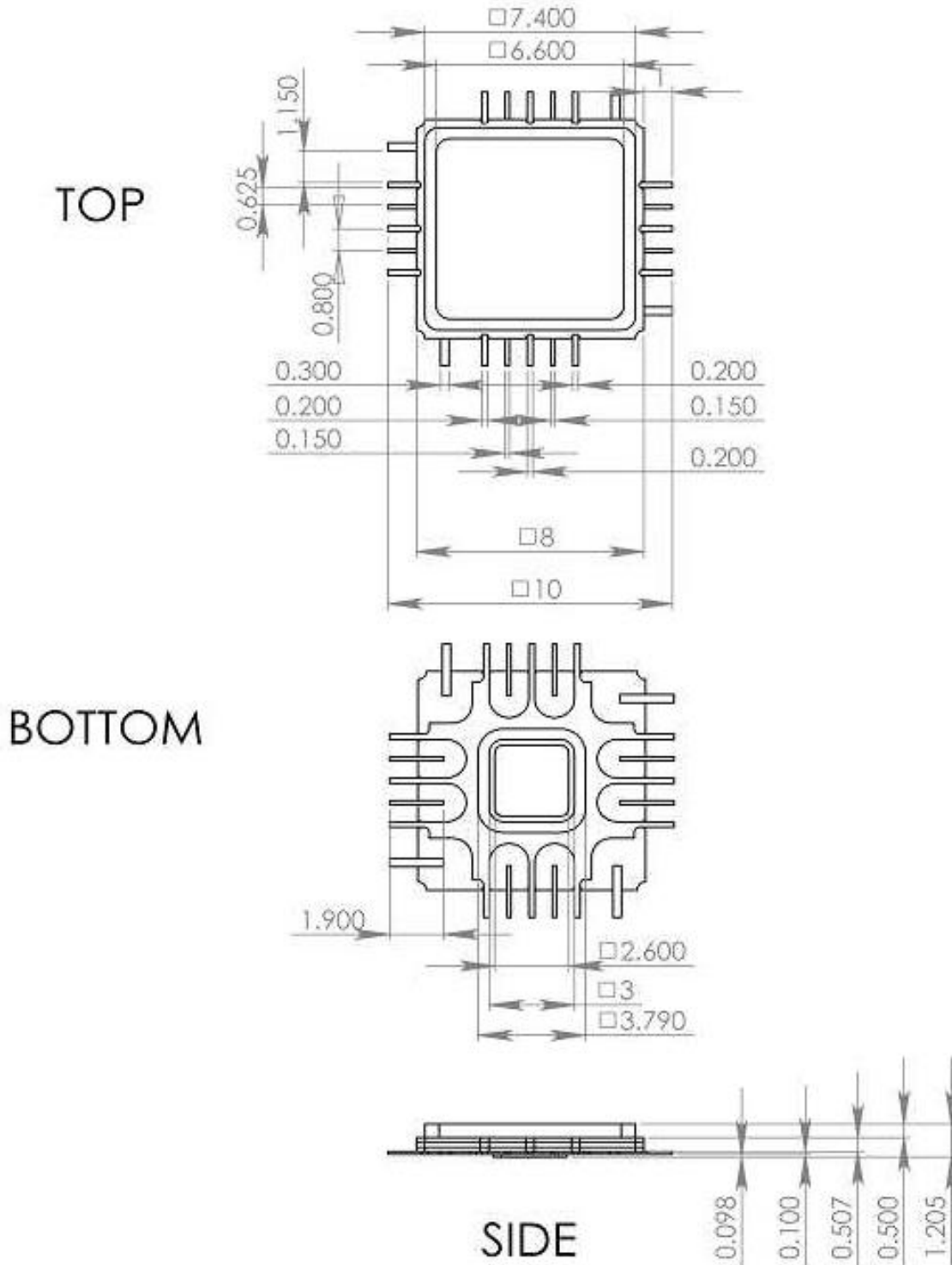


Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)



## REVISION HISTORY

Revision	Date	Changes
1.6.2	10-2024	Updated Package Information
1.5.2	05-2020	Updated Package Information
1.4.2	07-2019	Updated Letterhead
1.4.1	04-2015	Updated output jitter value
1.3.1	09-2014	Revised part as a clock distributor Updated pin out diagram Updated description to reflect operation as a clock distributor Updated terminal functions table Updated electrical characteristics table Updated package information section
1.2.1	08-2014	Updated maximum clock operational speed
1.1.1	03-2014	Updated maximum clock operational speed
1.0.1	10-2013	First release