ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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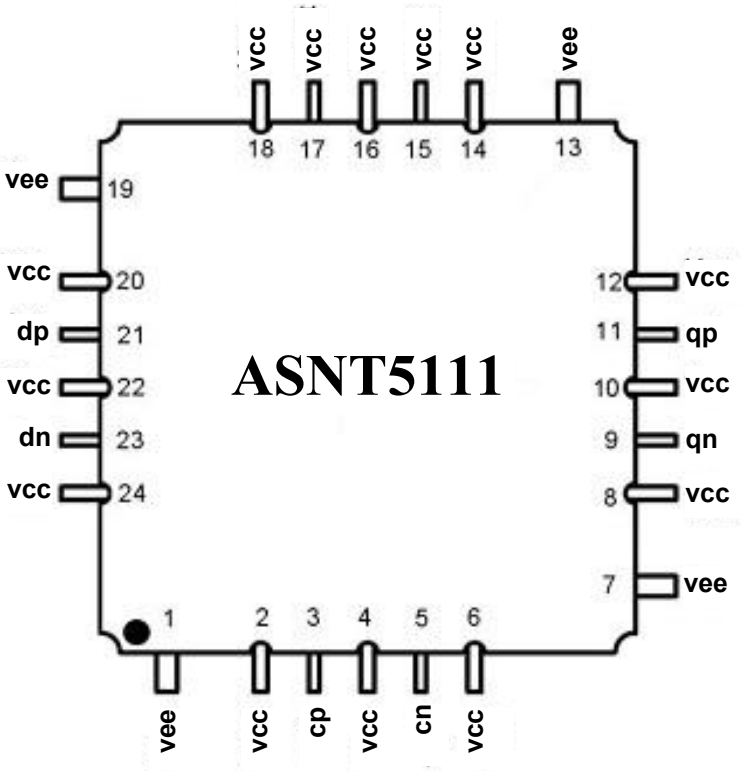
ASNT5111-KMC
DC-50*Gbps* D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 3*ps* set-up/hold time capability
- 88% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +4.0*V* or -4.0*V* power supply
- Power consumption: 520*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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DESCRIPTION

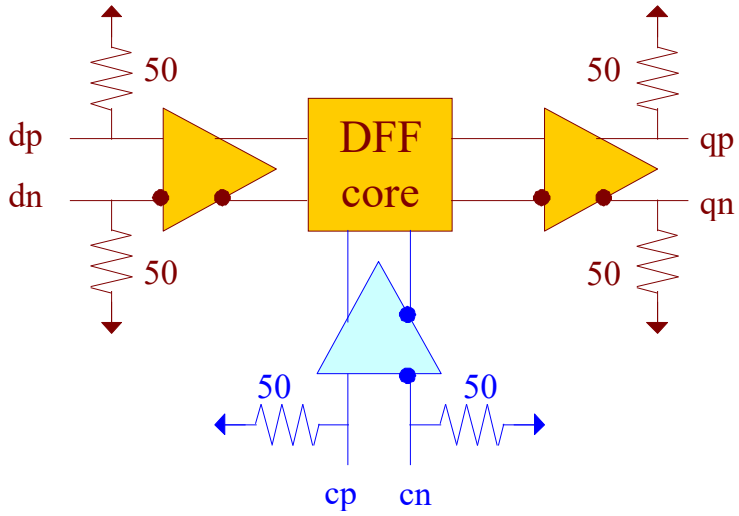

Fig. 1. Functional Block Diagram

The temperature stable ASNT5111-KMC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample a high-speed data signal dp/dn with a full-rate external clock cp/cn to create a full-rate retimed NRZ data output qp/qn.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground and vee = −4.0*V*), or a positive supply (vcc = +4.0*V* and vee = 0.0*V* = ground). For a positive supply, all I/Os need AC termination when connected to any devices with a 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -4.0*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-4.4	*V*
Power Consumption		0.58	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	21	CML input	Differential high-speed data inputs with internal SE 50*Ohm* termination to vcc
dn	23		
cp	3	CML input	Differential high-speed clock inputs with internal SE 50*Ohm* termination to vcc
cn	5		
qp	11	CML output	Differential high-speed data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
qn	9		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+4.0*V* or 0)	2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24
vee	Negative power supply (0*V* or -4.0*V*)	1, 7, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.8	-4.0	-4.2	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		130		*mA*	
Power consumption		520		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data (dp/dn)					
Data Rate	DC		50	*Gbps*	
Swing	0.05		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		50	*GHz*	
Swing	0.05		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Clock Phase Margin	86	88	90	*%*	
HS Output Data (qp/qn)					
Data Rate	DC		50	*Gbps*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Rise/Fall times			10	*ps*	20%-80%
Output Jitter			2.5	*ps*	Peak-to-peak

PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package's leads will be trimmed to a length of 1.0*mm*. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

The part's identification label is ASNT5111-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous

substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

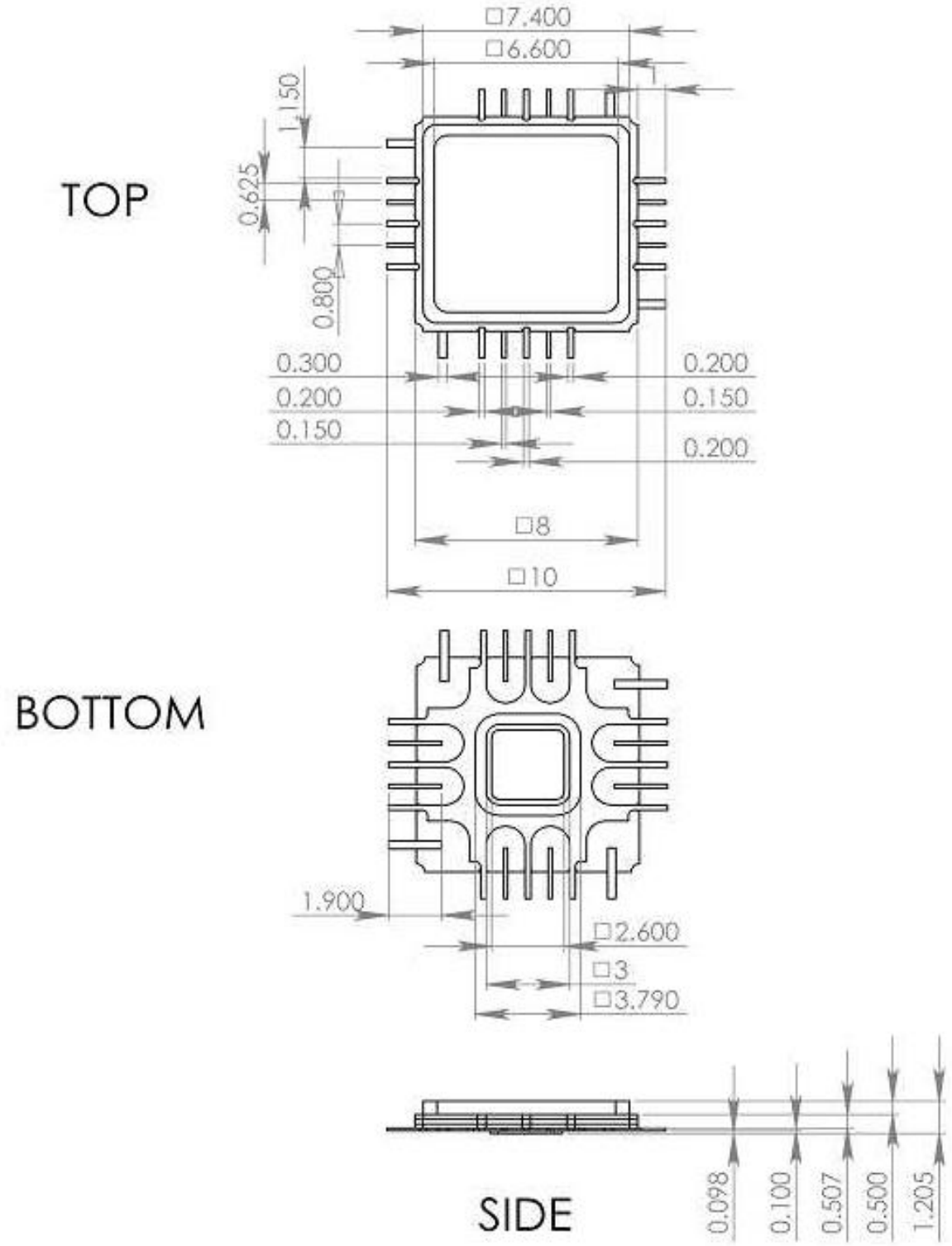

Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
2.4.2	04-2026	Minor formatting corrections
2.3.2	10-2024	Updated Package Information
2.2.2	02-2020	Updated Package Information
2.1.2	07-2019	Updated Letterhead
2.1.1	12-2016	Revised features Revised power supply configuration Revised absolute maximum ratings Revised electrical characteristics Revised package information
2.0.1	02-2013	Revised title Added package pin out drawing Revised functional block diagram Revised description Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Added package information and mechanical drawing Format correction
1.0	02-2008	First release