ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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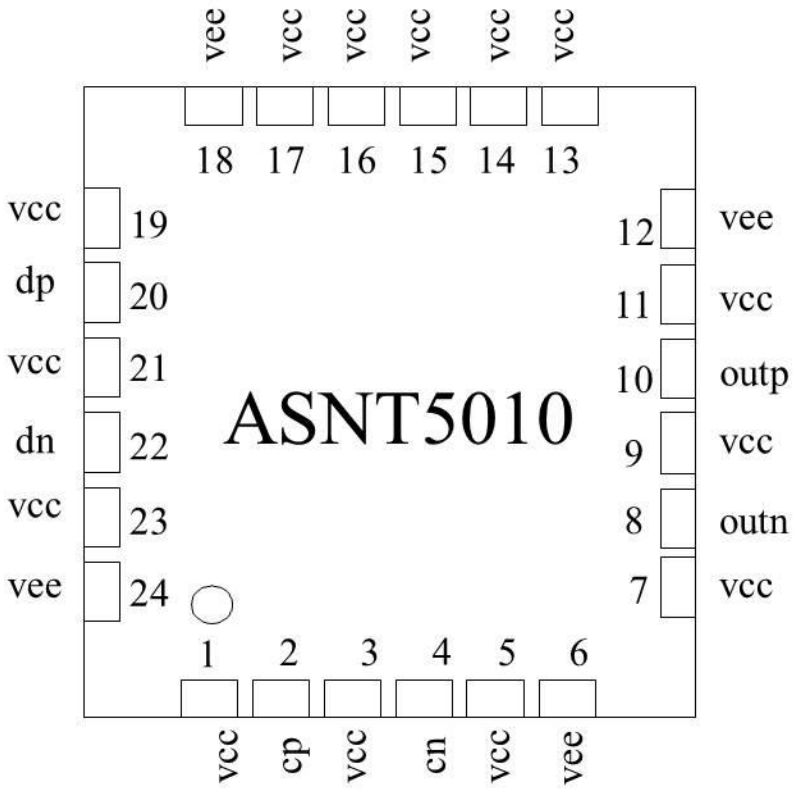
# ASNT5010-PQC
# DC-17*Gbps* D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 8*ps* set-up/hold time capability
- 89% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 415*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 24-pin package



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# DESCRIPTION

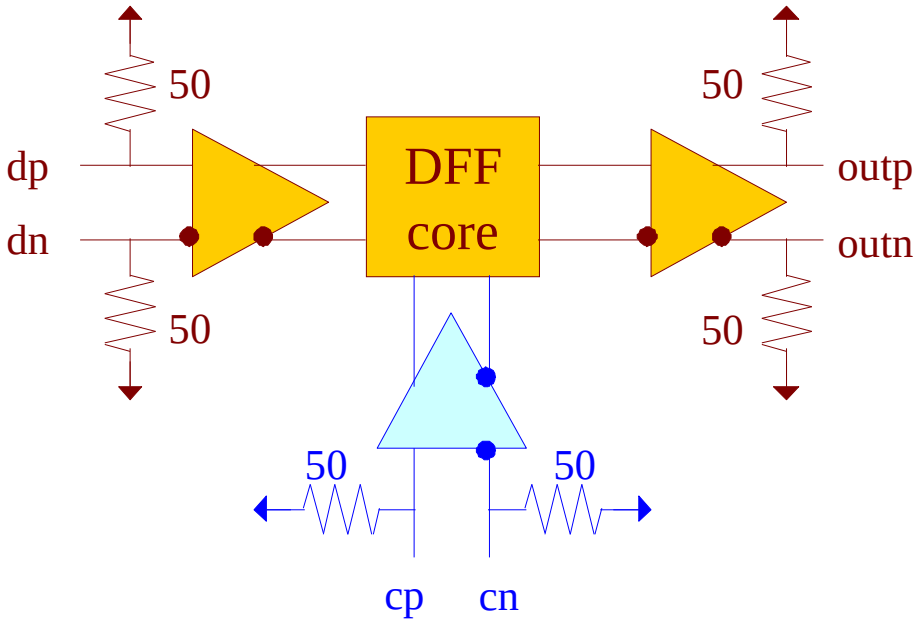


*Fig. 1. Functional Block Diagram*

The temperature stable ASNT5010-PQC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample a high-speed data signal dp/dn with a full-rate external clock cp/cn to create a full-rate retimed NRZ data output outp/outn. Sampling occurs on the falling clock edge.

The part's I/O's support the CML logic interface with on chip 50*Ohms* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

# POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

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**All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.**

# ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

*Table 1. Absolute Maximum Ratings*

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply Voltage (vee) | | -3.6 | *V* |
| Power Consumption | | 0.46 | *W* |
| RF Input Voltage Swing (SE) | | 1.0 | *V* |
| Case Temperature | | +90 | *ºC* |
| Storage Temperature | -40 | +100 | *ºC* |
| Operational Humidity | 10 | 98 | *%* |
| Storage Humidity | 10 | 98 | *%* |

# TERMINAL FUNCTIONS

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| **Name** | **No.** | **Type** | |
| **High-Speed I/Os** | | | |
| dp | 20 | CML input | Differential data inputs with internal SE 50*Ohms* termination to vcc |
| dn | 22 | | |
| cp | 2 | CML input | Differential clock inputs with internal SE 50*Ohms* termination to vcc |
| cp | 4 | | |
| outp | 10 | CML output | Differential data outputs with internal SE 50*Ohms* termination to vcc. Require external SE 50*Ohms* termination to vcc |
| outn | 8 | | |

| Supply and Termination Voltages | | |
|---|---|---|
| **Name** | **Description** | **Pin Number** |
| vcc | Positive power supply (+3.3*V* or 0) | 1, 3, 5, 7, 9, 11, 13, 14, 15, 16, 17, 19, 21, 23 |
| vee | Negative power supply (0*V* or -3.3*V*) | 6, 12, 18, 24 |

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# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| vee | -3.1 | -3.3 | -3.5 | *V* | ±6% |
| vcc | | 0.0 | | *V* | External ground |
| *I*vee | | 125 | | *mA* | |
| Power consumption | | 415 | | *mW* | |
| Junction temperature | -40 | 25 | 125 | *°C* | |
| **HS Input Data (dp/dn)** | | | | | |
| Frequency | DC | | 17 | *Gbps* | |
| Voltage swing, pk-pk | 0.05 | | 0.8 | *V* | Single ended, unused input not connected or AC terminated |
| CM Voltage Level | vcc-0.8<br>vcc | | | *V* | Must match for both inputs |
| Setup/Hold time | | 8 | | *ps* | Relative to negative clock edge |
| **HS Input Clock (cp/cn)** | | | | | |
| Frequency | DC | | 17 | *GHz* | |
| Voltage swing, pk-pk | 0.05 | | 0.8 | *V* | Single ended, unused input not connected or AC terminated |
| CM Voltage Level | vcc-0.8 | | vcc | *V* | Must match for both inputs |
| Clock Phase Margin | 85 | 87 | 89 | *%* | |
| **HS Output Data (outp/outn)** | | | | | |
| Data rate | DC | | 17 | *Gbps* | |
| Latency | | 67 | | *ps* | From Clock input to Data output |
| Logic “1” level | | vcc | | *V* | |
| Logic “0” level | | vcc-0.4 | | *V* | With external 50*Ohms* DC termination |
| Clock-to-output delay | 55 | 65 | 75 | ps | |
| Rise/Fall times | | 20 | | *ps* | 20%-80% |
| Output Jitter | | 10 | | *ps* | Peak-to-peak |
| **Receiver Sensitivity** | | | | | |
| Differential Voltage Swing for each P and N input | 25 | | 400 | *mV* | Peak-to-peak |
| Differential Voltage Swing between the P and N inputs | 50 | | 800 | *mV* | Peak-to-peak |
| ViL Single Ended – Centered on CM Voltage | -25 | | | *mV* | P signal referenced to N signal |
| ViH Single Ended – Centered on CM Voltage | +25 | | | *mV* | P signal referenced to N signal |

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| Simulated Timing Data | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Test Case** | | | | | | | | |
| | **Slow** | | | **Nominal** | | | **Fast** | | |
| | **-25C** | **125C** | **Δ** | **-25C** | **125C** | **Δ** | **-25C** | **125C** | **Δ** |
| **Propagation Delay, ps** | 78.3 | 93.8 | **15.5** | 75.4 | 89.7 | **14.3** | 74.1 | 88.1 | **14.0** |
| **Set Up Time, ps** | 4.1 | 3.1 | **1.0** | 3.2 | 2.3 | **0.9** | 2.4 | 1.8 | **0.6** |
| **Hold Time, ps** | -6.0 | -4.8 | **1.2** | -5.2 | -4.2 | **1.0** | -4.7 | -3.8 | **0.9** |

# PACKAGE INFORMATION

The die is housed in a standard 24-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply or power for the negative supply.

The part's identification label is ASNT5010-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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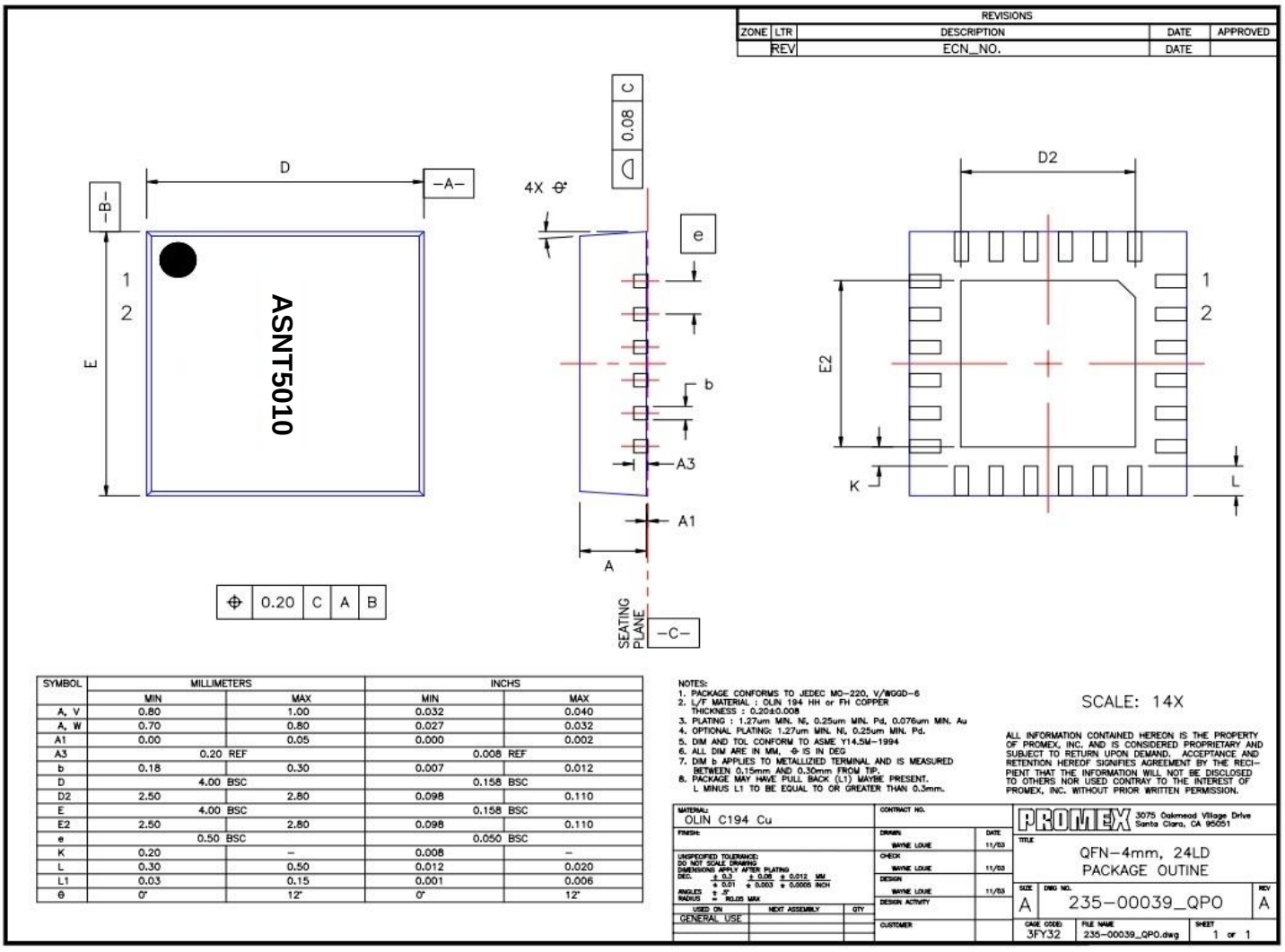


| SYMBOL | MILLIMETERS | | INCHS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A, V | 0.80 | 1.00 | 0.032 | 0.040 |
| A, W | 0.70 | 0.80 | 0.027 | 0.032 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A3 | 0.20 REF | | 0.008 REF | |
| b | 0.18 | 0.30 | 0.007 | 0.012 |
| D | 4.00 BSC | | 0.158 BSC | |
| D2 | 2.50 | 2.80 | 0.098 | 0.110 |
| E | 4.00 BSC | | 0.158 BSC | |
| E2 | 2.50 | 2.80 | 0.098 | 0.110 |
| e | 0.50 BSC | | 0.050 BSC | |
| K | 0.20 | – | 0.008 | – |
| L | 0.30 | 0.50 | 0.012 | 0.020 |
| L1 | 0.03 | 0.15 | 0.001 | 0.006 |
| θ | 0° | 12° | 0° | 12° |

*Fig. 2. QFN 24-Pin Package Drawing (All Dimensions in mm)*

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# REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 3.7.2 | 11-2024 | Specified sampling edge of clock, added timing simulation data, corrected input swing description |
| 3.6.2 | 02-2020 | Updated Package Information |
| 3.5.2 | 07-2019 | Updated Letterhead |
| 3.5.1 | 02-2019 | Added setup/hold time to Electrical Characteristics table |
| 3.4.1 | 08-2018 | Corrected latency specifications |
| 3.3.1 | 08-2018 | Added latency specifications |
| 3.2.1 | 06-2018 | Updated electrical characteristics |
| 3.1.1 | 02-2013 | Revised title<br>Revised package information |
| 3.0.1 | 01-2013 | Added package pin out drawing<br>Revised functional block diagram<br>Added power supply configuration<br>Added absolute maximum ratings<br>Revised terminal functions<br>Revised electrical characteristics<br>Added package information and mechanical drawing<br>Format correction |
| 2.0 | 07-2009 | Revised electrical characteristics |
| 1.0 | 02-2008 | First release |