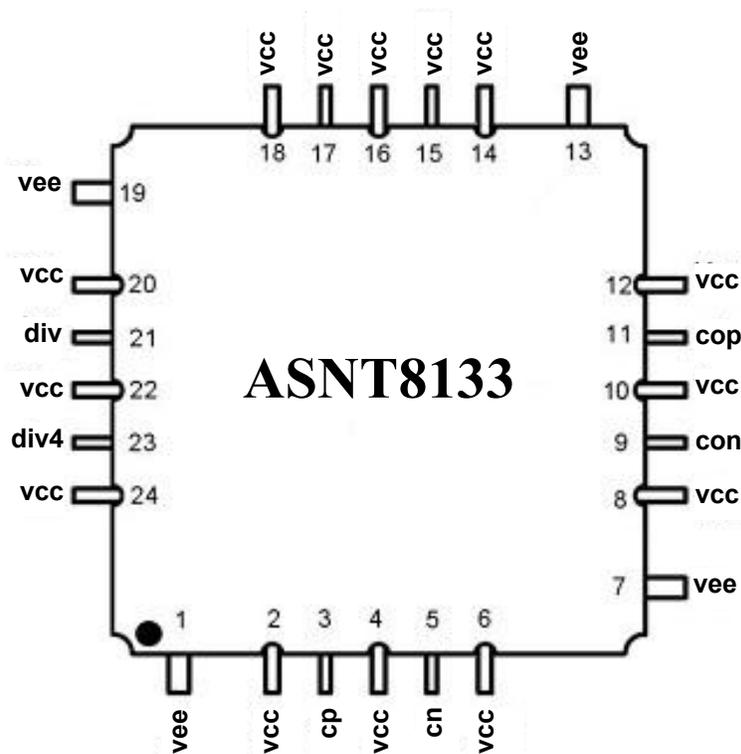




ASNT8133-KMC DC-50GHz High-Speed Clock Divider by 1, 2, or 4

- Wide input clock frequency range from DC to 50GHz
- Selectable Forwarded, Divided-by-2, or Divided-by-4 output
- 50% duty cycle of the divided clock signals
- Fully differential CML input interface
- Fully differential CML output interface with 400mV single-ended swing
- CMOS 3.3V control signals
- Single +3.3V or -3.3V power supply
- Power consumption: 845mW at full operational speed
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



DESCRIPTION

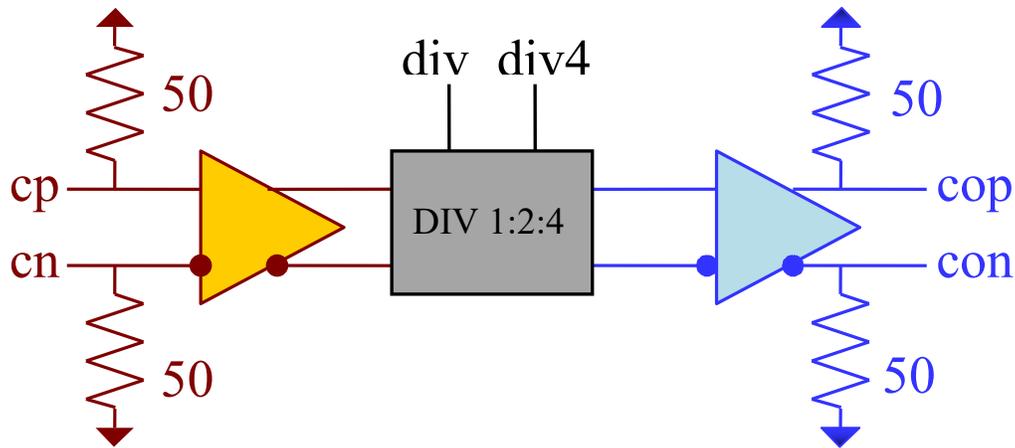


Fig. 1. Functional Block Diagram

ASNT8133-KMC is a high-speed, low-power divider by-1, by-2, or by-4 with increased sensitivity. The part shown in Fig. 1 accepts a CML input clock signal cp/cn with the speed from DC to maximum operational frequency and provides a clean 50% duty cycle output signal cop/con with its frequency defined by the states of CMOS level div and div4 control signals as shown in Table 1.

Table 1. Clock frequency division control signals

div	div4	Output Frequency
"0"	x	Forwarded, no division
"1"	"0"	Divided by 2
"1"	"1"	Divided by 4

The part's high-speed I/Os support the CML logic interface with on chip 50Ohms termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0V =ground and vee = -3.3V), or a positive supply (vcc = +3.3V and vee = 0.0V = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50Ohms termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0V and vee = -3.3V.



ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.92	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
cp	3	CML input	Differential clock input with internal SE 50Ohms termination to vcc
cn	5		
cop	11	CML output	Differential clock outputs with internal SE 50Ohms termination to vcc. Require external SE 50Ohms termination to vcc
con	9		
Static I/Os			
div	21	CMOS Input	Output clock frequency select signals. Pull-up to vcc
div4	23		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0V)		2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24
vee	Negative power supply (0V or -3.3V)		1, 7, 13, 19



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I _{vee}		255		mA	
Power consumption		845		mW	
Junction temperature	-25	50	125	°C	
HS Input Clock (cp/cn)					
Maximum Frequency	50			GHz	
Swing	120		800	mV	Differential or SE, p-p
CM Voltage Level	vcc-0.8	vcc-0.2	vcc	mV	Must match for both inputs
Output Divided Clock (cop/con)					
Maximum Forwarded Frequency	25			GHz	div = "0"
Maximum Divided Frequency	25			GHz	div = "1"
Logic "1" level		vcc		V	
Logic "0" level		vcc-0.4		V	With external 50Ohms termination
Duty cycle	45	50	55	%	
Additive Jitter		TBD		ps	Peak-to-peak
Divide Ration Control Signals (div, div4)					
Logic "1" level	V _{CC} -0.4			V	
Logic "0" level		V _{EE} +0.4		V	

PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package's leads will be trimmed to a length of 1.0mm. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
 - 3.9.1 Solderability
 - 3.2.2 Solder Purity Maintenance
 - 3.9.2 Solderability Maintenance
 - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8133-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

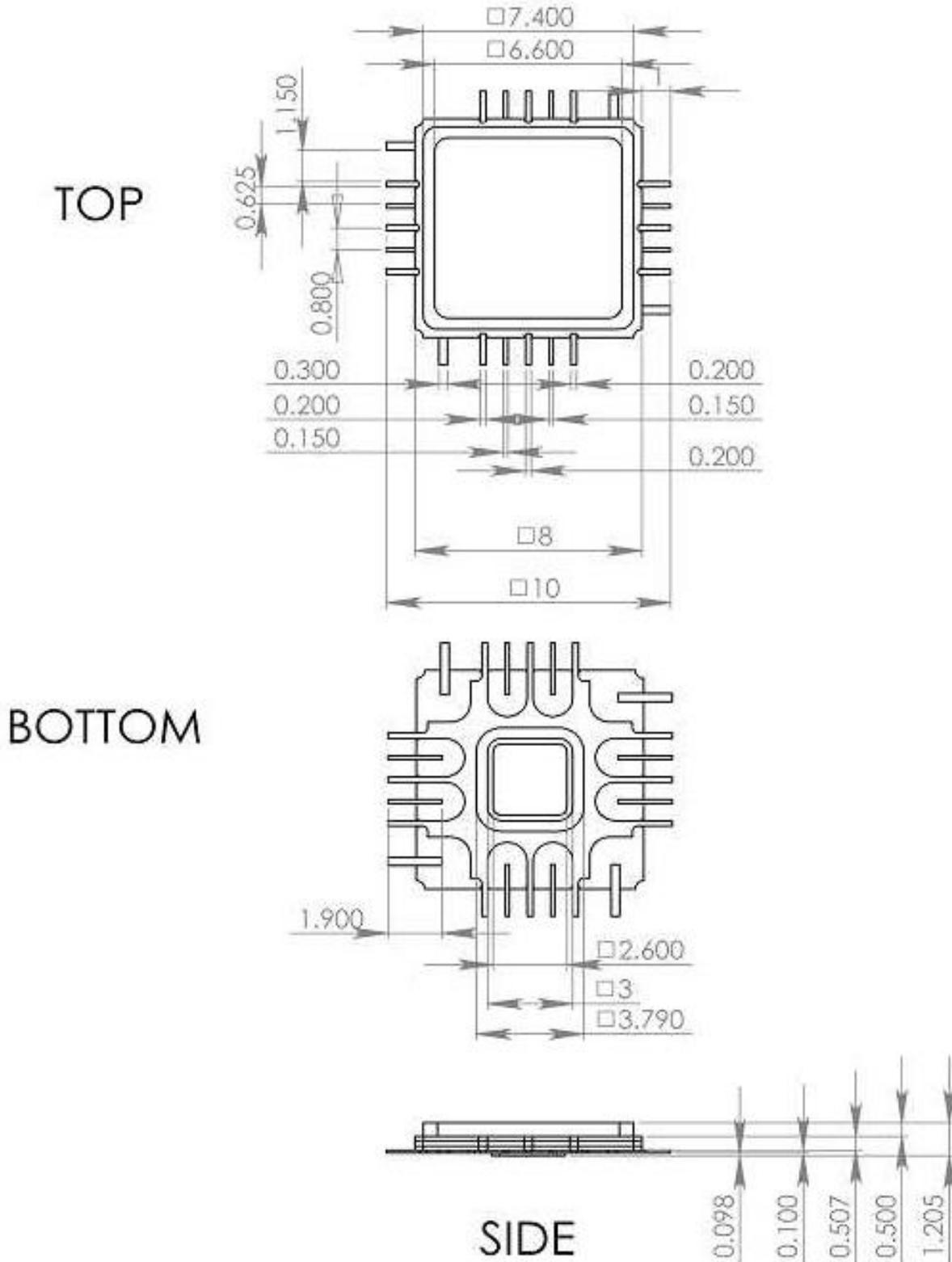


Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)



This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.3.2	07-2025	Updated Package Information
1.2.2	02-2020	Updated Package Information
1.1.2	07-2019	Updated Letterhead
1.1.1	01-2016	Revised Description section Added content to Electrical Characteristics table
1.0.1	07-2015	First release
1.0.0	03-2015	Preliminary release