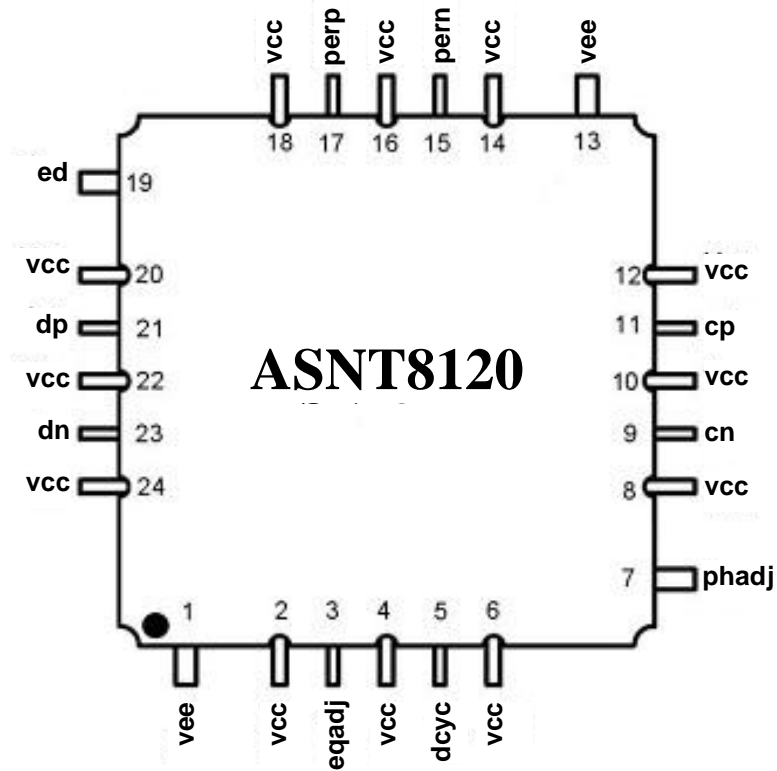




ASNT8120-KMC DC-28.6Gbps Linear Phase Detector

- Broadband linear phase detector with differential output
- Adjustable data input equalizer with a by-pass possibility
- Selectable input clock multiplier by 2 with externally adjustable duty cycle
- Output clock duty cycle indicator
- Data edge density indicator
- Fully differential CML input data and clock interfaces
- Fully differential CML-type output phase error interface with 300mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 760mW
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package





DESCRIPTION

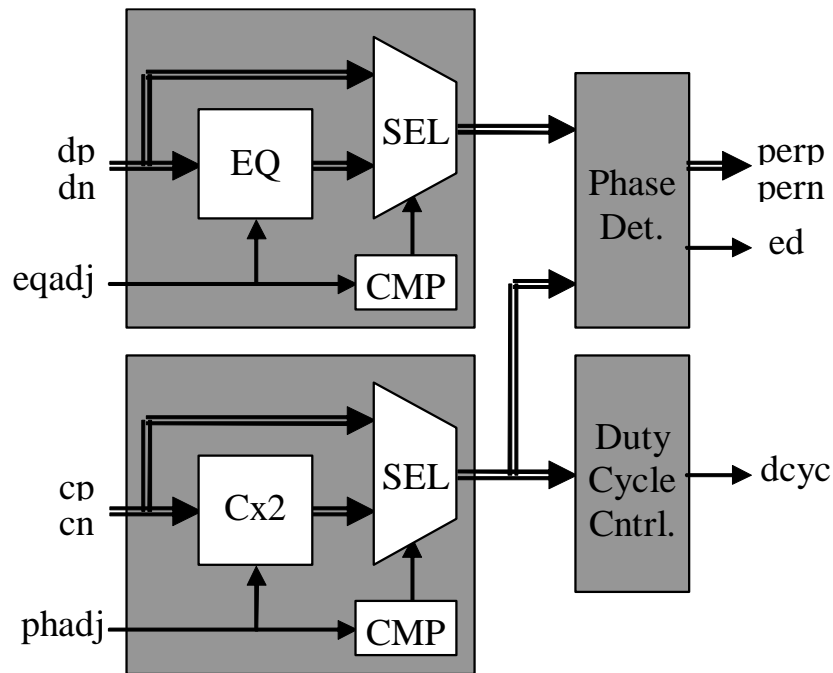


Fig. 1. Functional Block Diagram

The ASNT8120-KMC SiGe IC shown in Fig. 1 provides a differential phase error signal **perp/pern** that indicates the phase difference between the data **dp/dn** bit transitions and the edges of the input clock **cp/cn**. The input data spectrum can be corrected by the equalizer **EQ** with a frequency response adjustable by the variation of the control input signal **eqadj** within the voltage range from **vcc** to **vcc-2V**. The lower values of **eqadj** disable the equalizer and send the input data signal directly to the phase detector block **PhaseDet**. The input clock can be delivered to the phase detector block either directly or through the multiplier by 2 **Cx2** with its output duty cycle adjustable by means of the **phadj** control voltage. The **phadj** control operates similar to **eqadj** with a tunable range from **vcc** to **vcc-2V** and a multiplication enabling threshold value of **vcc-2V**.

The phase detector also provides two single-ended signals **ed** and **dcyc**. The **ed** output delivers an analog voltage indicating the number of transitions in the data bit stream. The duty cycle control block **DutyCycleCntrl** generates the analog signal **dcyc** that indicates the clock duty cycle deviation from 50%.

The part's differential input clock and data ports support the CML logic interface with on chip **50Ohm** termination to **vcc** and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also **POWER SUPPLY CONFIGURATION**). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in **ELECTRICAL CHARACTERISTICS**. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The output phase error port supports a CML-type interface with on chip **100Ohm** termination to **vcc** and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also **POWER SUPPLY CONFIGURATION**). The differential DC signaling mode is recommended for optimal performance.

Equalizer

The simulated equalizer frequency response at different values of the eqadj signal is shown in Fig. 2 and its simulated control characteristic is shown in Fig. 3.

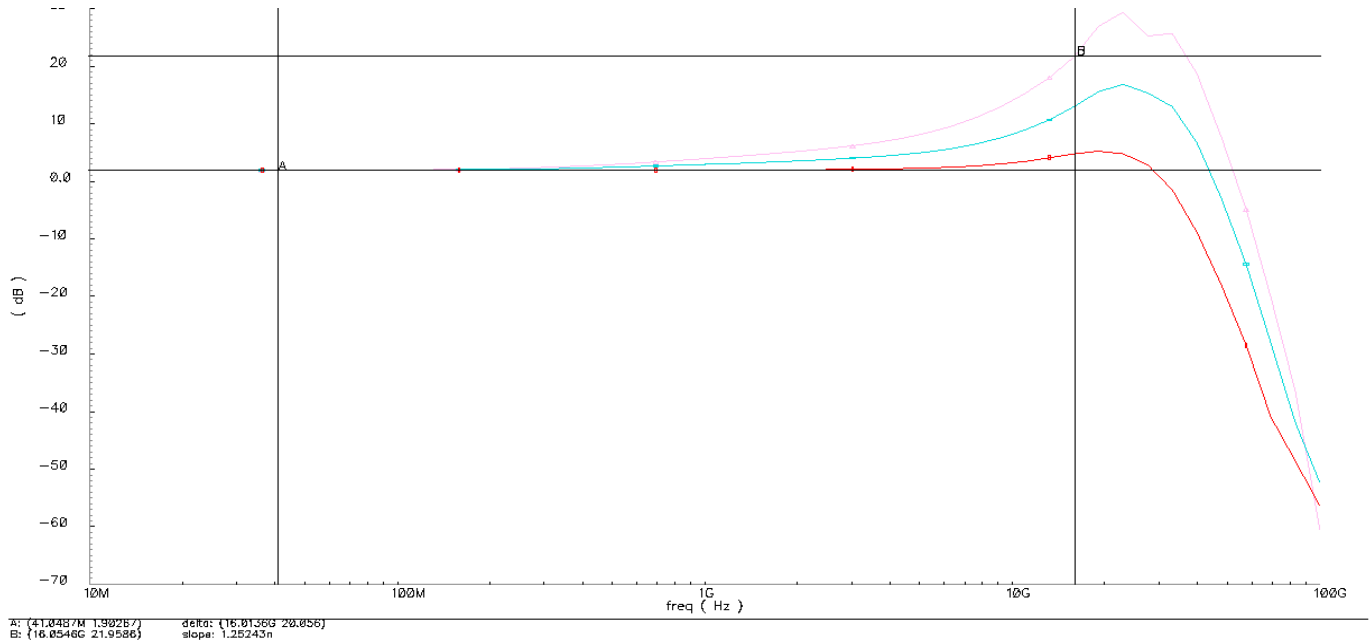


Fig. 2. Equalizer Frequency Response at Full, Half, and No Gain

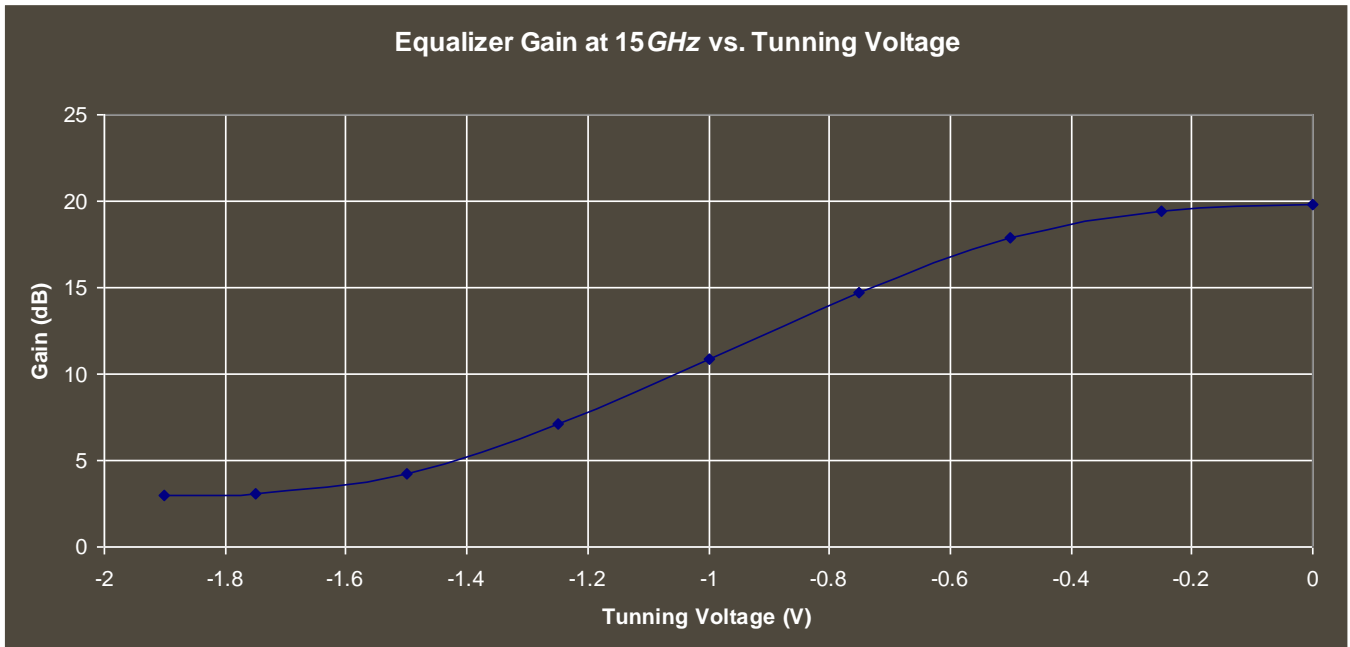


Fig. 3. Equalizer Control Characteristic



Clock Multiplier

The multiplier operation is illustrated in Fig. 4 which shows the *dcyc* output voltage vs. the *phadj* input duty cycle control value for the case of multiplication by 2 of a 14.3GHz input clock.

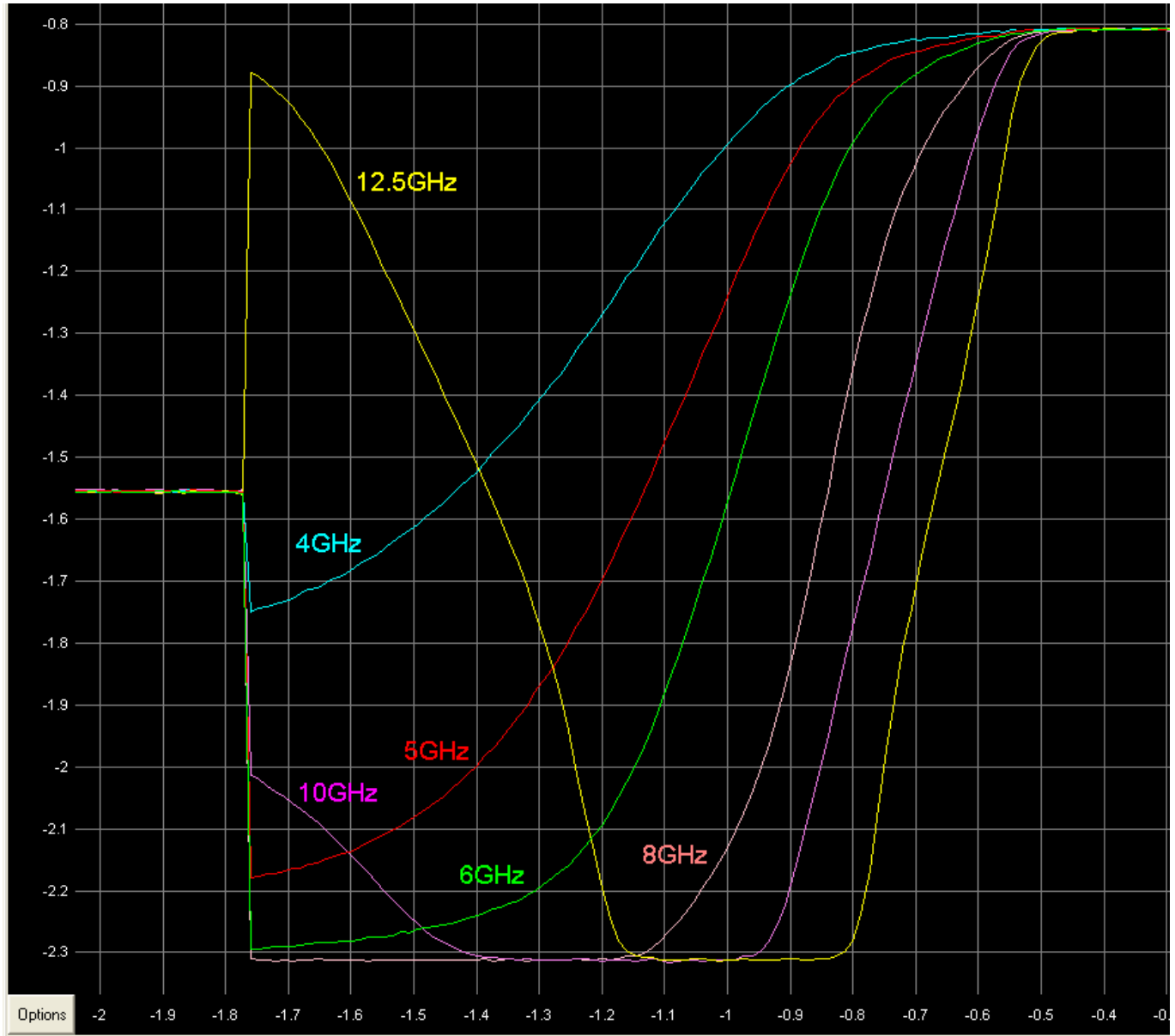


Fig. 4. Measured Duty Cycle Voltage vs. *phadj* Input Control Voltage at Different Clock Frequencies

Phase Detector

Transfer characteristics of the phase detector at 10Gb/s (measured) and 28.6Gb/s (simulated) data rates are shown in Fig. 5 and Fig. 6 respectively.

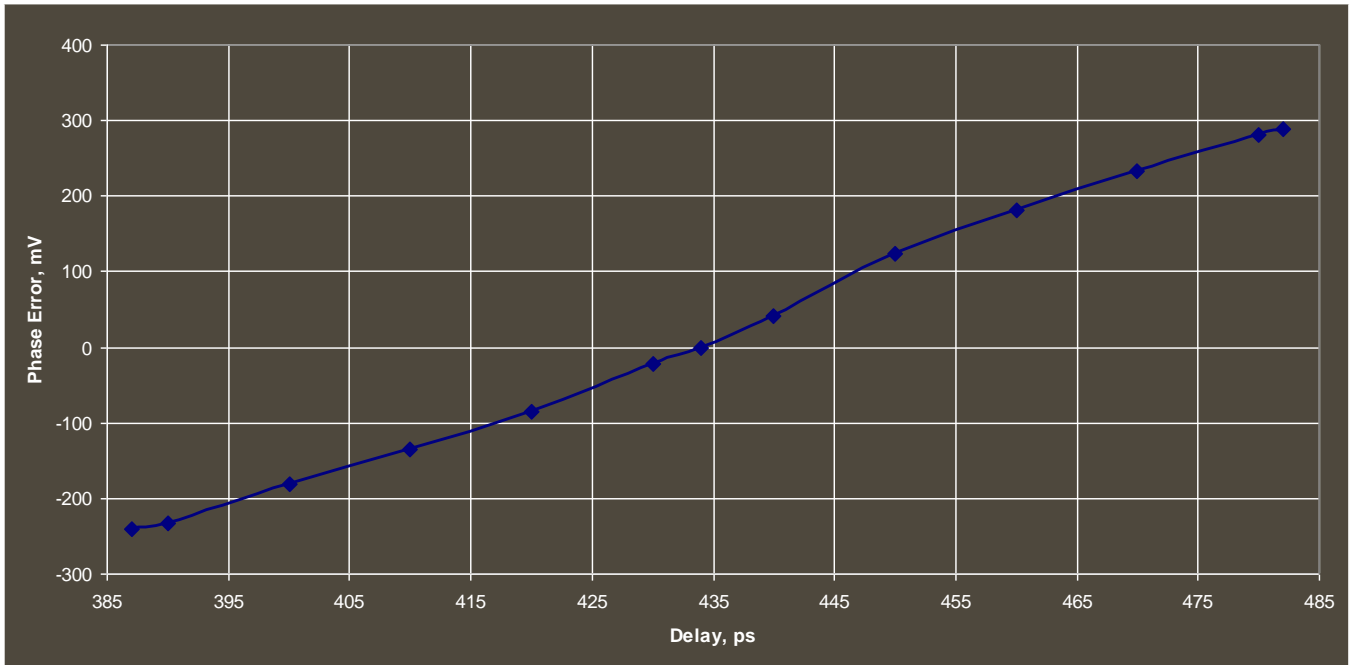


Fig. 5. Measured Phase Detector Characteristic at 10Gb/s Data Rate

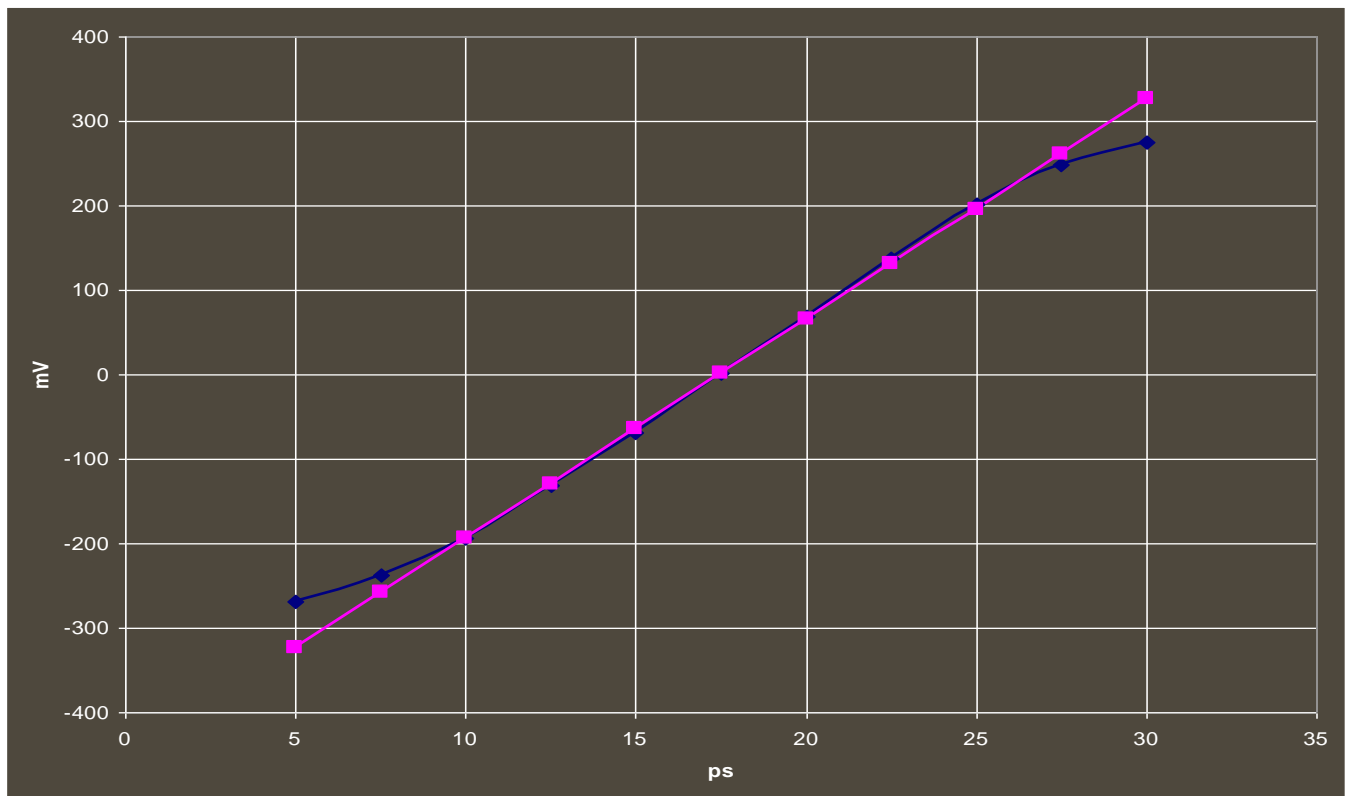


Fig. 6. Simulated Phase Detector Characteristic at 28.6Gb/s Data Rate

The edge density detector operation is illustrated in Fig. 7 for 10Gb/s data rate.

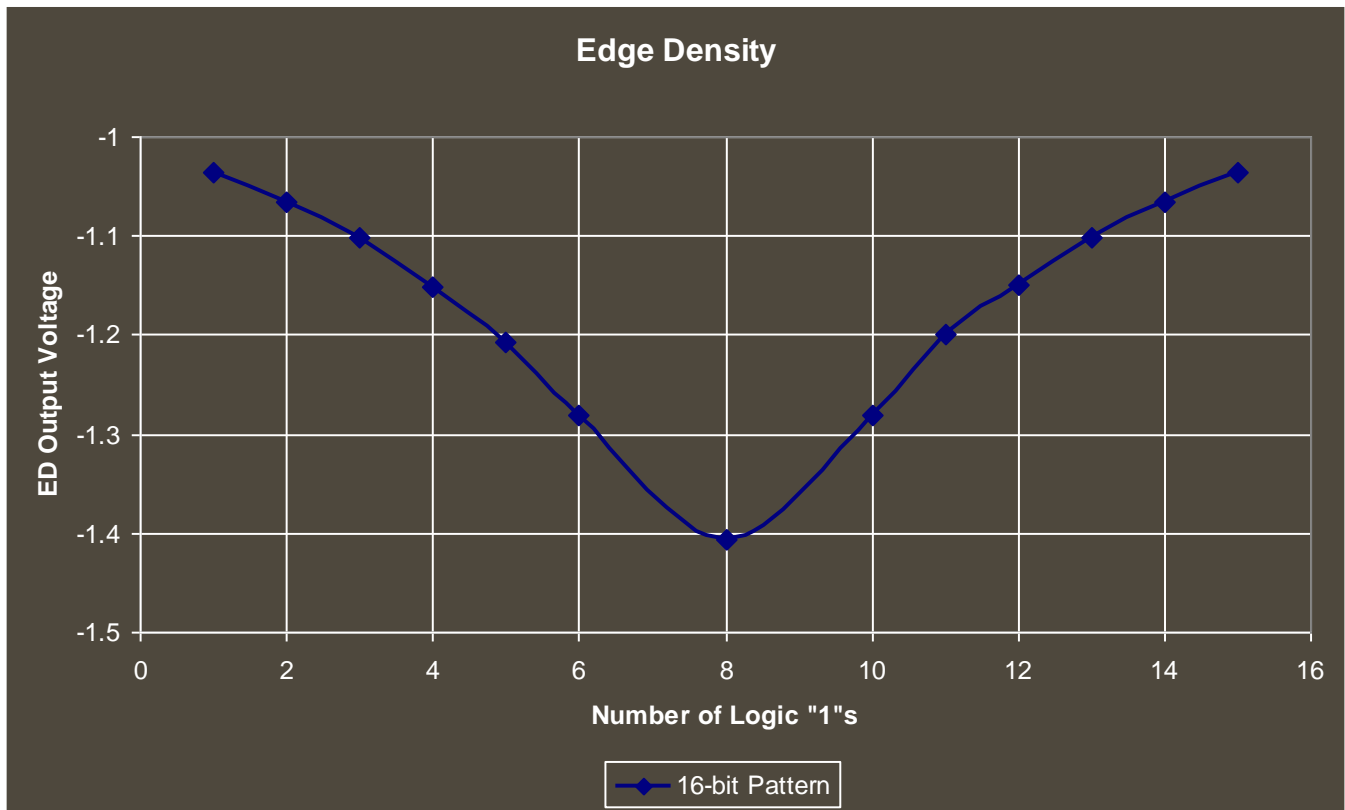


Fig. 7. Measured Edge Density Characteristic at 10Gb/s Data Rate

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply ($v_{cc} = 0.0V = \text{ground}$ and $v_{ee} = -3.3V$), or positive supply ($v_{cc} = +3.3V$ and $v_{ee} = 0.0V = \text{ground}$). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50Ω termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume $v_{cc} = 0.0V$ and $v_{ee} = -3.3V$.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed v_{cc}).



Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.84	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
dp	21	CML input	Differential high-speed data input signals with internal SE 50Ohm termination to vcc
dn	23		
cp	11	CML input	Differential high-speed clock input signals with internal SE 50Ohm termination to vcc
cn	9		
perp	17	Analog output	Differential phase error output with internal SE 100Ohm terminations to vcc.
pern	15		
eqadj	3	Analog input	Equalization level adjust / equalizer enable
phadj	7	Analog input	Duty cycle adjust / clock multiplier enable
dcyc	5	Analog output	Duty cycle indicator signal
ed	19	Analog output	Edge density indicator signal
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0V or -3.3V)		1, 13



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
Ivee		230		mA	
Power consumption		760		mW	
Junction temperature	-40	25	125	°C	
HS Input Data (dp/dn)					
Data Rate	DC		28.6	Gbps	
Swing	10		300	mV	Differential or SE, p-p
CM Voltage Level	vcc-0.3		vcc	V	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		14.3	GHz	
Swing	10		300	mV	Differential or SE, p-p
CM Voltage Level	vcc-0.3		vcc	V	Must match for both inputs
Phase Error Output (perp/pern)					
Linear range		300		mV	Single-ended
CM Voltage Level		vcc-0.275		V	
Tuning ports (eqadj, phadj)					
Linear control range	-2		0	V	
Switching threshold		-2		V	
Output indicators (ed, dcyc)					
Voltage range	-3.3		0.0	V	

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 8. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8120-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.



REVISION HISTORY

Revision	Date	Changes
2.1.2	02-2020	Updated Package Information
2.0.2	07-2019	Updated Letterhead
2.0.1	03-2013	Revised title Revised description Revised absolute maximum ratings Revised terminal functions Revised electrical characteristics Revised package information Added mechanical drawing Revised format
1.2.1	08-2012	Updated formatting
1.1.1	08-2012	Added pin out drawing Added power supply configuration text Added absolute maximum ratings table Revised electrical characteristics section Revised package information section Added revision history Modified format
1.0	07-2009	First release