ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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ASNT_ED45_2CH
2 Channel Error Detector
User Guide

Overview

The ADSANTEC Inc. ASNT_ED45_2CH has two independent error detecting channels. The unit accepts a NRZ (Non Return to Zero) industry standard PRBS patterns. The following are the selectable PRBS patterns that can be used: PRBS7, PRBS9, PRBS11, PRBS15, PRBS17, PRBS20, PRBS23, PRBS29 and PRBS31. Data can be applied single-ended or differentially. Data is clocked by a single-ended clock input. A single-ended clock output is provided by the clock input. A functional block diagram is shown below.

Getting Started
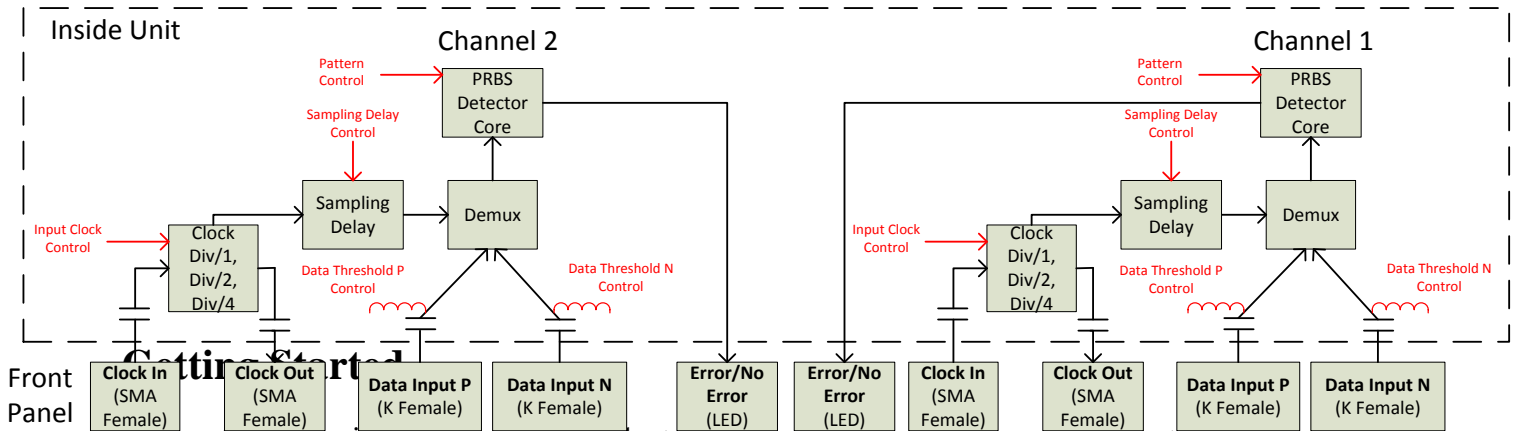
Connect the provided +5V AC/DC adapter to the unit. Power the unit on by turning the rocker switch on the back panel to the "ON" position. Observe a green light turn on next the +5V power jack and fan starts up. Next connect the provided USB cable to the computer and the unit. The USB connection on the back panel is a USB B jack. Observe a green light turn on next to the USB jack when the USB cable is connected to the computer and unit.

Note: the markings on the back panel for "USB" and "+5V DC 5A" have been swapped.

1.0 Software Installation

If software has already been installed go to **1.8**

1.1 Locate installation files given as shown in **Figure 1**. Double left-click on *setup.exe*

bin	4/8/2014 1:32 PM	File folder	
license	4/8/2014 1:32 PM	File folder	
supportfiles	4/8/2014 1:33 PM	File folder	
CDM v2.10.00 WHQL Certified.exe	4/8/2014 12:09 PM	Application	1,913 KB
dp.pmf	4/8/2014 1:33 PM	PMF File	1 KB
nidist.id	4/8/2014 1:33 PM	ID File	1 KB
setup.exe	10/7/2013 4:35 PM	Application	1,394 KB
setup.ini	4/8/2014 1:33 PM	Configuration sett...	5 KB

Figure 1. Setup Files

1.2 Select Target directory for location of installation files that will be installed. Then left-click on *Next*.

Figure 2. Installation Directory

1.3 Left-click on *Next*.

1.4 Wait for files to be installed.

1.5 Left-click on *Finish*

1.6 Left-click on *Restart* if requested.

1.7 Double left-click on the "CDM v2.10.00 WHQL Certified.exe" to install USB drivers. This file can be found in the same directory as the setup file used earlier to install software.

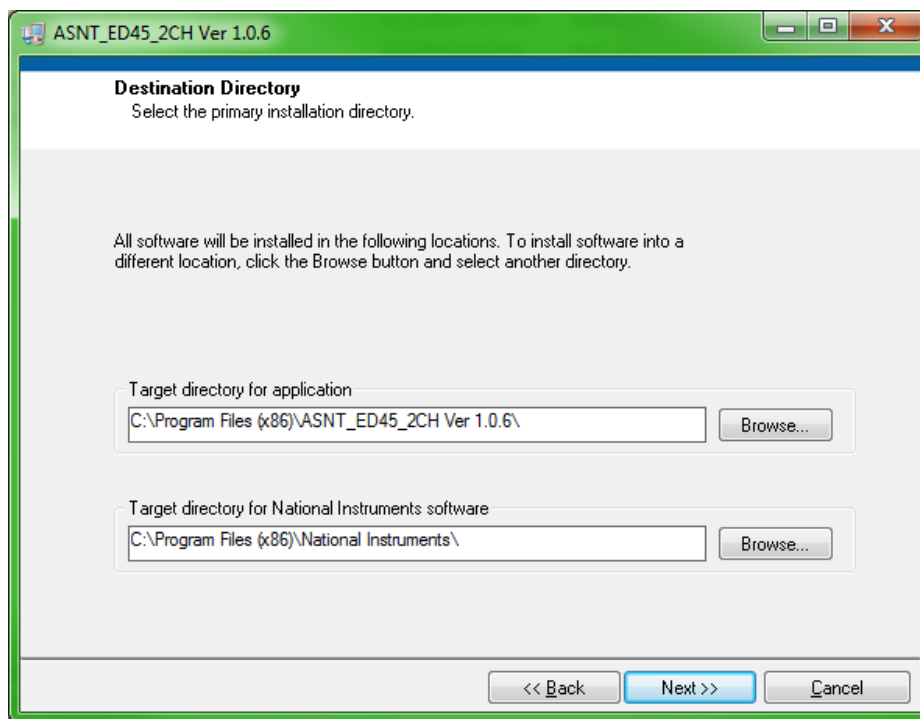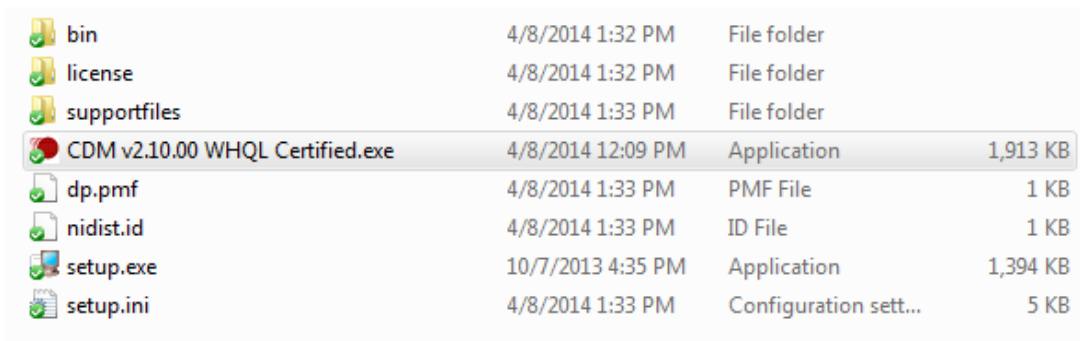|			
bin	4/8/2014 1:32 PM	File folder	
license	4/8/2014 1:32 PM	File folder	
supportfiles	4/8/2014 1:33 PM	File folder	
CDM v2.10.00 WHQL Certified.exe	4/8/2014 12:09 PM	Application	1,913 KB
dp.pmf	4/8/2014 1:33 PM	PMF File	1 KB
nidist.id	4/8/2014 1:33 PM	ID File	1 KB
setup.exe	10/7/2013 4:35 PM	Application	1,394 KB
setup.ini	4/8/2014 1:33 PM	Configuration sett...	5 KB

Figure 3. USB Driver

1.8 Double left-click on the icon *ASNT_ED45_2CH Vx.x.x* on the desktop to open the control software.

1.9 Referring to **Figure 4**, wait until the USB indicator has turned green. This indicates that the software is connected to the ASNT_ED45_2CH. If green indicator does not appear, then USB drivers may not be installed correctly or USB cable may need to be re-inserted.
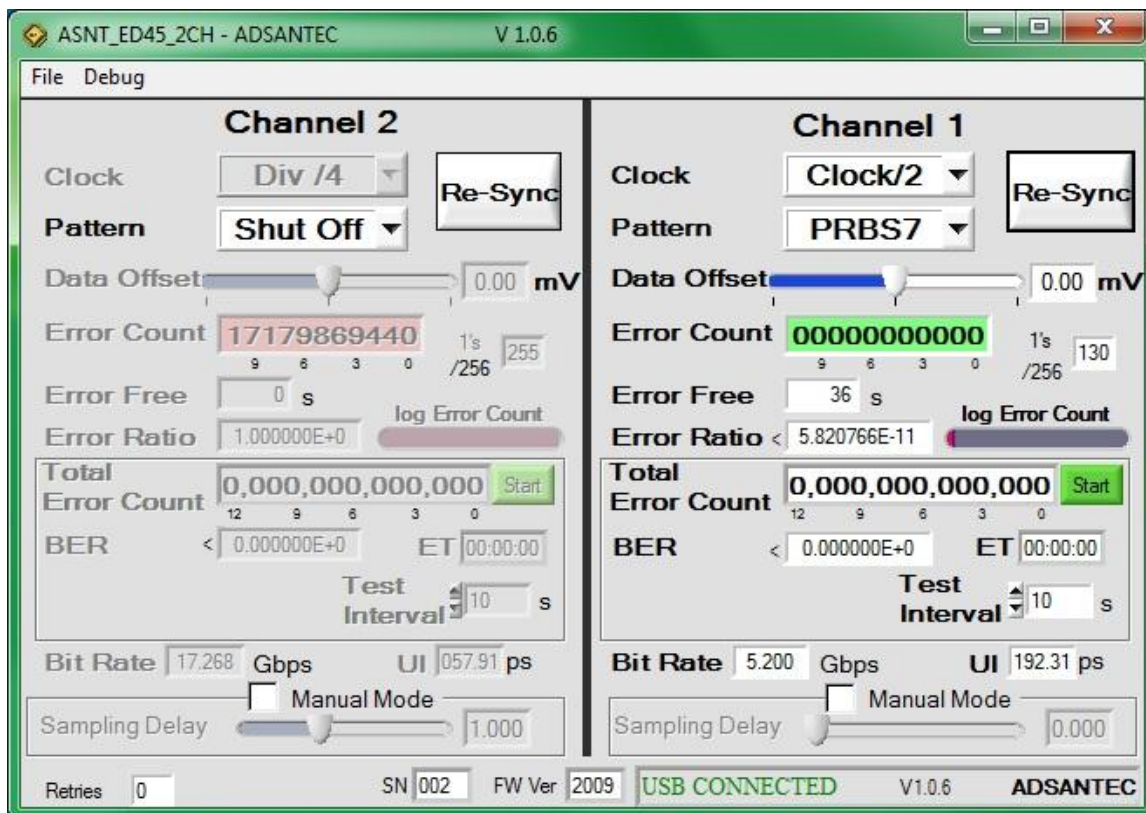
Figure 4. GUI – USB Connected

Front Panel Connections

Figure 5. Front Panel

Data Input (AC Coupled)

Apply a single-ended or differential PRBS7 to PRBS31 pattern to the Data Input channel on the front panel. All data inputs are AC coupled inside the unit and are k-type 2.92*mm* female connectors. External DC are not required and should not be used. Be careful when using SMA connections to data inputs as they may damage the data inputs. It is best to use k-type cables or use

k-type to SMA adapters. Apply at least a 200mV peak to peak signal single-ended for the unit to work properly, but do not apply a signal larger than 1V peak to peak as this will damage the unit. If applying single-ended data only, AC couple a 50Ohm termination to the other unused Data Input. There is a ~200mV common mode adjustment for each data input.

Clock In (AC Coupled)

Apply a half-rate clock to the Clock In female SMA connector. Example: 28$Gbps$ data input with a 14GHz clock is a half-rate clock. The Clock In is AC coupled inside the unit and needs at least 100mV peak to peak of amplitude but do not to exceed 1V peak to peak as this will damage the unit.

Clock Out (AC Coupled)

The Clock Out is an optional output that is not needed for the unit to operate normally. This Clock Out is a buffered clock from the Clock In. It provides an AC coupled output of typically 400mV and will be divided by one, two, or four from Clock In. If Clock input is selected on the GUI, then Clock Out will be divided by one. If Clock/2 input is selected on the GUI, then Clock Out will be divided by two. If Div/4 input is selected, then Clock Out will be divided by four. If Clock Out is unused, it is best to 50Ohm terminate the unused output.

LED

The front panel of the unit also provides feedback via two LED's for each channel. When the green LED is illuminated, the unit is detecting no errors currently in the data input. When the red LED is illuminated, the unit is currently detecting errors in the data input. Each channel has its own error/no error LED indicator.
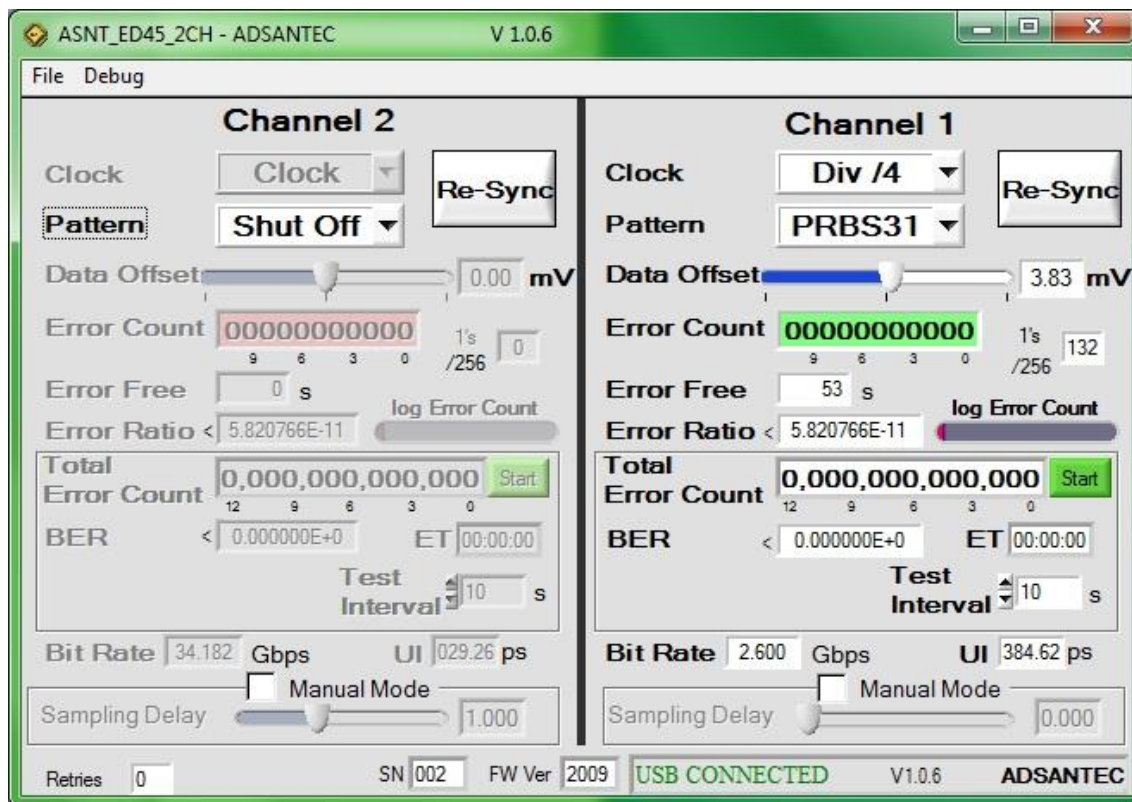
Operation

Figure 6. GUI

The GUI is has identical controls for each channel. Apply clock and data to the unit. Referring to **Figure 6**, select the appropraite Input Clock and Pattern. Select Input Clock to Clock for data rates below 26*Gbps*. For data rates above 26*Gbps*, select Clock/2. Addionally, Div/4 can be selected to lower the bitrate, which can be useful for checking every other bit or when working with high frequencies. Once input clock has been selected properly, check the Bit Rate box which should indicate the correct data input rate. When using "Clock/2" selection for Input Clock, Bit Rate box will display half the data rate. If not, then Input Clock is improperly selected or wrong clock frequency is being used. The UI box shows the unit interval (bit time) in *ps*.

Left-click on Re-Sync to automatically align clock vs. data. After a few seconds, the Error Count box will be green when there are no errors. Red or white when there are errors. The lower the datrate, the longer is takes for the error count to update. At data rates <5Gbps, it will take many seconds to update. If the unit is not counting errors, the Error Free box will start counting. As soon as any errors are found, the Error Free box will reset. The Error Ratio box will display the current error ratio.

The slider labeled Data Offset for adjusts the data input thresholds between data input P and N on each channel.

The box below Error Ratio provides a way to measure total error count, BER over a test interval time that can be set in seconds. The Error Ratio is only correct when the Input Clock is selected as half-rate. Once a time in seconds is put into the Test Interval box, left-clicking the Start button will begin the count. The box ET is the elapsed time in the format hours:minutes:seconds. To reset the timer, left-click the Stop button.

If the user wants to manually adjust clock vs. data input delay then first select the Manual Mode box. The Sampling Delay slider can then be manual adjusted.

Two channel data with one clock

When using only one clock as shown above, connect the clock input to channel 2. Connect channel 2's Clock Out to Channel 1 Clock In.

If using data rates above $26Gbps$, select Clock/2 clock for Channel 2's Input Clock and Clock for Channel 1's Input Clock selection in the GUI.

If using data rates below $26Gbps$, select Clock for Channel 2's Input Clock and Clock/2 for Channel 1's Input Clock selection in the GUI.

REVISION HISTORY

Revision	Date	Changes
1.3.2	07-2019	Updated Letterhead
1.3.1	09-2016	Updated Screenshots to reflect latest software Revision Added "Div/4" information about use of quarter-rate clock
1.2.1	07-2016	Updated GUI screen shots Removed clock duty cycle control
1.1.1	07-2016	Changes to GUI and modes of operation
1.0.1	04-2016	Preliminary Release