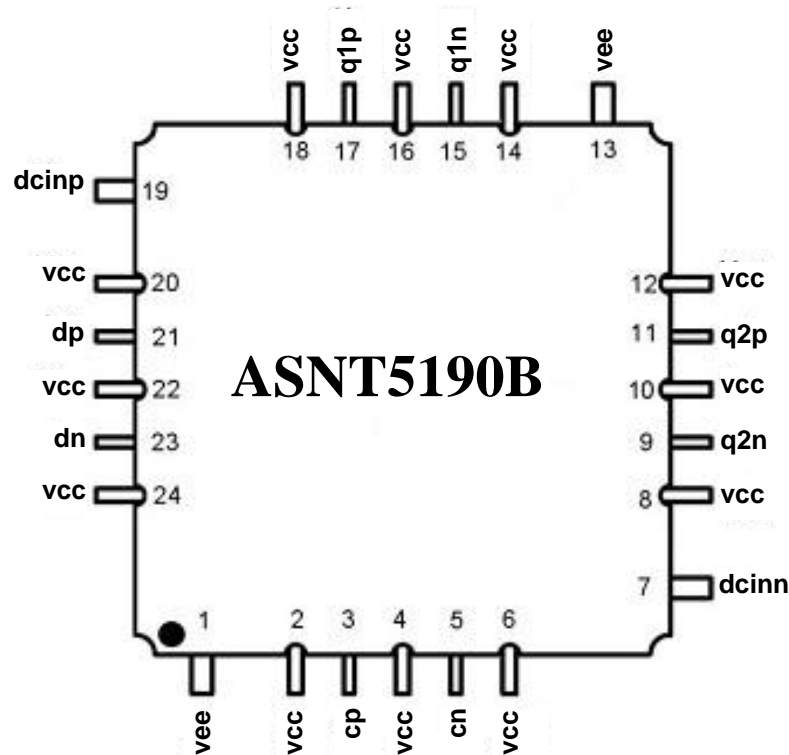




ASNT5190B-KMC DC-64Gbps Broadband Digital 1:2 Demultiplexer

- High speed broadband 1:2 Demultiplexer
- External control of internal clock's duty cycle
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Ideal for high speed proof-of-concept prototyping
- Fully differential CML input interfaces
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 600mW
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package





DESCRIPTION

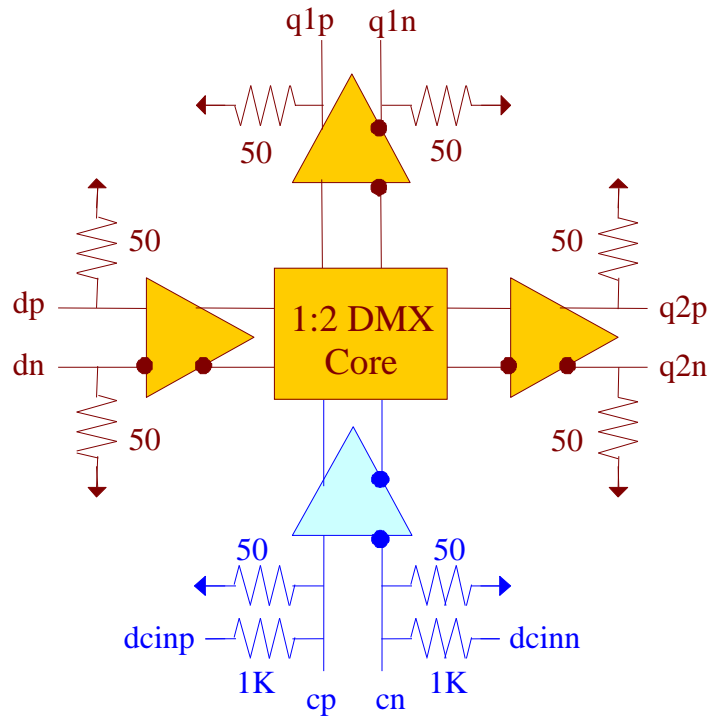


Fig. 1. Functional Block Diagram

The temperature stable ASNT5190B-KMC SiGe IC can be utilized as a high speed 1:2 demultiplexer, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can receive a high speed differential data input signal dp/dn and effectively demultiplex it into two high speed differential data output signals $q1p/q1n$ and $q2p/q2n$ by using a high speed differential clock input signal cp/cn . The duty cycle of the internal clock can be adjusted through ports $dcinp/dcinn$.

The part's I/O's support the CML logic interface with on chip 50Ω termination to VCC and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply ($VCC = 0.0V = \text{ground}$ and $VEE = -3.3V$), or a positive supply ($VCC = +3.3V$ and $VEE = 0.0V = \text{ground}$). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50Ω termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume $VCC = 0.0V$ and $VEE = -3.3V$.



ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.65	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
dp	21	CML input	Differential data input signals with internal 50Ohms termination to VCC
dn	23		
q1p	17	CML output	Differential data output signals with internal 50Ohms termination to VCC
q1n	15		
q2p	11	CML output	Differential data output signals with internal 50Ohms termination to VCC
q2n	9		
cp	3	CML input	Differential clock input signals with internal 50Ohms termination to VCC
cn	5		
Control Ports			
dcinp	19	Analog inputs	cp common mode control voltage
dcinn	7		cn common mode control voltage
Supply and Termination Voltages			
Name	Description	Pin Number	
vcc	Positive power supply (+3.3V or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24	
vee	Negative power supply (0V or -3.3V)	1, 13	



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
v _{ee}	-3.1	-3.3	-3.5	V	±6%
v _{cc}		0.0		V	External ground
I _{vee}		180		mA	
Power consumption		600		mW	
Junction temperature	-40	25	125	°C	
HS Input Data (dp/dn)					
Data rate	DC		64	Gbps	
Swing	0.05		1.0	V	Differential or SE, p-p
CM Voltage Level	v _{cc} -0.8		v _{cc}	V	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		32	GHz	
Swing	0.05		1.0	V	Differential or SE, p-p
CM Voltage Level	v _{cc} -0.8		v _{cc}	V	Must match for both inputs
Duty cycle	45	50	55	%	
HS Output Data (q1p/q1n, q2p/q2n)					
Data rate	DC		32	Gbps	
Logic "1" level		v _{cc}		V	
Logic "0" level		v _{cc} -0.4		V	With external 50Ω DC termination
Rise/Fall times	6	8	10	ps	20%-80%
Output Jitter			1	ps	Peak-to-peak
Common Mode Control Ports (dcin/dcinn)					
Input signal range	-3.3		0	V	

PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package's leads will be trimmed to a length of 1.0mm. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
 - 3.9.1 Solderability
 - 3.2.2 Solder Purity Maintenance
 - 3.9.2 Solderability Maintenance
 - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder



The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5190B-KMC. The first 9 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.



ADSANTEC

Ultra High-Speed Mixed Signal ASICs

*Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505*

*Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com*

REVISION HISTORY

Revision	Date	Changes
1.0.2	10-2024	Updated Package Information
0.1.2	05-2020	Updated Package Information
0.0.2	07-2019	Updated Letterhead
0.0.1	09-2014	Preliminary release