ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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Offices: 310-530-9400 / Fax: 310-530-9402
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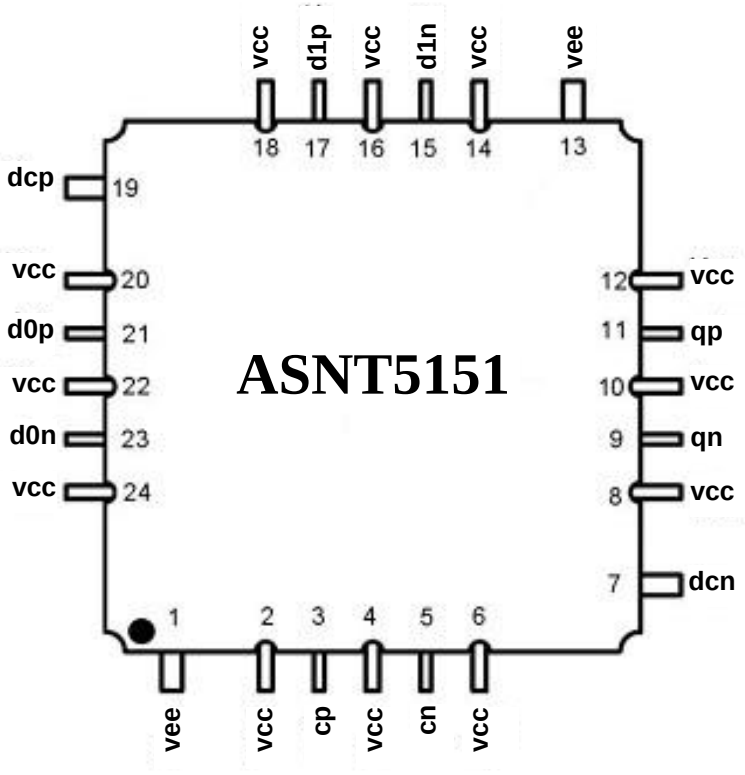
ASNT5151-KMC
DC-64*Gbps* Broadband Digital 2:1 Multiplexer/Selector

- High speed broadband 2:1 Multiplexer/Selector (MUX)
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Ideal for use as a high isolation selector switch or as a high speed 2-to-1 serializer
- Ideal for high speed proof-of-concept prototyping
- Fully differential CML input interface
- Fully differential CML output interface with 600*mV* single-ended swing
- Analog input clock common mode voltage control
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 415*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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DESCRIPTION

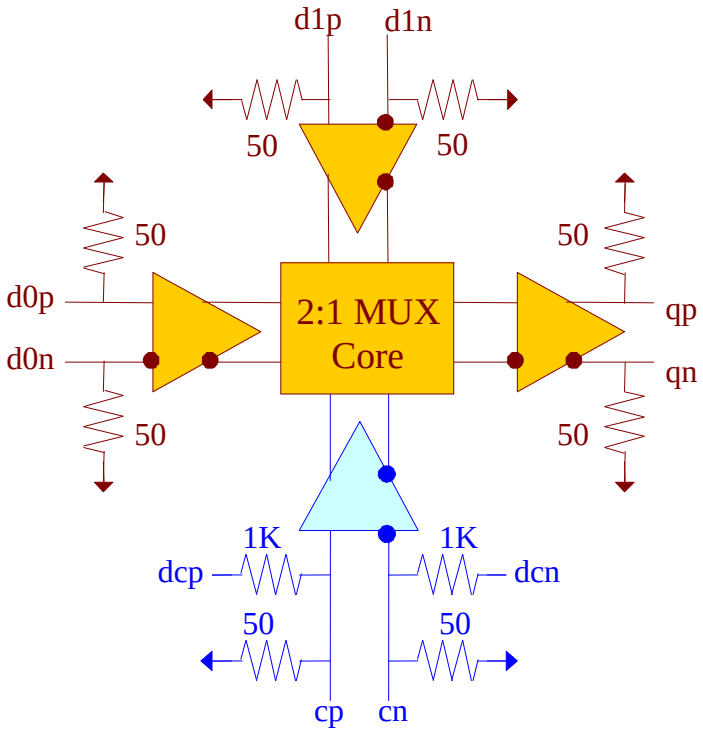

Fig. 1. Functional Block Diagram

The temperature stable and broadband ASNT5151-KMC SiGe IC can be utilized as either a high isolation selector switch or a high speed 2:1 serializer and is intended for use in high-speed measurement / test equipment. When employed as a selector switch, the IC can route one of its differential data input signals d0p/d0n or d1p/d1n to its differential output qp/qn while effectively blocking the other data input. Selection of a specific data input is achieved through appropriate external DC biasing of the selector signal inputs cp/cn. The logic is shown in Table 1.

Table 1. Truth Table

c	d0	d1	out
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

As a 2:1 serializer, the IC can receive high speed input data signals into d0p/d0n and d1p/d1n and effectively multiplex them into a double frequency rate NRZ output data signal by using a high speed input clock signal on its selector signal inputs cp/cn. The signals should be aligned as shown in Fig. 2. To ensure both maximum timing margins and low output signal jitter, limit the amount of jitter on the input signals (D0, D1, and C) to only a few picoseconds.

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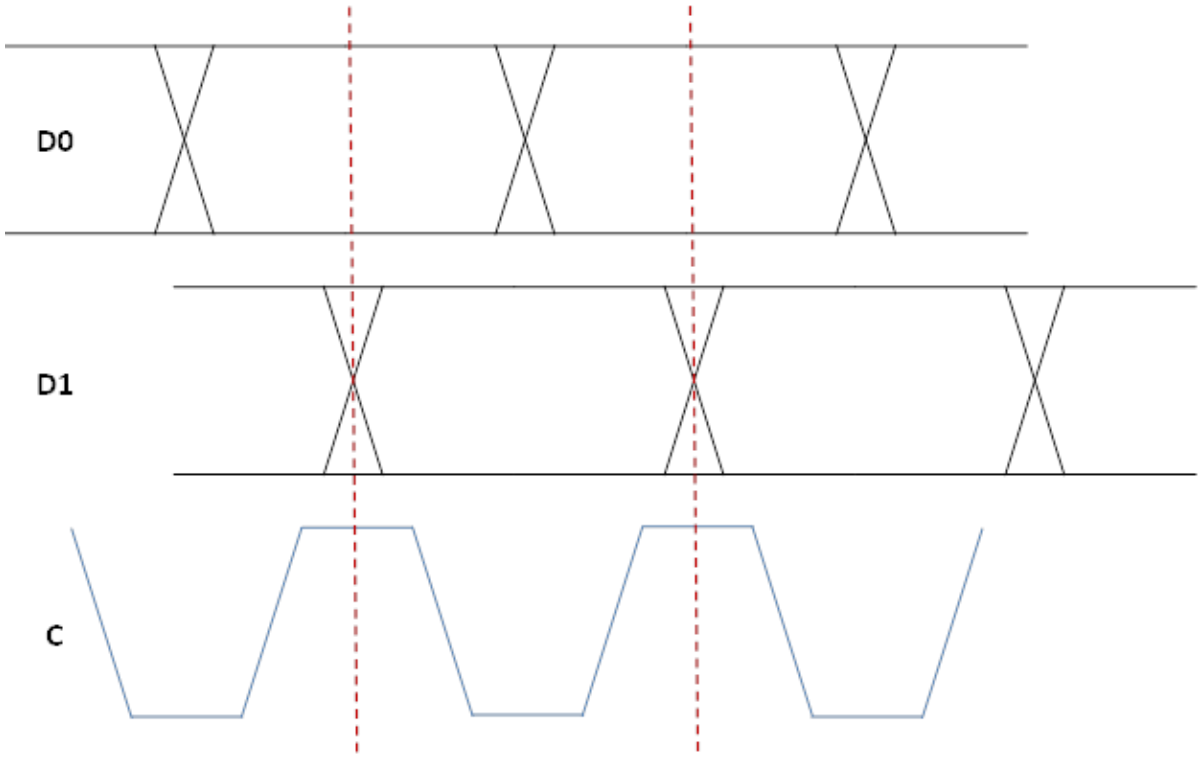

Fig. 2. Input Signal Timing Diagram

The common-mode voltage levels of the input clock signals can be adjusted using the analog control inputs dcp/dcn.

The part's I/O's support the CML logic interface with on chip 50*Ohms* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All max voltage limits are referenced to ground.

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Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.45	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
d0p	21	CML input	Differential data input signals with internal SE 50*Ohms* termination to vcc
d0n	23		
d1p	17	CML input	Differential data input signals with internal SE 50*Ohms* termination to vcc
d1n	15		
cp	3	CML input	Differential clock input signals with internal SE 50*Ohms* termination to vcc
cn	5		
dcp	19	Analog inputs	cp common mode control voltage
dcn	7		cn common mode control voltage
qp	11	CML output	Differential data output signals with internal SE 50*Ohms* termination to vcc. Also require external SE 50*Ohms* termination to vcc
qn	9		
Supply and Termination Voltages			
Name	**Description**		**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)		1, 13

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		125		*mA*	
Power consumption		415		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (d0p/d0n, d1p/d1n)					
Data rate	DC		50	*Gbps*	When used as a selector
Frequency	DC		25	*GHz*	When used as a selector
Data rate	DC		32	*Gbps*	When used as a multiplexer
Swing	50		800	*mV*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		32	*GHz*	
Swing	50		800	*mV*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty cycle	45	50	55	*%*	
HS Output Data (qp/qn)					
Data rate	DC		50	*Gbps*	When used as a selector
Frequency	DC		25	*GHz*	When used as a selector
Data rate	DC		64	*Gbps*	When used as a multiplexer
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.6		*V*	With external 50*Ohms* DC termination
Rise/Fall times	5	7	9	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak
Common Mode Control Ports (dcp/dcn)					
Input Signal Range	-3.3		0.0	*V*	

PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFP package shown in Fig. 3. The package’s leads will be trimmed to a length of 1.0*mm*. After trimming, the package’s leads will be further processed as follows:

1. The lead’s gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

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The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5151-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

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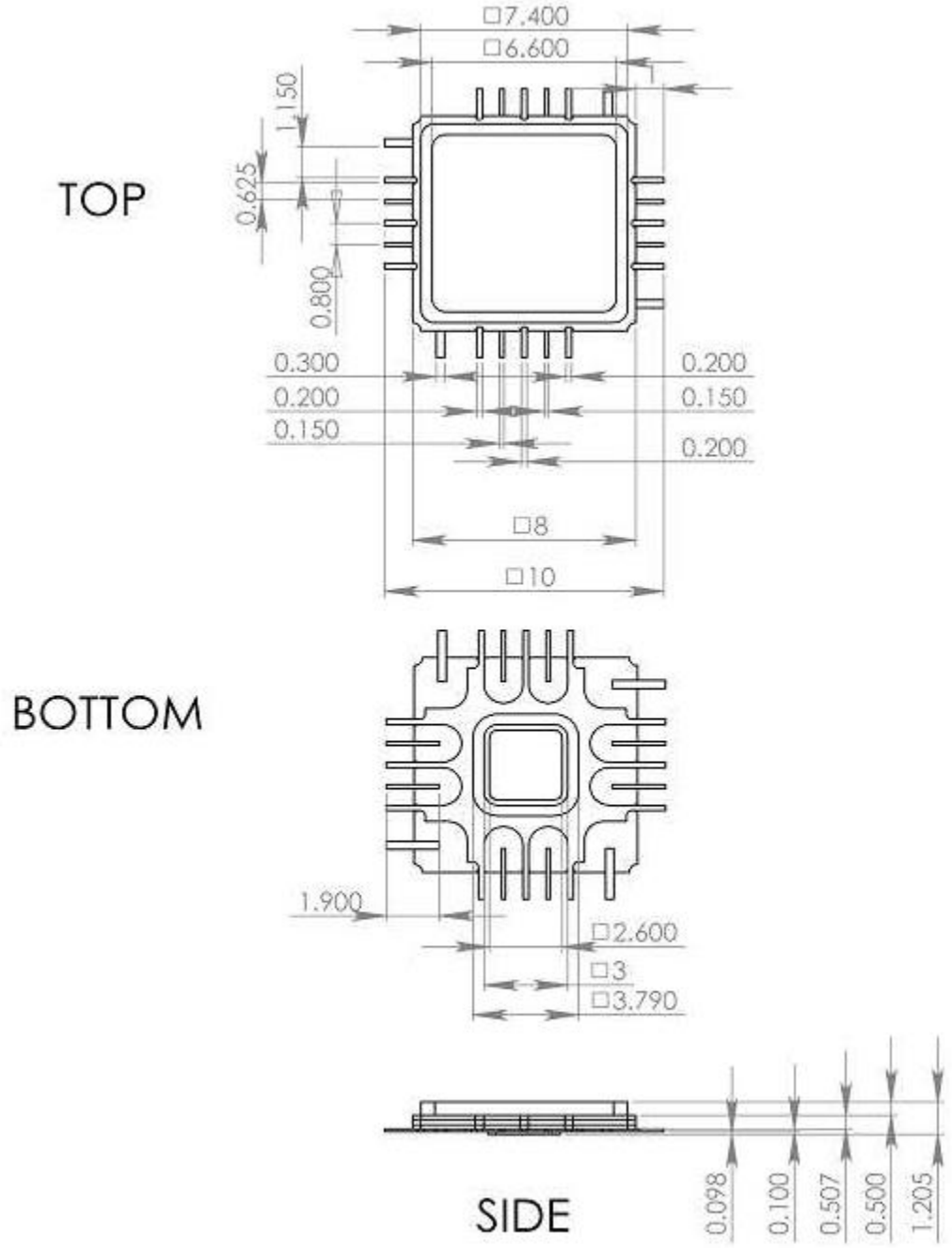

Fig. 3. CQFP 24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.5.2	10-2024	Updated Package Information
1.4.2	05-2020	Updated Package Information
1.3.2	07-2019	Updated Letterhead
1.3.1	02-2019	Added truth table Revised package information section
1.2.1	04-2014	Added Required Input Signal Alignment section
1.1.1	11-2013	Included CM level shifting knobs on the clock input pins Revised characteristics and pin diagram Revised functional block diagram and description Revised terminal functions Revised electrical characteristics
1.0.1	11-2013	First release