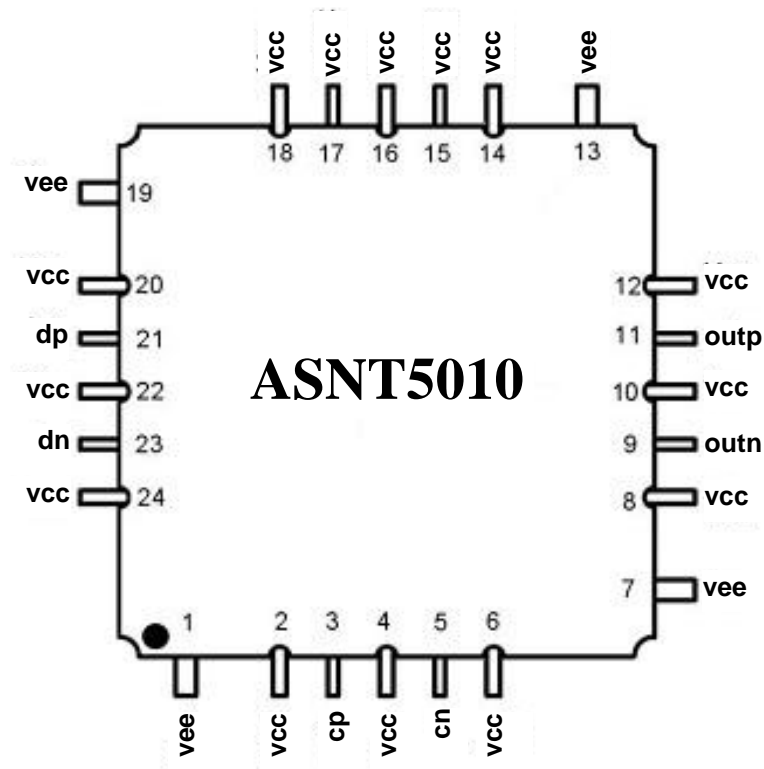




## ASNT5010-KMC DC-32Gbps D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 6.5ps set-up/hold time capability
- 87% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 415mW
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



## DESCRIPTION

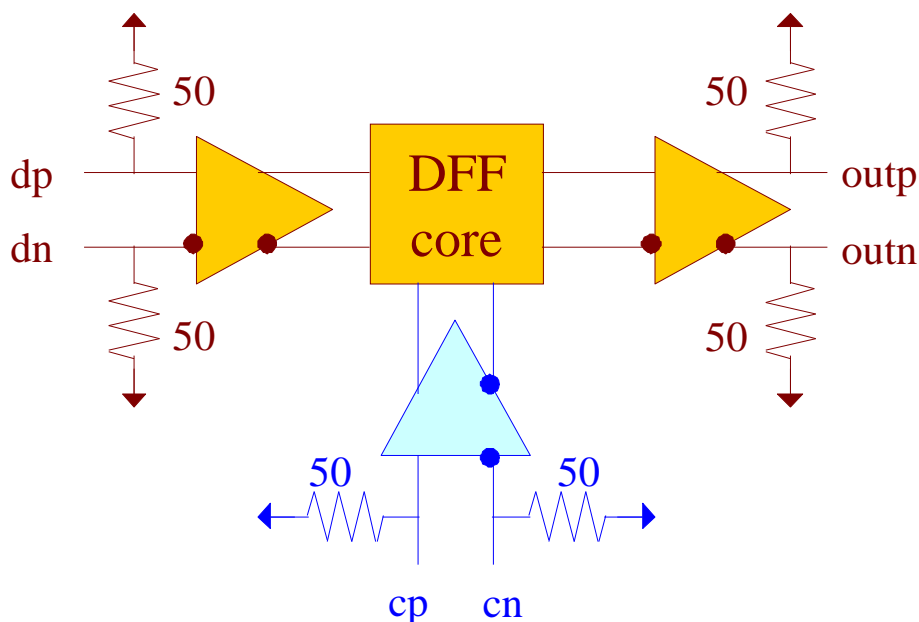


Fig. 1. Functional Block Diagram

The temperature stable ASNT5010-KMC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample a high-speed data signal **dp/dn** with a full-rate external clock **cp/cn** to create a full-rate retimed NRZ data output **outp/outn**. Sampling occurs on the falling clock edge.

The part's I/O's support the CML logic interface with on chip 50 $\Omega$  termination to **vcc** and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

## POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (**vcc** = 0.0V = ground and **vee** = -3.3V), or positive supply (**vcc** = +3.3V and **vee** = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50 $\Omega$  termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume **vcc** = 0.0V and **vee** = -3.3V.**



## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.46	W
RF Input Voltage Swing (SE)		1.2	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
dp	21	CML input	Differential data inputs with internal SE 50 <i>Ohms</i> termination to vcc
dn	23		
cp	3	CML input	Differential clock inputs with internal SE 50 <i>Ohms</i> termination to vcc
cp	5		
outp	11	CML output	Differential data outputs with internal SE 50 <i>Ohms</i> termination to vcc. Require external SE 50 <i>Ohms</i> termination to vcc
outn	9		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24
vee	Negative power supply (0V or -3.3V)		1, 7, 13, 19



## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I <sub>vee</sub>		125		mA	
Power consumption		415		mW	
Junction temperature	-40	25	125	°C	
<b>HS Input Data (dp/dn)</b>					
Data rate	DC		32	Gbps	
Voltage swing, pk-pk	0.05		1.0	V	Single ended, unused input not connected or AC terminated
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
Setup/Hold time		6.5		ps	Relative to negative clock edge
<b>HS Input Clock (cp/cn)</b>					
Frequency	DC		32	GHz	
Voltage swing, pk-pk	0.05		1.0	V	Single ended, unused input not connected or AC terminated
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
Rise/fall time			500	ps	For reliable data latching
Clock Phase Margin	85	87	89	%	
<b>HS Output Data (outp/outn)</b>					
Data rate	DC		32	Gbps	
Latency		67		ps	From Clock input to Data output
Logic "1" level		vcc		V	
Logic "0" level		vcc-0.4		V	With external 50Ohms DC termination
Clock-to-output delay	55	65	75	ps	
Rise/Fall times		13		ps	20%-80%
Output Jitter		4		ps	Peak-to-peak
<b>Receiver Sensitivity (Voltage Swing)</b>					
Differential	25		400	mV	Pk-to-pk for each P and N input
Differential	50		800	mV	Pk-to-pk between P and N inputs
Single Ended	50			mV	P or N input signal around common-mode voltage level on the other input

<b>Simulated Timing, ps</b>									
Parameter	Slow Process Corner			Nominal Process Corner			Fast Process Corner		
	-25C	125C	Δ	-25C	125C	Δ	-25C	125C	Δ
Propagation Delay	78.3	93.8	15.5	75.4	89.7	14.3	74.1	88.1	14.0
Set Up Time	4.1	3.1	1.0	3.2	2.3	0.9	2.4	1.8	0.6
Hold Time	-6.0	-4.8	1.2	-5.2	-4.2	1.0	-4.7	-3.8	0.9



## PACKAGE INFORMATION

The die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

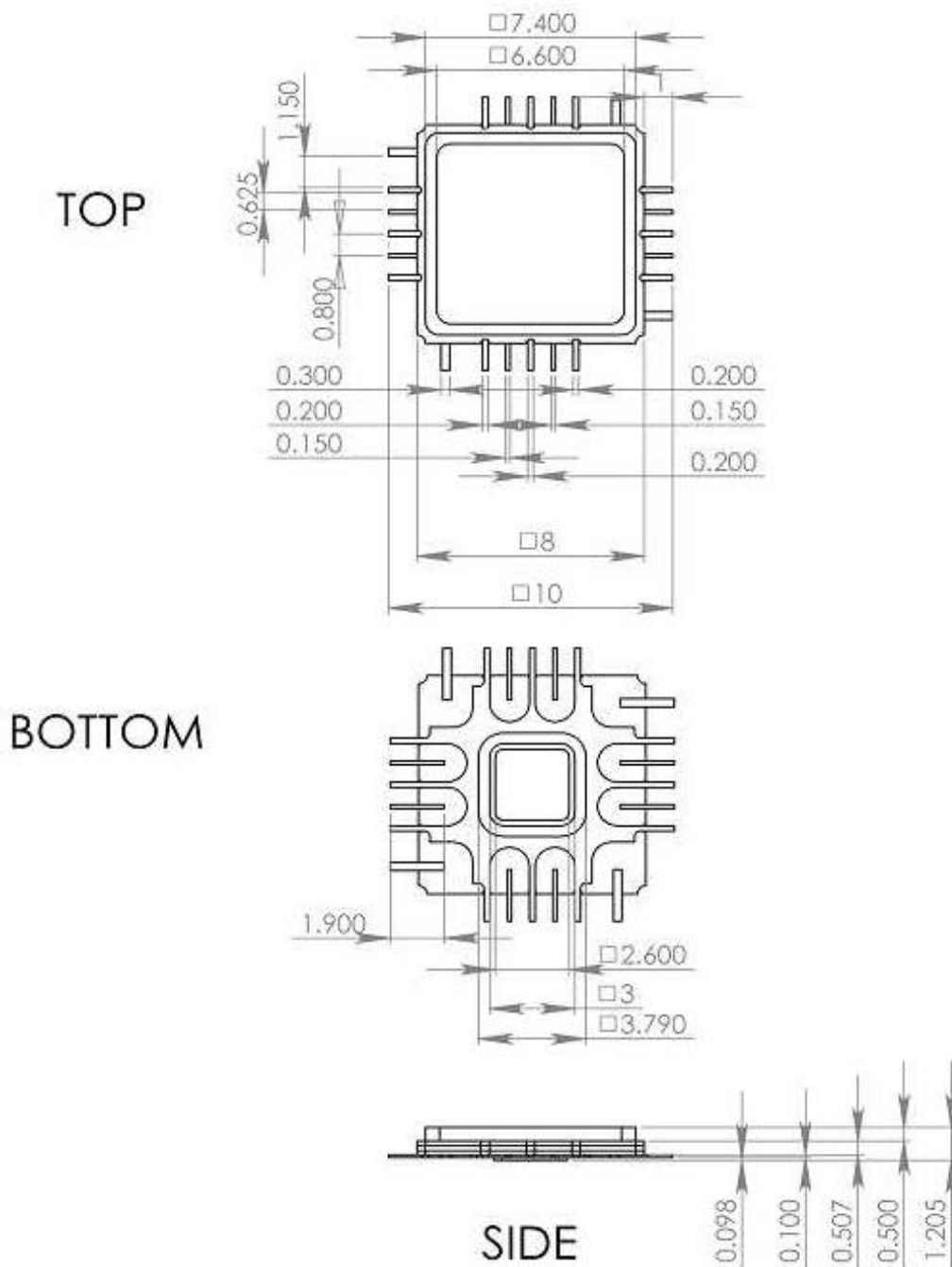


Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)



The part's identification label is ASNT5010-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

## REVISION HISTORY

Revision	Date	Changes
2.9.2	02-2025	Corrected maximum input swings Added input clock rise/fall time specification
2.8.2	11-2024	Specified sampling edge of clock, added timing simulation data, corrected input swing description
2.7.2	02-2020	Updated Package Information
2.6.2	07-2019	Updated Letterhead
2.6.1	02-2019	Added setup/hold time to Electrical Characteristics table
2.5.1	08-2018	Corrected latency specifications
2.4.1	08-2018	Added latency specifications
2.3.1	06-2018	Updated electrical characteristics
2.2.1	06-2018	Updated electrical characteristics Updated package information
2.1.1	02-2013	Revised title Revised package information
2.0.1	01-2013	Revised title Added package pin out drawing Revised functional block diagram Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Added package information and mechanical drawing Format correction
1.0	02-2008	First release