ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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ASNT2032-MBL
Digital DMUX 12-to-24 with LVDS Interfaces

- Digital demultiplexer (DMUX) 12-to-24 with LVDS output interface
- Programmable LVDS/CML/ECL input interface
- Supports data rates from 1.0*Mbps* to 3.6*Gbps*
- Preset function for synchronization of multiple parallel devices
- Two pairs of clock divided-by-2 and synchronous clock enable outputs for supporting a tree-type demultiplexation structure
- Selectable clock divided-by-4 or divided-by-2 output
- Power supply of +3.3*V*
- Industrial temperature range
- Low power consumption of 924*mW* at 3.6*Gbps*
- Available in custom 256-pin BGA package (13*mm* x 13*mm* x 2.5*mm*)

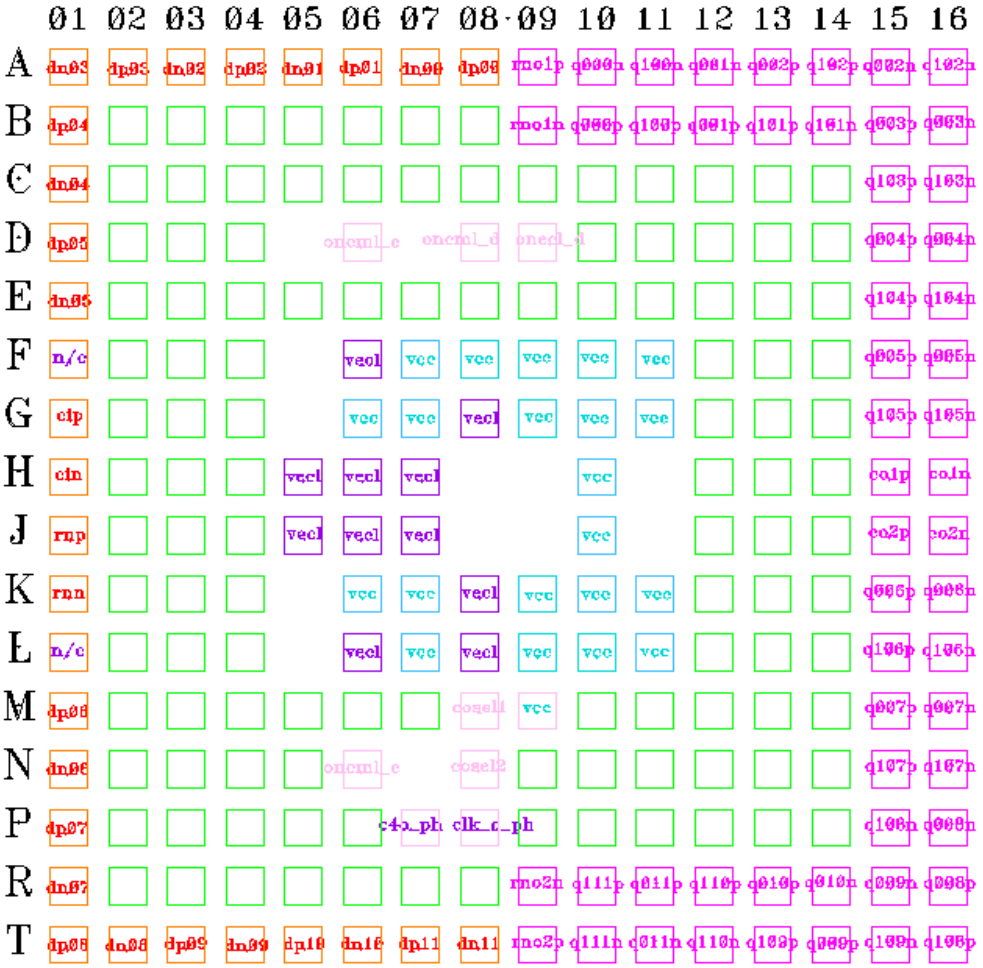

Fig. 1. BGA Ball Placement, view from the Top of Package

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DESCRIPTION

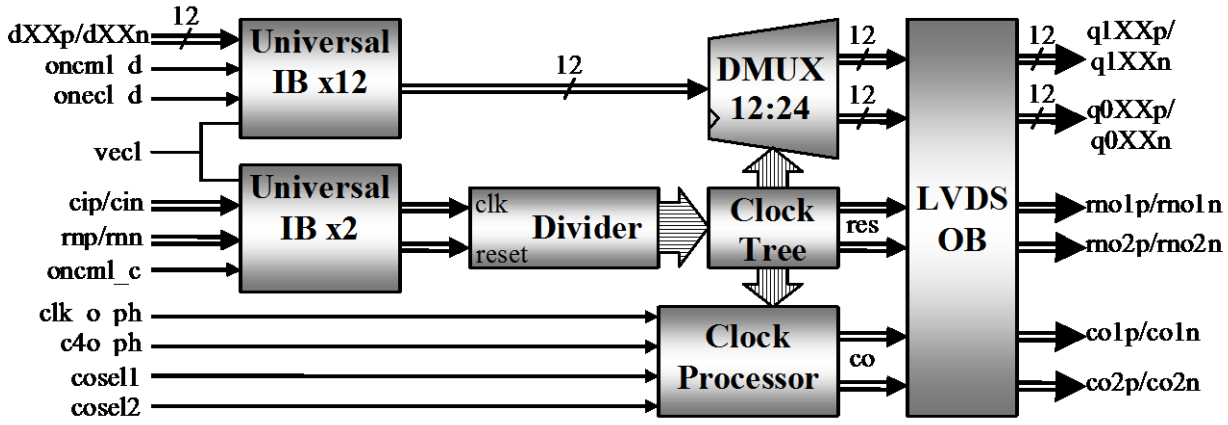

Fig. 2. Functional Block Diagram

ASNT2032-MBL is a broadband multichannel digital deserializer/demultiplexer (DMUX) 12-to-24 with an external initial preset function, selectable LVDS, CML or ECL input interface, and LVDS output interface. The part shown in Fig. 2 also features selectable clock divided-by-2 or clock divided-by-4 outputs with multiple phases. The latter is intended for DDR interface support.

The operational speed of the DMUX is defined by an external clock signal (cip/cin) that is converted into the required timing signals by its internal divider. The divider can be preset to a certain initial state by an external active-low reset signal (rnp/rnn), which allows synchronization of multiple DMUX devices operating in parallel. The reset signal is retimed inside the chip by the external clock and its positive edge must satisfy the timing shown in Fig. 3. The position of the reset signal's negative edge is not important.

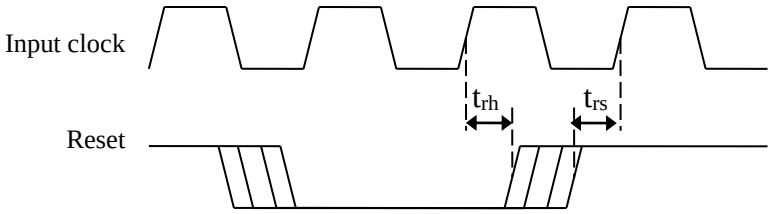

Fig. 3. Reset Timing Diagram.

The optimal alignment of input data (dXXp/dXXn) and clock (cip/cin) is illustrated in Fig. 4.

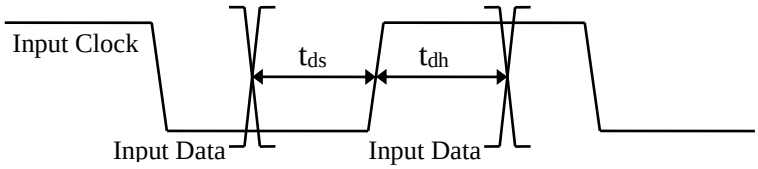

Fig. 4. Input Timing Diagram

The actual values of setup (t_{rs} and t_{ds}) and hold (t_{rh} and t_{dh}) times are presented in ELECTRICAL CHARACTERISTICS.

This part also supports cascaded tree-type structures as shown in Fig. 5, by supplying two synchronous copies of clock divided-by-2 (co1p/co1n and co2p/co2n) and clock enable (rno1p/rno1n and rno2p/rno2n) signals.

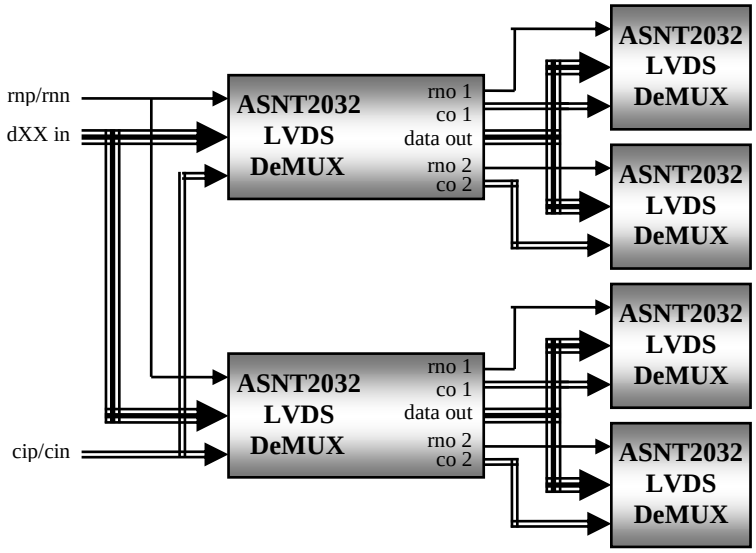

Fig. 5. Cascaded Tree-Type Structure

A clock divided-by-4 output signal can also be provided for higher flexibility instead of a clock divided-by-2. The type of output clock co1p/co1n and co2p/co2n can be controlled by the cosel1 and cosel2 signal values shown in Table 1.

Table 1. Clock divided-by-2 and clock divided-by-4 selection

cosel1 or cosel2 value	Clock output co1 or co2, respectively
"0" (default)	Clk/2
"1"	Clk/4

All chip outputs are phase aligned with each other, with the capability to select the output clock phase relative to the output data. They are also stabilized over PVT variations. The selection is performed by applying the c4o_ph and clk_o_ph signals. The default values of those signals are defined by on-chip terminations to vee and are equal to "0". Possible phase relations of the outputs are shown in Table 2.

The DMUX IC uses one positive power supply vcc = +3.3*V* and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

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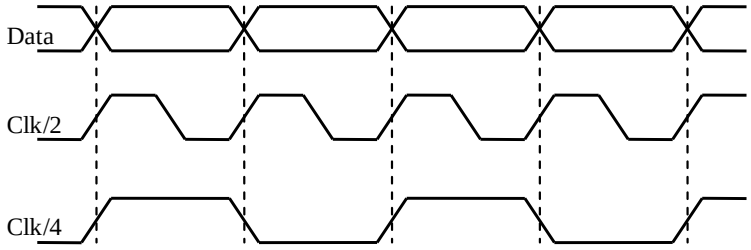
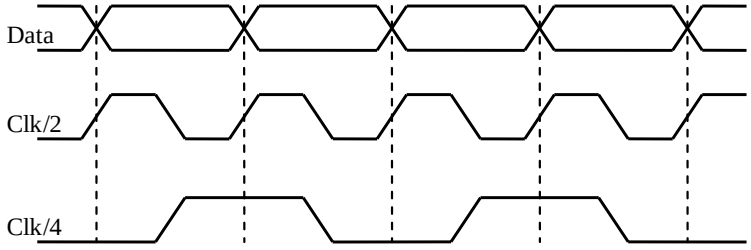
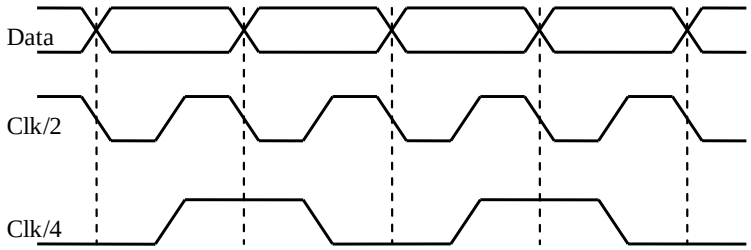
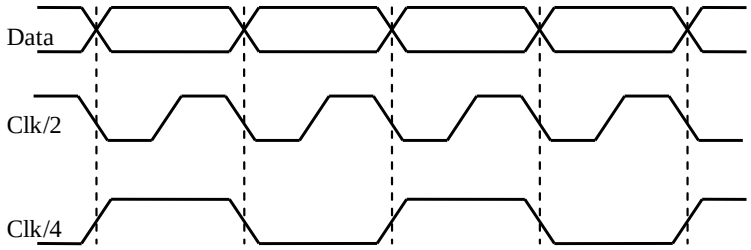
Table 2. Output clock phase selection

<table>
<tr><th>clk_o_ph</th><th>c4o_ph</th><th></th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>Clk/2 rising edges and Clk/4 edges are syncronous with data transition.
 
</td></tr>
<tr><td>1</td><td>Only Clk/4 edges are shifted from data transition (half data period).
 
</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>Clk/2 rising edges and Clk/4 edges are shifted from data transition (half data period).
 
</td></tr>
<tr><td>1</td><td>Only Clk/2 edges are shifted from data transition (half data period).
 
</td></tr>
</table>

LVDS/ECL/CML Input Buffers

The data input buffer may operate with LVDS, ECL or CML interfaces. The clock and divider reset input buffers may only be used as CML or LVDS. To select the desired interface, refer to Table 3.

Table 3. Input interface selection

on_ecl (for data input only)	on_cml	Interface
"0" (default)	"0" (default)	LVDS
"1"	"0"	ECL
"0"	"1"	CML
"1"	"1"	Not Allowed

When the ECL mode is selected, the vecl voltage must be set to 2*V* below vcc and should support both sourcing and sinking of the current.

Possible application schemes for different interfaces are detailed in Table 4, where *V*cm is the common-mode voltage of the applied signal.

Table 4. Input Application Schemes

Interface type	**Input type**	**direct (p) signal**			**inverted (n) signal**		
		Swing, *mV*	**Connection**	***V*cm, *V***	**Swing, *mV***	**Connection**	***V*cm, *V***
LVDS	Diff.	$\Delta V^{*)}$	DC	1.2±1.0	$\Delta V^{*)}$	DC	1.2±1.0
	SE	$\Delta V^{*)}$	AC	-	Threshold	DC	1.2±1.0
		Threshold	DC	1.2±1.0	$\Delta V^{*)}$	AC	-
CML or ECL	Diff.	$\Delta V^{*)}$	DC	vcc-Swing/2	$\Delta V^{*)}$	DC	vcc-Swing/2
			AC	-		AC	-
	SE	$\Delta V^{*)}$	AC	-	-	Not connected	-
		$\Delta V^{*)}$	AC	-	Threshold	DC	vcc
		-	N/C	-	$\Delta V^{*)}$	AC	-
		Threshold	DC	vcc	$\Delta V^{*)}$	AC	-

*) – ΔV is defined in ELECTRICAL CHARACTERISTICS as Swing (SE).

DeMUX 12:24

The block consists of 12 independent 1-to-2 demultiplexers with a standard M-S/M-S-S architecture. It latches in the data signals on both edges of half-rate clock c/2 that is supplied by the internal divider and delivers the deserialized outputs aligned to the corresponding clock edges. The output data signals are marked with "1" and "2" and are both aligned to the positive edge of the output clock divided-by-2.

Divider-by-4

The divider-by-4 converts the input clock signal (cip/cin) into clock divided-by-2 (c/2) and clock divided-by-4 (c/4) signals internally aligned to the positive edge of the input clock. The divider can be preset to the 0 initial state by the external active-low reset signal rnp/rnn that is internally retimed by the positive edge of the input clock. The timing diagram is presented in Fig. 3 above.

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LVDS Output Buffers

The LVDS output buffers are designed in full compliance with the LVDS standard and operate from a 3.3*V* supply at frequencies up to 3*GHz*. The buffer requires external 100*Ohm* differential DC termination.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 5 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 5. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.6	*V*
Power Consumption		1.1	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

The ball assignment for the BGA package is shown in Table 6 and Table 7.

Table 6. Package Signal Balls

Name	Code	Type	Description
High-Speed Inputs			
dp00	A8	LVDS, CML, or ECL	Differential data inputs
dn00	A7		
dp01	A6		
dn01	A5		
dp02	A4		
dn02	A3		
dp03	A2		
dn03	A1		
dp04	B1		
dn04	C1		
dp05	D1		
dn05	E1		
dp06	M1		
dn06	N1		
dp07	P1		
dn07	R1		
dp08	T1		
dn08	T2		
dp09	T3		
dn09	T4		
dp10	T5		
dn10	T6		
dp11	T7		
dn11	T8		
rnp	J1	LVDS or CML	Differential divider reset input
rnn	K1		
cip	G1	LVDS or CML	Differential clock input
cin	H1		
High-Speed Outputs			
rno1p	A9	LVDS	Differential divider reset outputs
rno1n	B9		
rno2p	T9		
rno2n	R9		
co1p	H15	LVDS	Differential clock outputs
co1n	H16		
co2p	J15		
co2n	J16		

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Name	Code	Type	Description
q0p<00>	B10	LVDS	Differential data outputs
q0n<00>	A10		
q1p<00>	B11		
q1n<00>	A11		
q0p<01>	B12		
q0n<01>	A12		
q1p<01>	B13		
q1n<01>	B14		
q0p<02>	A13		
q0n<02>	A15		
q1p<02>	A14		
q1n<02>	A16		
q0p<03>	B15		
q0n<03>	B16		
q1p<03>	C15		
q1n<03>	C16		
q0p<04>	D15		
q0n<04>	D16		
q1p<04>	E15		
q1n<04>	E16		
q0p<05>	F15		
q0n<05>	F16		
q1p<05>	G15		
q1n<05>	G16		
q0p<06>	K15		
q0n<06>	K16		
q1p<06>	L15		
q1n<06>	L16		
q0p<07>	M15		
q0n<07>	M16		
q1p<07>	N15		
q1n<07>	N16		
q0p<08>	R16		
q0n<08>	P16		
q1p<08>	T16		
q1n<08>	P15		
q0p<09>	T14		
q0n<09>	R15		
q1p<09>	T13		
q1n<09>	T15		
q0p<10>	R13		
q0n<10>	R14		

Name	Code	Type	Description
q1p<10>	R12	LVDS	Differential data outputs
q1n<10>	T12		
q0p<11>	R11		
q0n<11>	T11		
q1p<11>	R10		
q1n<11>	T10		
Low-Speed Control Signals			
cosel1	M8	3.3*V* CMOS DC	Binary control signals with a default value of "0"
cosel2	N8		
clk_o_ph	P8		
c4o_ph	P7		
oncml_c	D6, N6		
onecl_d	D9		
oncml_d	D8		

Table 7. Package Power Supply Balls

Name	Code	Type	Value, *V*
vee	B2-B8, C2-C14, D2-D4, D10-D14, E2-E14, F2-F4, F12-F14, G2-G4, G12-G14, H2-H4, H12-H14, J2-J4, J12-J14, K2-K4, K12-K14, L2-L4, L12-L14, M2-M7, M10-M14, N2-N5, N9-N14, P2-P6, P9-P14, R2-R8	Ground	0
vcc	F7-F11, G6, G7, G9-G11, H10, J10, K6, K7, K9-K11, L7, L9-L11, M9	Positive supply voltage	3.3
vecl	F6, G8, H5, H6, H7, J5, J6, J7, K8, L6, L8	ECL input termination voltage	vcc-2*V*
n/c	F1, L1	Not connected	
X	D5, D7, F5, G5, H8, H9, H11, J8, J9, J11, K5, L5, N7	Removed balls	

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.14	+3.3	+3.47	*V*	±5%
vee		0.0		*V*	External ground
*I*vcc		280		*mA*	
Power consumption		924		*mW*	
Junction temperature	-25	50	125	*°C*	
Input Data (dXXp/dXXn)					
Data Rate	1		3600	*Mbps*	
Swing (SE)	50		600	*mV*	Peak-to-peak
CM Voltage Level	1		3.3	*V*	In LVDS mode
Interface	LVDS, ECL, CML				Complies with IEEE Std
Input Clock (cip/cin)					
Frequency	1		3600	*MHz*	
Swing (SE)	50		600	*mV*	Peak-to-peak
CM Voltage Level	1		3.3	*V*	In LVDS mode
Interface	LVDS, CML				Complies with IEEE Std
Output Data (q0XX, q1XX)					
Data Rate	0.5		1800	*Mbps*	
Swing (SE)	250	325	400	*mV*	Peak-to-peak
CM Voltage Level	1.125	1.2	1.275	*V*	
Interface	LVDS				Complies with IEEE Std
Divided Output Clock (co1p/co1n, co2p/co2n)					
Frequency	0.5/0.25		1800/900	*MHz*	
Swing (SE)	250	325	400	*mV*	Peak-to-peak
CM Voltage Level	1.125	1.2	1.275	*V*	
Interface	LVDS				Complies with IEEE Std
CMOS Control Inputs					
Internal termination		600		*KOhm*	Terminated to vee
Logic “1” level	vcc-0.3			*V*	
Logic “0” level			vee+0.3	*V*	
Timing Parameters					
Data skew		0		*ps*	By simulations
Clock skew		0		*ps*	
t_{ds}		-90		*ps*	
t_{dh}		200		*ps*	
t_{rs}		25		*ps*	
t_{rh}		25		*ps*	

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PACKAGE INFORMATION

The chip is packaged in a custom 256-pin BGA package shown in Fig**.** 6.

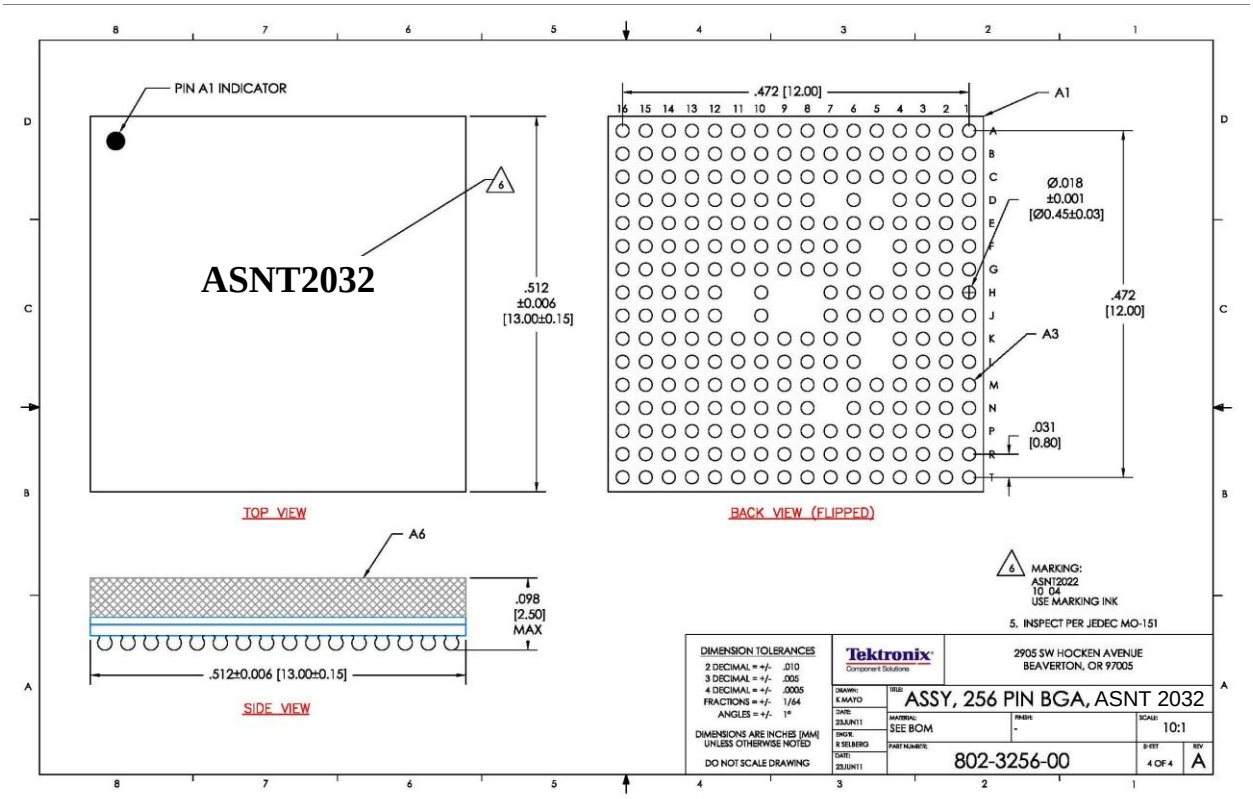

Fig. 6. BGA Package Drawing (All Dimensions in mm)

The part's identification label is ASNT2032-MBL. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
1.9.2	05-2020	Updated Package Information
1.8.2	07-2019	Updated Letterhead
1.8.1	01-2015	Added Table 4 (Input Application Schemes)
1.7.1	01-2015	Corrected ball numbers for co1p and co1n signals
1.6.1	07-2014	Corrected maximum frequency
1.5.1	04-2014	Added specifications for CMOS control signals Added description of default control states
1.4.1	08-2013	Added reset timing in Description and in Electrical Characteristics
1.3.1	01-2013	Corrected format Corrected block diagram Added Absolute Maximums Rating table Corrected Package Information section
1.2	01-2012	Revised Electrical Characteristics
1.1	08-2011	Revised Electrical Characteristics
1.0	06-2011	First release