ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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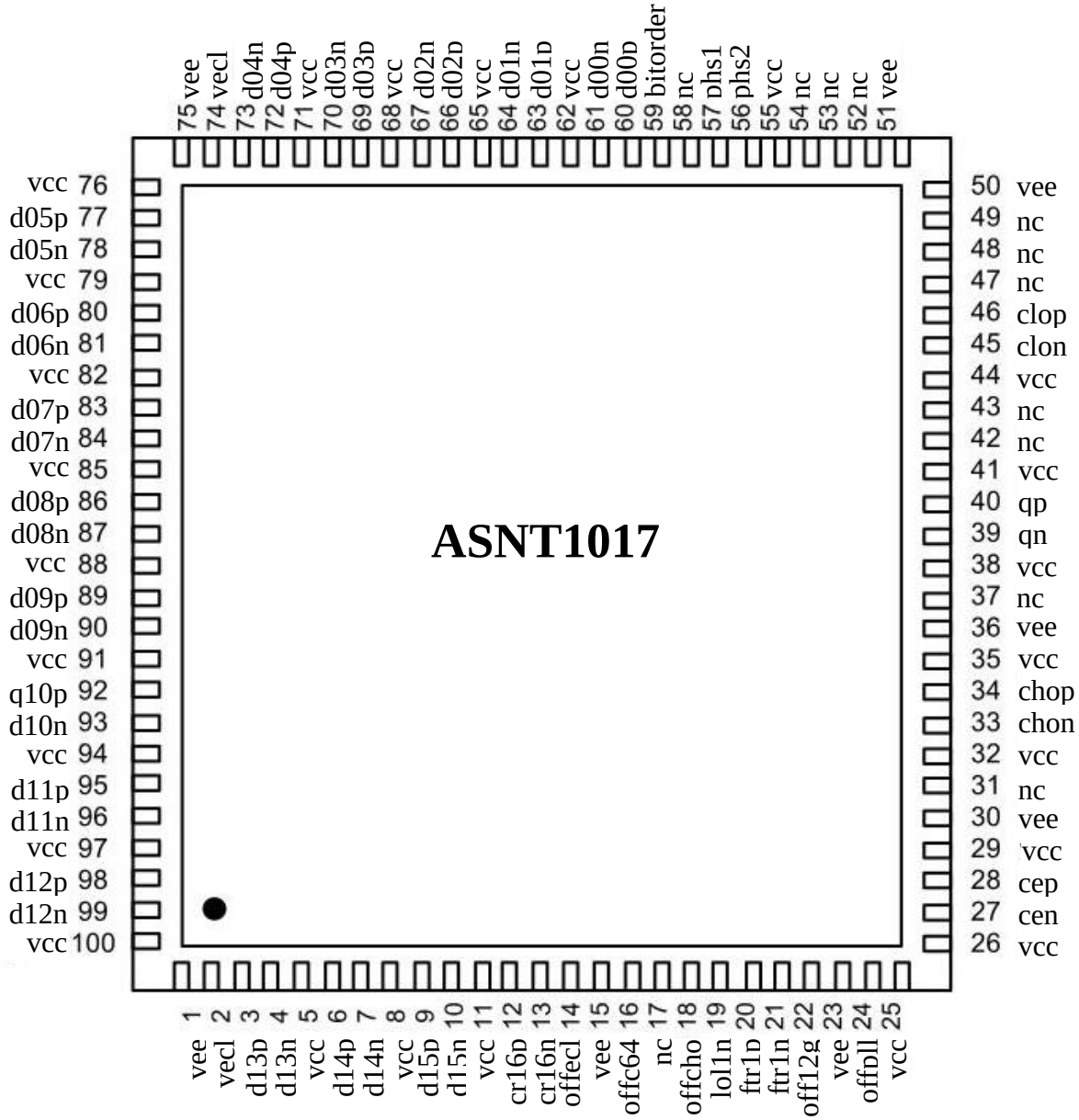
ASNT1017-PQA
DC-to-17*Gbps* Programmable Multiplexer 16:1 / Serializer

- Programmable serializer 16-to-1 with CMU or digital operational modes
- Supports data rates from 12.0*Gb/s* to 14.3*Gb/s* in CMU mode and DC to 17*Gb/s* in digital mode
- LVDS compliant input data buffers
- Selectable full-speed or divided-by-2 clock output
- LVDS output clock-divided-by-16 with a selectable phase
- Single +3.3*V* power supply
- Industrial temperature range
- Low power consumption of 500*mW* at maximum speed
- Standard 100-pin QFN package (12*mm* x 12*mm*)



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DESCRIPTION

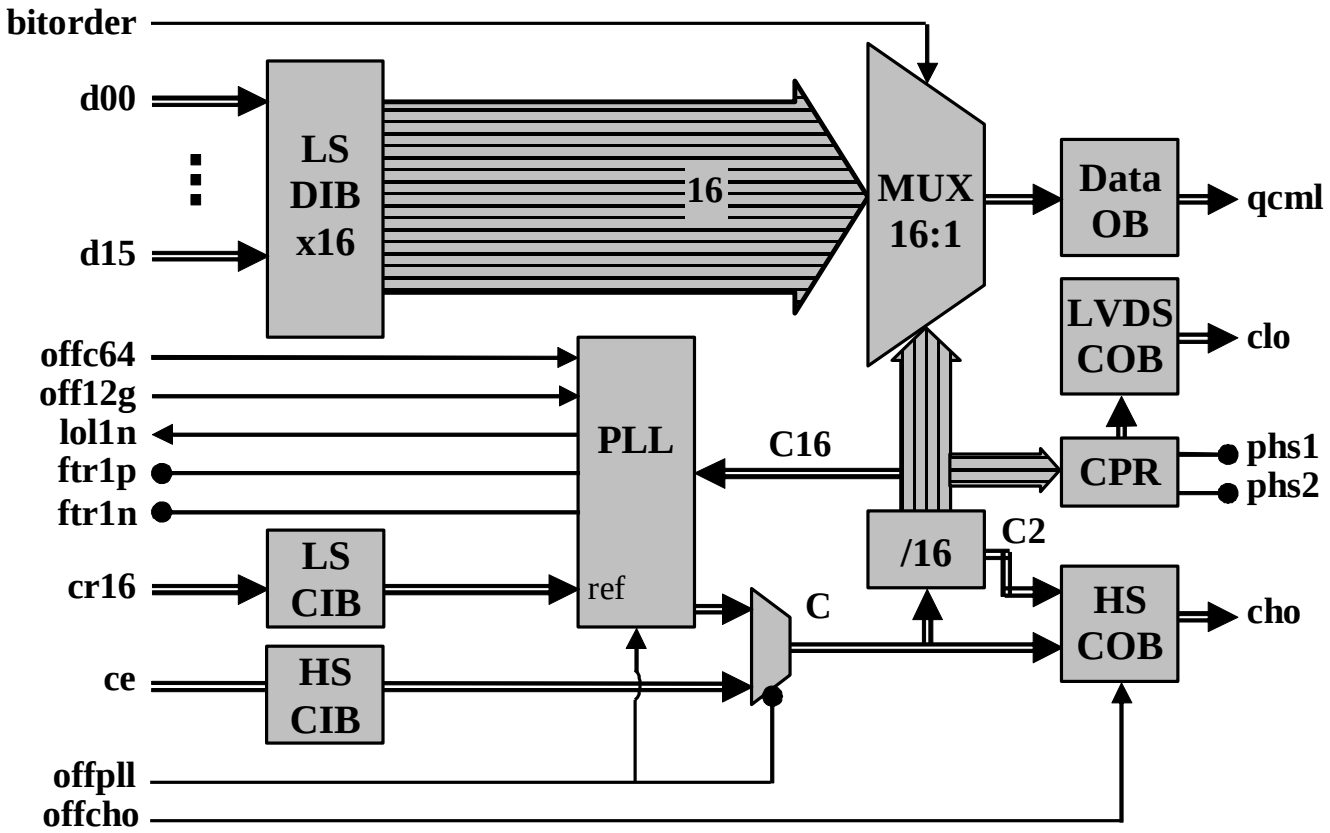

Fig. 1. Functional Block Diagram

ASNT1017-PQA is a low power and high-speed 16-to-1 programmable multiplexer (MUX) with an internal clock multiplier unit (CMU) that can also operate in digital mode using an external high-speed clock. The main function of the chip shown in Fig. 1 is to multiplex 16 parallel data channels running at a bit rate of $f_{bit}/16$ into a high-speed serial bit stream running at f_{bit}. It provides a high-speed output data channel for point-to-point data transmission over a 50*Ohm* controlled impedance media. The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

During normal operation, the serializer's low-speed input buffer LS DIBx16 accepts external 16-bit wide parallel data words d00-d15 through 16 differential LVDS inputs and delivers them to the multiplexer's core MUX16:1 for serialization. By utilizing the pin bitorder, the serializer can designate either d00 or d15 as the MSB (first output serial bit), thus simplifying the interface between the multiplexer and a digital data processor.

MUX16:1 utilizes multiple divided down clock signals that are generated from the full rate clock C by the internal divider /16. The divider also produces the half rate clock C2 for the high speed clock output buffer HS COB and the divided-by-16 clock signal C16 for use by the phase-locked loop PLL.

In PLL mode, the clock signal C is synthesized by the PLL which locks the internal signal C16 to the external system-level clock cr16 delivered through the low speed clock input buffer LS CIB. The cr16 frequency may be selected as either 1/16 or 1/64 of the frequency of the activated VCO (voltage-controlled oscillator) in the PLL. The PLL contains 2 full rate VCOs to cover the required frequency range. One of the VCOs can be

selected utilizing the off12g control pin. The PLL also generates a loss-of-lock alarm signal lol1n. In digital mode, the PLL is disabled and the external signal ce delivered through the high-speed clock input buffer HS CIB is used as clock signal C.

The serialized words generated by MUX16:1 are transmitted as binary signals qcml by the differential CML output buffer Data OB. The selectable full-rate or half-rate clock cho is transmitted by a similar CML buffer (HS COB) in parallel with the high-speed data. The clock and data outputs are well phase-matched to each other resulting in a very little relative skew over the operating temperature range of the device. HS COB may be disabled or its operational mode changed by means of the 3-state (vee, vcc, not connected) CMOS signal offcho. Both output stages are back terminated with on-chip 50*Ohm* resistors.

The chip also provides a differential low speed output clock clo though an LVDS clock output buffer (LVDS COB). The 0º, 90º, 180º, or 270º phase of the clock signal can be selected using control pins phs1 and phs2 as shown in Table 2.

The serializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

LS DIBx16

The Low-Speed Data Input Buffer (LS DIB) is a proprietary universal input buffer (UIB) that can run at a frequency up to 1.0*GHz*. The input termination impedance is controlled by 3.3*V* CMOS signal offecl and is set to 100*Ohm* differential if offecl="1" (true LVDS mode, default state) or 50*Ohm* single-ended to vecl if offecl="0" (CML mode). The value of vecl should be equal to vcc in CML mode or vcc-2*V* in PECL mode. In this case, the corresponding termination voltage source should be able to both sink and source up to 20*mA* of current. Possible input clock application schemes are detailed in Table 1, where *V*cm is the common-mode voltage of the clock signal.

Table 1. LS Input Clock Application Schemes

Interface type	Clock type	cep signal			cen signal		
		Swing, *mV*	**Connection**	***V*cm, *V***	**Swing, *mV***	**Connection**	***V*cm, *V***
LVDS (offecl ="1")	Diff.	70-to-500	DC	1.2±1.0	70-to-500	DC	1.2±1.0
	SE	140-to-900	AC	-	Threshold	DC	vee-to-vcc
		Threshold	DC	vee-to-vcc	140-to-900	AC	-
CML or PECL (offecl ="0")	Diff.	70-to-500	DC	vcc-Swing/2	70-to-500	DC	vcc-Swing/2
			AC	-		AC	-
	SE	140-to-900	AC	-	-	Not connected	-
		140-to-900	AC	-	Threshold	DC	vcc
		-	Not connected	-	140-to-900	AC	-
		Threshold	DC	vcc	140-to-900	AC	-

As can be seen, UIB is designed to accept differential signals with amplitudes above 60*mV* peak-to-peak (p-p), DC common mode voltage variation between negative (vee) and positive (vcc) supply rails, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes above 60*mV*p-p and threshold voltages between vee and vcc. UIB fully complies with LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

LS CIB

The Low-Speed Clock Input Buffer (LS CIB) is the same UIB described above. This block is used to deliver the low speed system clock cr16 as a reference signal to the PLL.

PLL

The Phase Locked Loop (PLL) contains a phase frequency detector, charge pump, an on-chip integrator with an additional off-chip filter connected between the pins ftr1p and ftr1n (Fig. 2), and two selectable LC-tank VCOs centered at 14*GHz* and 12.5*GHz*. The main function of the PLL is to synthesize the full rate clock C by aligning the phase and frequency of the C16 signal to the externally applied system clock cr16. The required frequency of cr16 is defined by the 3.3*V* CMOS control signal offc64 and should be either 1/16 (offc64="1") or 1/64 (offc64="0") of the activated VCO's frequency. The active-low 3.3*V* CMOS loss-of-lock lol1n alarm signal is generated by the PLL if its two input clock signals are not matching in phase and/or frequency.

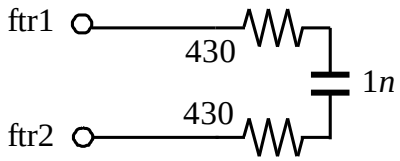

Fig. 2. External Filter Schematic

Selection of different VCOs of the PLL is achieved by utilizing the 3.3*V* CMOS control pin off12g. The logic "1" chooses the high-speed VCO, while the logic "0" (default state) selects the low-speed VCO. At any state, the unused VCO is turned completely off in order to save power.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can accept high-speed clock signals at its differential CML input port cep/cen. It can also accept a single-ended signal with a threshold voltage applied to the unused pin. HS CIB can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended 50*Ohm* termination to vcc for each input line.

/16

The Divider-by-16 (/16) includes four divide-by-2 circuits connected in series. The high-speed clock C is fed into the first divide-by-2 circuit that generates the half-rate clock C2. C2 is then routed internally to the next divide-by-2 circuit and outside of the block to MUX16:1. Other divided down clock signals are formed and routed to MUX16:1 in a similar fashion. C16 is passed on to LVDS COB to become the output low speed clock signal clo.

MUX16:1

The 16-to-1 Multiplexer (MUX16:1) utilizes a tree-type architecture which latches the incoming data on the negative edge of the C16 clock signal supplied by /16. The 16-bit wide data word is subsequently multiplexed and delivered to Data OB as a single serial data stream. The latency of this circuit block is equal to roughly one period of C16. The output bit order is controlled by the 3.3*V* CMOS signal bitorder. The first output serial bit (MSB) corresponds to d00 when bitorder="0" (default), or to d15 when bitorder="1".

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Data OB

The Data Output Buffer (Data OB) receives high-speed serial data from MUX16:1 and converts it into differential CML output signal qcmlp/qcmln. The buffer utilizes internal 50*Ohm* loads to vcc and requires the matching of 50*Ohm* external termination resistors connected between vcc and each output.

HS COB

The High Speed Clock Output Buffer (HS COB) utilizes the same termination scheme as Data OB and can operate at maximum frequency while producing a full single-ended CML output swing. The buffer can be enabled or disabled by the external 3-state (”1"=vcc, “0”=vee, “n/c”=not connected) 3.3*V* CMOS control signal offcho. The “n/c” default state corresponds to the C2 output signal, the logic “0” state provides a full-rate clock output signal, while the logic “1” state disables the buffer completely.

CLK Proc

By utilizing the 3.3*V* CMOS control pins phs1 and phs2, the phase of clo can be altered in accordance with Table 2.

Table 2. Output Clock Phase Selection

phs1	phs2	C16 phase
vee (default)	vee (default)	270°
vee	vcc	180°
vcc	vee	90°
vcc	vcc	0°

LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives the divided clock C16 and converts it into LVDS output signal clo. The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2.0*GHz* with a nominal output current of 3.5*mA*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 standards.

Output Timing

The phase relation between the output data qp/qn and the full rate output clock cho is specified in Table 3 and illustrated by Fig. 3.

Table 3. Output Data-to-Clock Phase Delay

Junction temperature, °C	τ,*ps*	
	Min.	Max.
-25	77	80
50	82	86
125	87	91

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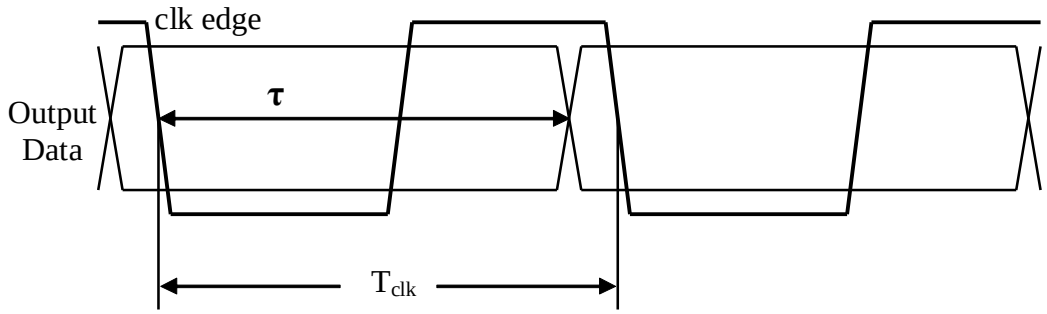

Fig. 3. Output Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 4 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.6	*V*
Power Consumption		0.72	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	5, 8, 11, 25, 26, 29, 32, 35, 38, 41, 44, 55, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100
vee	Negative power supply (GND or 0*V*)	1, 15, 23, 30, 36, 50, 51, 75
vecl	Input termination voltage (vcc for CML, vcc-2*V* for ECL)	2, 74
nc	**Keep not connected!**	17, 31, 37, 42, 43, 47, 48, 49, 52, 53, 54, 58

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cep	28	Input	CML differential external clock inputs with internal SE 50*Ohm* termination to vcc
cen	27		
chop	34	Output	CML differential clock outputs. Require external SE 50*Ohm* termination to vcc. Can be disabled by offcho
chon	33		
qp	40	Output	CML differential data outputs. Require external SE 50*Ohm* termination to vcc
qn	39		
Controls			
lol1n	19	LS Out, CMOS	PLL lock indicator (high: locked; low: no lock)
ftr1p	20	I/O	PLL external filter connections (see Fig. 2)
ftr1n	21		
offecl	14	LS In., CMOS	LS input termination selector (active: low, CML or PECL depending on vecl connection; default: high, LVDS)
offc64	16	LS In., CMOS	Input reference clock rate selection (active: low, divided-by-64; default: high, divided-by-16)
offcho	18	LS In., CMOS	3-state HS COB control (high: buffer is disabled; n/c: half-rate output clock; low: full-rate output clock)
off12g	22	LS In., 3-state	VCO frequency selection (active: high, high-speed VCO; default: low, low-speed VCO)
offpll	24	LS In., CMOS	PLL activation signal (active: high, PLL is off; default: low, PLL is on)
phs1	57	LS In., CMOS	Low-speed output clock phase selection (see Table 2)
phs2	56		
bitorder	59	LS In., CMOS	Input bit order selection (active: high, d15 is serialized first; default: low, d00 is serialized first)

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TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
Low-Speed I/Os			
cr16p	12	Input	LVDS clock inputs
cr16n	13		
clop	46	Output	LVDS clock outputs
clon	45		
d00p	60	Input	LVDS data inputs
d00n	61		
d01p	63		
d01n	64		
d02p	66		
d02n	67		
d03p	69		
d03n	70		
d04p	72		
d04n	73		
d05p	77		
d05n	78		
d06p	80		
d06n	81		
d07p	83		
d07n	84		
d08p	86		
d08n	87		
d09p	89		
d09n	90		
d10p	92		
d10n	93		
d11p	95		
d11n	96		
d12p	98		
d12n	99		
d13p	3		
d13n	4		
d14p	6		
d14n	7		
d15p	9		
d15n	10		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.14	+3.3	+3.47	*V*	±5%
vee		0.0		*V*	External ground
*I*vcc		150		*mA*	
Power consumption		500		*mW*	
Junction temperature	-25	50	125	*°C*	
LS Input Data (d00p/d00n-d15p/d15n)					
Data Rate	0.0	937.5	1063	*Mbps*	
Differential Swing	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	vee		vcc	*V*	
LS Input Reference Clock (cr16p/cr16n)					
Frequency	747		831	*MHz*	12.5*GHz* VCO is active
	807		893	*MHz*	14*GHz* VCO is active
Differential Swing	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	vee		vcc	*V*	
VCO Frequency Range					
Frequency	12.0		13.3	*GHz*	12.5*GHz* VCO is active
Frequency	12.9		14.3	*GHz*	14*GHz* VCO is active
HS Input Clock (cep/cen)					
Frequency	0.0	15	17	*GHz*	
Swing (Diff or SE)	0.2		1.2	*V*	Peak-to-peak
CM Voltage Level	vcc-0.8		vcc	*V*	
Duty Cycle	40	50	60	*%*	
HS Output Data (qcmlp/qcmln)					
Data Rate	0.0	15	17	*Gbps*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.6		*V*	
Jitter		12		*ps*	Peak-to-peak @12.5*Gb/s*
HS Output Clock (chop/chon)					
Frequency	0.0	15	17	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.6		*V*	
Jitter		5		*ps*	Peak-to-peak @12.5*GHz*
Duty Cycle		50		*%*	
LS Output Clock (clop/clon)					
Frequency	0.0	937.5	1063	*MHz*	
Interface		LVDS			Meets the IEEE Std.
CMOS Control Inputs (3-state input has an additional N/C state)					
Logic “1” level	vcc-0.4			*V*	
Logic “0” level			vee+0.4	*V*	

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PACKAGE INFORMATION

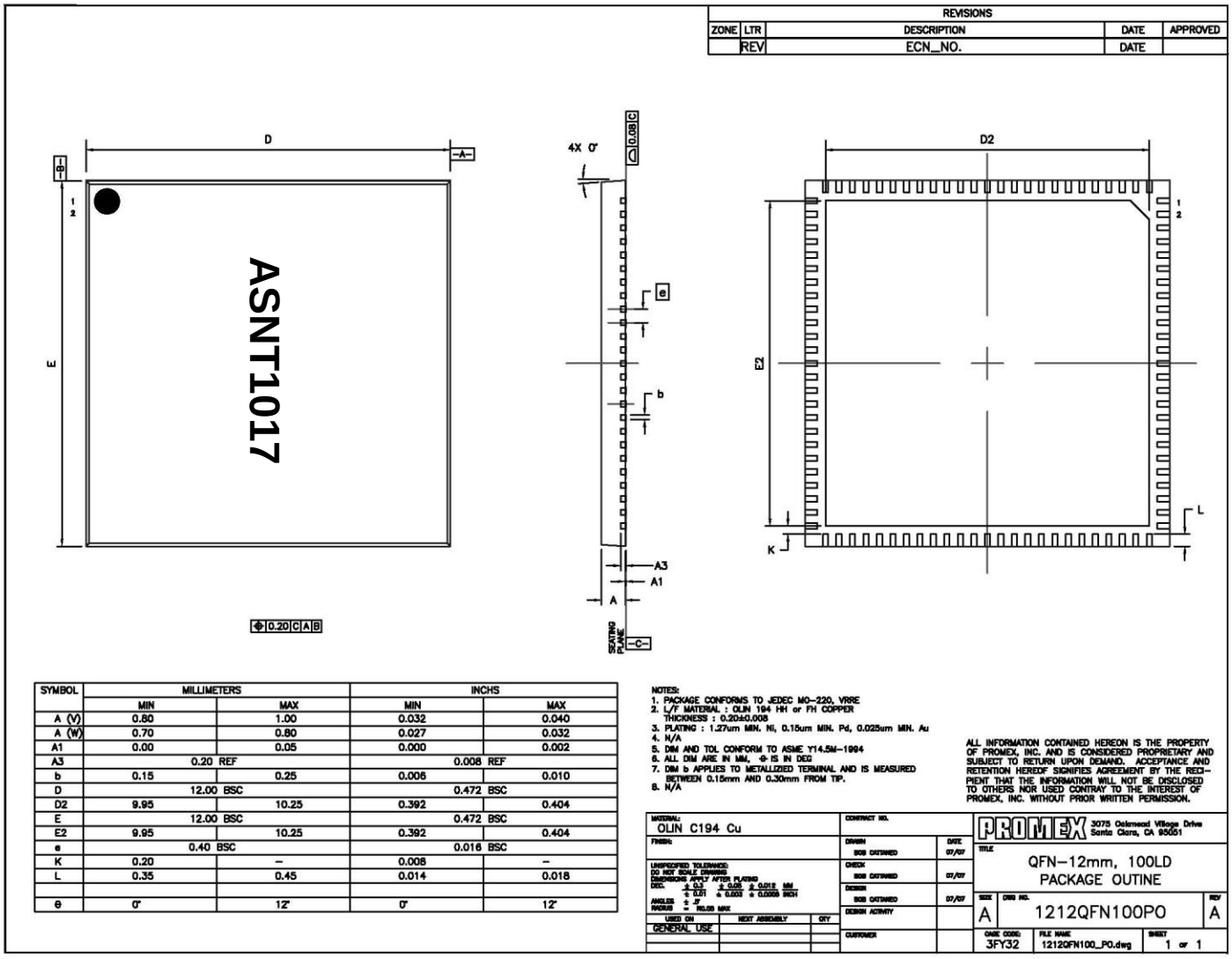

Fig. 4. Package Drawing

The chip die is housed in a custom 100-pin QFN package shown in Fig. 4. Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the vcc plain that is power for the positive supply.

The part's identification label is ASNT1017-PQA. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
2.4.2	05-2020	Updated Package Information
2.3.2	07-2019	Updated Letterhead
2.3.1	08-2013	Corrected locking range for the 14*GHz* VCO (changed frequencies of the HS and reference clocks in Description and Electrical Characteristics)
2.2.1	07-2013	Corrected Format Corrected Description Corrected Electrical Characteristics
2.1.1	06-2012	Corrected Terminal Functions (offpll pin assigned as a control)
2.0.1	06-2012	Corrected Description Revised Electrical Characteristics section Corrected Terminal Functions Revised Package Information section New template
1.0	01-2011	First release